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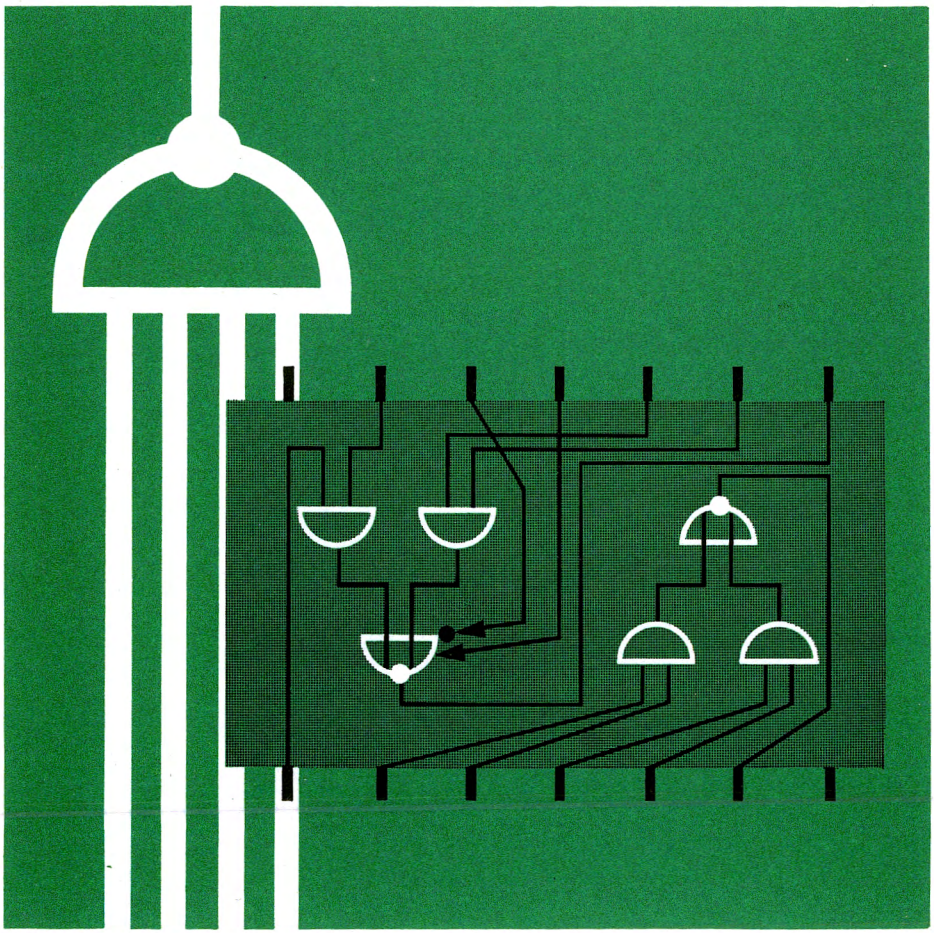

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SIEMENS AKTIENGESELLSCHAFT

Published by Bereich Halbleiter 8000 München 80, Balanstraße 73

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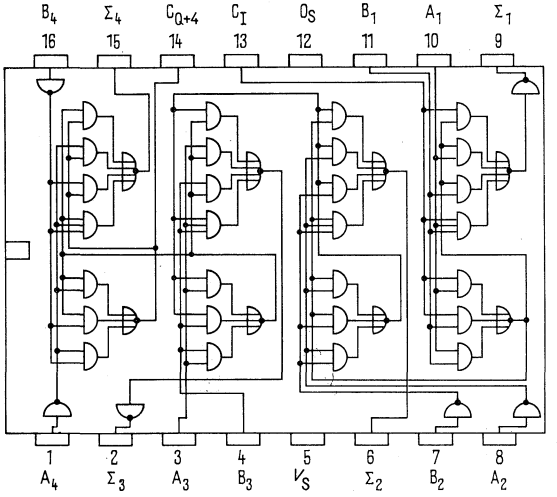
Contents



Pin configuration
top view

Truth table

inputs				outputs					
				C_I=L / C_2=L			C_I=H / C_2=H		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_{Q+4}	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_{Q+4}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Notes:

The input conditions at A_1, A_2, B_1, B_2 and C_I are used to determine the output state at Σ_1 and Σ_2 and the internal carry C_2.
The input conditions at C_2, A_3, B_3, A_4 and B_4 determine the output state at Σ_3, Σ_3 and C_{Q+4}.

FLH 251 – 4929
FLH 255 – 49829

order numbers

FLH 251: Q67000–H138
FLH 255: Q67000–H247

Dual 2-input NAND-Gate and Quadruple Inverter

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=400 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V		8	16	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		24	44	mA

Delay times, V_S=5 V, T_A=25 °C

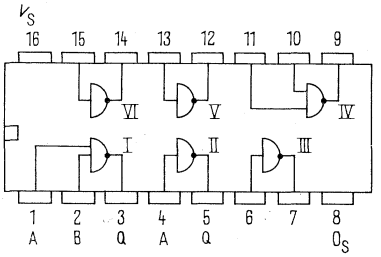
Propagation delay	t_{PHL}	C_1=15 pF		7	15	ns
	t_{PLH}	R_L=400 Ω		11	22	ns

Logical data

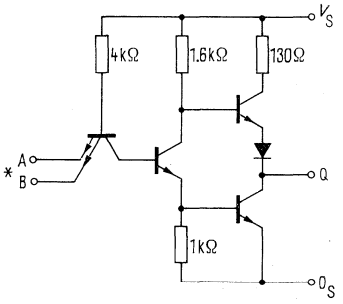
Output load factor, each output	F_Q			10	
Input load factor, each input	F_I			1	

Logic gate I and IV $Q=\overline{AB}$

Logic gate II, III, V, and VI $Q=\overline{A}$



Pin configuration
top view



Schematic (each gate)

*) Input B gate I and IV only

FLH 271 – 7405
FLH 271 S – 7405 S1
FLH 271 T – 7405 S3
FLH 275 – 8405
FLH 275 S – 8405 S1
FLH 275 T – 8405 S3

order numbers

FLH 271: Q67000–H154
FLH 271S: Q67000–H462
FLH 271T: Q67000–H459
FLH 275: Q67000–H248
FLH 275S: Q67000–H460
FLH 275T: Q67000–H461

Hexinverter with Open Collector Output

The FLH 271/275, S, and T are suited for wired-AND-connection. Resistance table and formulae see FLH 201.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
H-output current, each output	I_{QH}	V_S=4.75 V, V_Q=5.5 V, V_{IL}=0.8 V			250	µA
H-supply current	I_{SH}	V_S=5.0 V, V_I=0 V, T_A=25 °C		6	12	mA
L-supply current	I_{SL}	V_S=5.0 V, V_I=5.0 V, T_A=25 °C		18	33	mA

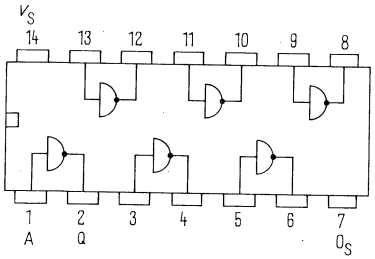
Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	R_L=400 Ω, C_1=15 pF		8	15	ns
	t_{PLH}	R_L=4 kΩ		40	55	ns

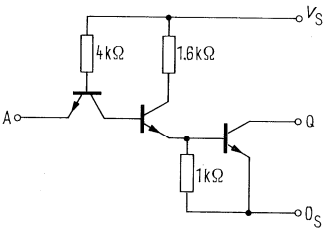
Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	
Logic		$Q=\overline{A}$				

FLH 271/275S: as FLH 271/275, however output 15 V/250 µA
FLH 271/275T: as FLH 271/275, however output 5,5 V/50 µA



Pin configuration
top view



Schematic (each gate)

FLH 281 – 7442
FLH 285 – 8442

order numbers

FLH 281: Q67000–L3
FLH 285: Q67000–L13

BCD-Decimal-Decoder

The FLH 281/285 decodes binary-coded-decimal numbers. The inputs of the FLH 281/285 may be directly connected to the outputs of any decimal counter. The reanired connections are A — Q_A, B — Q_B, C — Q_C, and D — Q_D.

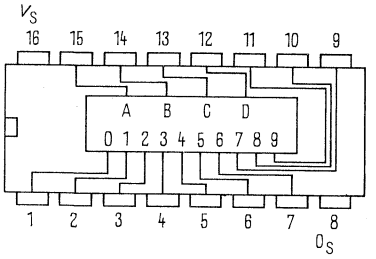
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4,75 V	2.0			V
L-input voltage	V_{IL}	V_S=4,75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2 V, V_{IL}=0.8 V, $-I_{QH}$=400 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2 V, V_{IL}=0.8 V, I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_I=5.5 V, V_S=5.25 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_{IL}=0.4 V, V_S=5.25 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
Supply current	I_S	V_S=5.25 V		28	56	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay to output 0	t_{PHL}	R_L=400 Ω, C_1=15 pF	10	22	30	ns
	t_{PLH}		10	17	25	ns
to output 1 to 9	t_{PHL}			23	35	ns
	t_{PLH}			26	35	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	



Pin configuration
top view

Truth table

BCD-inputs				Decimal-outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

FLH 291 – 7403
FLH 291 S – 7403 S1
FLH 291 T – 7403 S3
FLH 295 – 8403
FLH 295 S – 8403 S1
FLH 295 T – 8403 S3

order numbers

FLH 291: Q67000–H149
FLH 291S: Q67000–H242
FLH 291T: Q67000–H429
FLH 295: Q67000–H249
FLH 295S: Q67000–H437
FLH 295T: Q67000–H438

Quadruple 2-input NAND-Gate with Open Collector Output

The FLH 291/295, S and T are suited for wired-AND-connections. Resistance table and formulae see FLH 201.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{SS}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
H-output current, each output	I_{QH}	V_S=4.75 V V_{IL}=0.8 V, V_Q=5.5 V			250	µA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V		4	8.0	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		12	22	mA

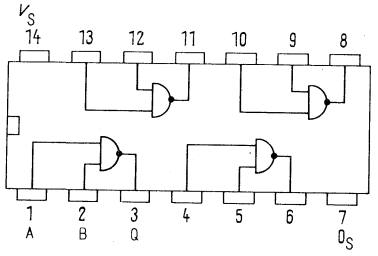
Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	R_L=400 Ω | C_1=15 pF		8	15	ns
	t_{PLH}	R_L=4.0 kΩ | C_1=15 pF		35	45	ns

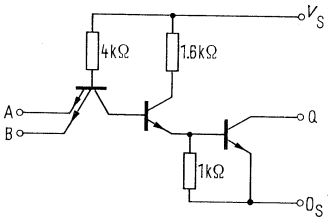
Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	
Logic		$Q=\overline{A \wedge B}$				

FLH 291/295 S: as FLH 291/295, however output 15 V/250 µA
FLH 291/295 T: as FLH 291/295, however output 5.5 V/50 µA



Pin configuration
top view



Schematic (each gate)

FLH 291 U – 7426
FLH 295 U – 8426

order numbers
FLH 291U: Q67000–H506
FLH 295U: Q67000–H507

Quadruple 2-input NAND-Gate with Open Collector Output with 12 V/ 50 µA

The FLH 291/295 U are suited for wired-AND-connections. Resistance table and formulae see FLH 201. The maximum output voltage at output Q ist 15 V, the maximum output reverse current is 50 µA at 12 V. Thus the circuit is in particular intended for 12-V-systems.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage (output transistor blocked)	V_{QH}	V_S=4.75 V V_{IL}=0.8 V, I_{QH}=1 mA			15	V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V I_{QL}=16 mA			0.4	V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
	I_I	V_I=5.5 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
H-output current, each output	I_{QH}	V_S=4.75 V | V_Q=12 V V_{IL}=0.5 V			50	µA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V		4.0	8.0	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		12	22	mA

Delay times, V_S=5 V, T_A=25 °C

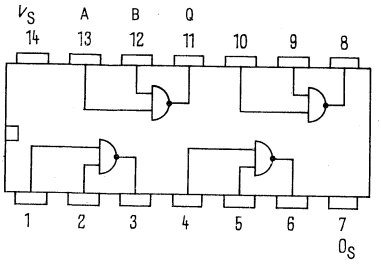
Propagation delay	t_{PHL}	C_L=15 pF		11	17	ns
	t_{PLH}	R_L=1 kΩ		16	24	ns

Logical data

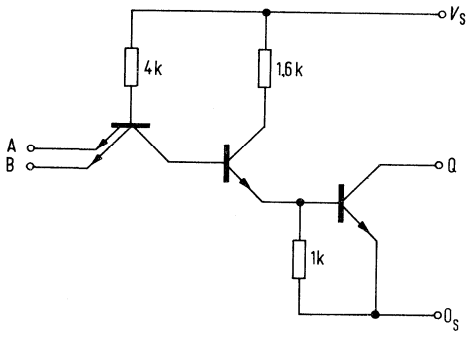
Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	

Logic $Q=\overline{AB}$

FLH 291 U – 8426
FLH 295 U – 7426



Pin configuration
top view



Schematic (each gate)

FLH 321 – 4930
FLH 325 – 49830

order numbers

FLH 321: Q67000–H139
FLH 325: Q67000–H315

Quadruple 2-input NAND-Powergate

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=1.2 mA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=48 mA		0.28	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =2.25 V			1.0	mA
L-input current each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		70	mA
H-Supply current	I_{SH}	V_S=5.25 V V_I=0 V		8	16	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		34	54	mA

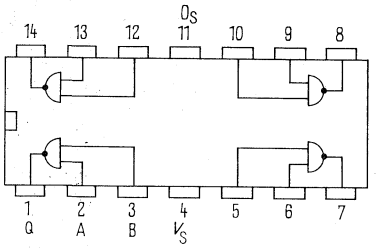
Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	C_L=15 pF		8	15	ns
	t_{PLH}	R_L=400 Ω		13	22	ns

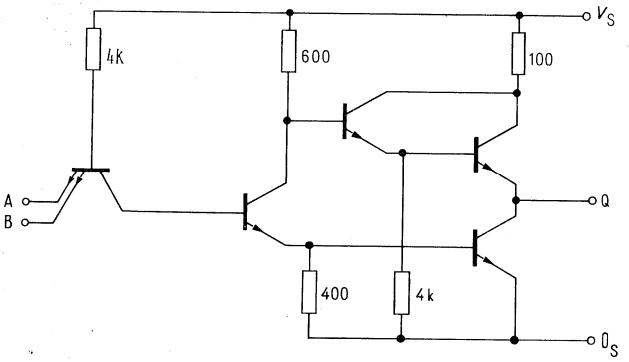
Logical data

Output load factor, each output	F_Q				30	
Input load factor, each input	F_I				1	
Logic		$Q=\overline{AB}$				

For development recommended: **FLH 531**



Pin configuration
top view



Schematic (each gate)

FLH 331 – 4931
FLH 335 – 49831

order numbers

FLH 331: Q67000–H140
FLH 335: Q67000–H316

Dual 5-input NAND-Gate

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V, $-I_{QH}$=400 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH} I_I	V_H=2,4 V | V_S V_I=5.5 V | =5.25 V			40 1.0	µA mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V		2	4	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		6	12	mA

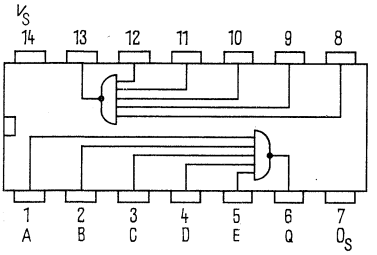
Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL} t_{PLH}	C_L=15 pF R_L=400 Ω		8 13	15 22	ns ns

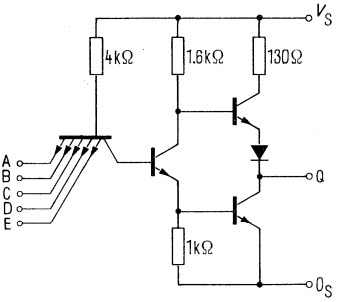
Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	

Logic $Q=\overline{ABCDG}$



Pin configuration
top view



Schematic (each gate)

FLH 341 – 7486
FLH 345 – 8486

order numbers
FLH 341: Q67000–H354
FLH 345: Q67000–H297

Quadruple 2-input Exclusive-OR-Gate

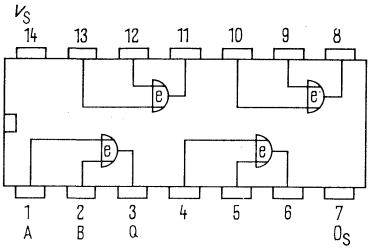
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V, V_{IH}=2 V $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V V_{IL}=0.8 V, V_{IH}=2 V, I_{QL}=16 mA			0.4	V
H-input current, each input	I_{IL}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =5.25 V			1	mA
L-input current, each input	$-I_{IH}$	V_S=5.25 V V_{IL}=0,4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V V_{IH}=4.5 V, V_{IL}=0 V	18		55	mA
Supply current	I_S	V_S=5.25 V V_I=4.5 V		30	50	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	C_L=15 pF, R_L=400 Ω		11	17	ns
2nd input L-signal	t_{PLH}			15	23	ns
Propagation delay	t_{PHL}			13	22	ns
2nd input H-signal	t_{PLH}			18	30	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	
Logic		$Q=A\bar{B}+\bar{A}B$				



Pin configuration
top view

Truth table

inputs		output
A	B	Q
L	L	L
L	H	H
H	L	H
H	H	I

FLH 351 – 7413
FLH 355 – 8413
FLH 601 – 74132
FLH 605 – 84132

order numbers

FLH 351:	Q67000–L19
FLH 355:	Q67000–H325
FLH 601:	Q67000–H618
FLH 605:	Q67000–H624

FLH 351, FLH 355 Dual 4-input NAND-Schmitt-Trigger
FLH 601, FLH 605 Quadruple 2-input NAND-Schmitt-Trigger

These Schmitt-Triggers have different threshold voltages for rising and falling input signals (V_{TI} and V_{TU}). The hysterisis is 0.8 V. The internal temperature compensation ensures an excellent stability of the threshold voltages and hysteresis over the entire temperature range. The circuits can be triggered either by slowly rising input pulses or by DC-voltages. The output signal is in either case TTL-compatible. The operating frequency is above 10 MHz typically.
Applications: TTL-systems interface, pulse shaper, pulse stretcher, threshold detector and multivibrator.

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
Upper threshold voltage	V_{Tu}	V_S=5.0 V	1.5	1.7	2.0	V
Lower threshold voltage	V_{TI}	V_S=5.0 V	0.6	0.9	1.1	V
Hysterisis	V_H	V_S=5.0 V	0.4	0.8		V
H-output voltage	V_{QH}	V_S=4.75 V $-I_{QH}$=800 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V I_{QL}=16 mA		0.22	0.4	V
Input current at V_{Tu}	$-I_{Tu}$	V_S=5.0 V, V_I=1.7 V		0.65		mA
Input current at V_{TI}	$-I_{TI}$	V_S=5.0 V V_I=0.9 BV				
Input current at V_{TI}	$-I_{TI}$	V_S=5.0 V, V_I=0.9 V		0.85		mA
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =5,25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V		1.0	1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V, V_I=0 V		14	28	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		20	36	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	C_L=15 pF		15	22	ns
	t_{PLH}	R_L=400 Ω		18	27	ns

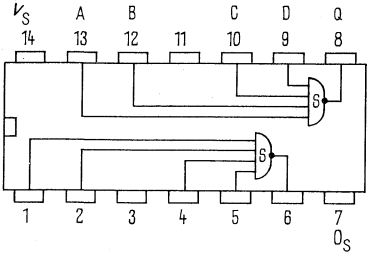
Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	

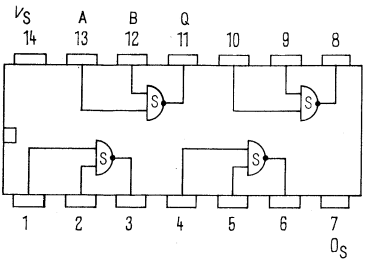
Logic FLH 351/5 $Q=\overline{ABCD}$

Logic FLH 601/5 $Q=\overline{AB}$

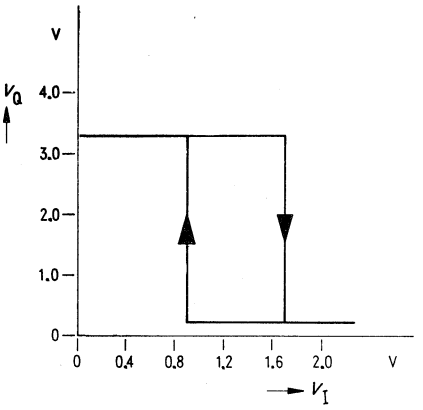
FLH 351, FLH 355



FLH 601, FLH 605

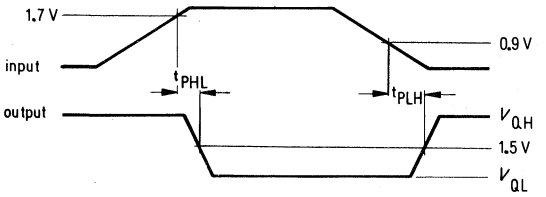


Pin configurations, top view

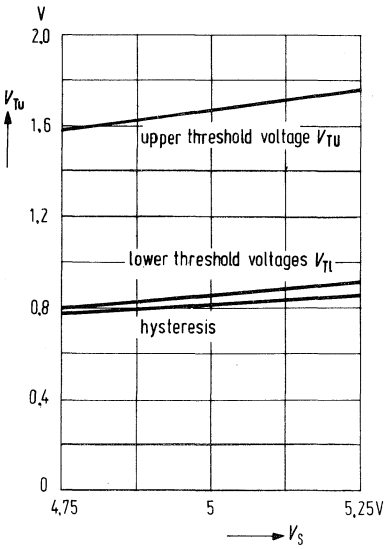


Typical transfer characteristic $V_Q = f(V_I)$

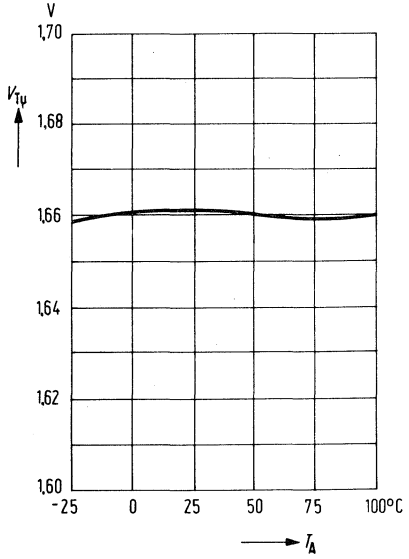
Pulse diagram



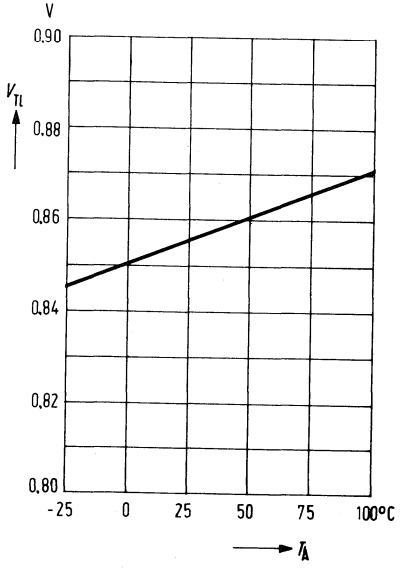
Threshold voltages and hysteresis as a function of the supply voltage V_S at T_A=25 °C



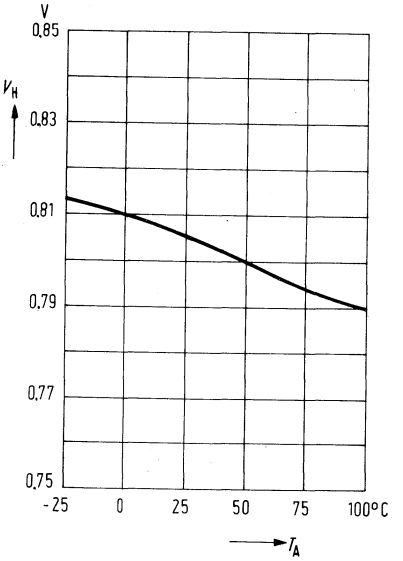
Upper threshold voltage V_{Tu} as a function of the ambient temperature T_A at V_S=5 V



Lower threshold voltage V_{TI} as a function of the ambient temperature T_A at $V_S = 5$ V



Hysteresis V_H as a function of the ambient temperature T_A at $V_S = 5$ V



FLH 361 – 7443
FLH 365 – 8443

order numbers

FLH 361: Q67000–H35
FLH 365: Q67000–H404

Excess-3-Decimal-Dekoder

The FLH 361/365 decode the Excess-3-code into the decimal numbers 0 to 9

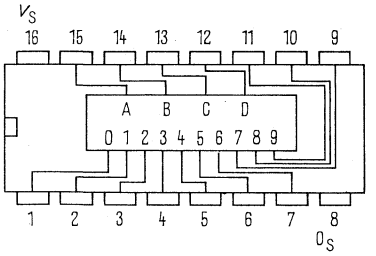
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IH}=2 V, V_{IL}=0.8 V $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, V_{IL}=0.8 V I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
Supply current	I_S	V_S=5.25 V		28	56	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	R_L=400 Ω C_L=15 pF	10	23	35	ns
	t_{PLH}		10	26	35	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	



Pin configuration
top view

Truth table

excess-3-inputs				decimal-outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	H	H	H	L	H	H	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H	H	H
L	H	H	H	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	L	H
H	H	L	L	H	H	H	H	H	H	H	H	H	L
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H

FLH 371 - 7444
FLH 375 - 8444

order numbers

FLH 371: Q67000–H357
FLH 375: Q67000–H403

Excess-3-Gray-Decimal-Decoder

The FLH 371/375 decode the Excess-3-Gray-code into the decimal numbers 0 to 9 (single step code).

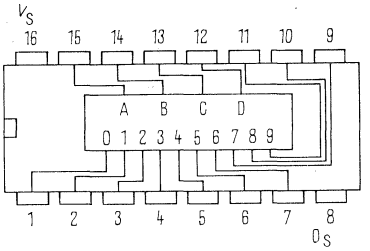
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IH}=2 V, V_{IL}=0.8 V $-I_{QH}$=400 µA	2.4			
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, V_{IL}=0.8 V I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH} I_I	V_{IH}=2.4 V | V_S V_I=5.5 V | =5.25 V			40 1.0	µA mA
L-input current, each input	$-I_{IH}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
Supply current	I_S	V_S=5.25 V		28	56	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL} t_{PLH}	R_L=400 Ω C_L=15 pF	10 10	23 26	35 35	ns ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	



Pin configuration
top view

Truth table

excess-3-Gray-inputs				decimal-outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	H	L	H	H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H

FLH 381 – 7408
FLH 385 – 8408
FLH 391 – 7409
FLH 395 – 8409

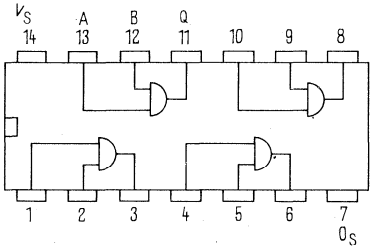
order numbers

FLH 381:	Q67000–H398
FLH 385:	Q67000–H402
FLH 391:	Q67000–H399
FLH 395:	Q67000–H425

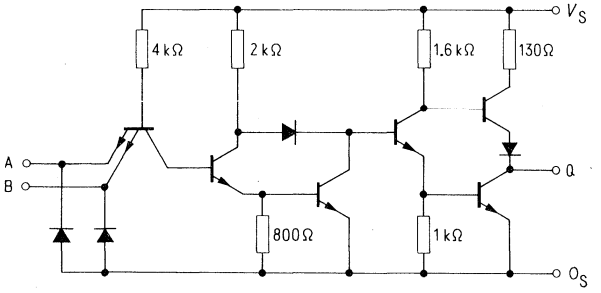
FLH 381, FLH 385 Quadruple 2-input AND-Gate
FLH 391, FLH 395 Quadruple 2-input AND-Gate with Open Collector Output

The inputs of the gates are protected against reflexions by clamping diodes. The FLH 391/395 are suited for wired-AND-connections. Formulae and resistance table see FLH 201.

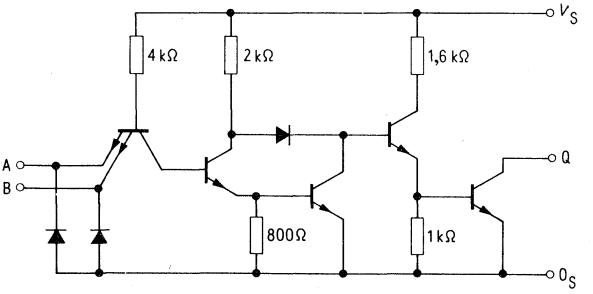
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage, FLH 381/385	V_{QH}	V_S=4.75 V V_{IH}=2.0 V $-I_{QH}$=800 µA	2.4			V
H-output current, FLH 391/395	I_{QH}	V_S=4.75 V V_{IH}=2 V, V_{QH}=5.5 V			250	µA
L-output voltage	V_{QL}	V_S=4.75 V V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_S=5.5 V | =5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output of FLH 381/385	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V, V_I=5 V		10	15	mA
L-supply current	I_{SL}	V_S=5.25 V, V_I=0 V		18	26	mA
Delay times, V_S=5 V, T_A=25 °C						
Propagation delay FLH 381/385	t_{PHL}	C_L=15 pF, R_L=400 Ω		17.5	27	ns
	t_{PLH}			12	19	ns
Propagation delay FLH 391/395	t_{PHL}	C_L=15 pF, R_L=400 Ω		21	32	ns
	t_{PLH}			16	24	ns
Logical data						
Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	
Logic		$Q=AB$				



Pin configuration
top view



Schematic (each gate)
FLH 381, FLH 385



Schematic (each gate)
FLH 391, FLH 395

FLH 401 – 74181
FLH 405 – 84181

order numbers
FLH 401: Q67000–H431
FLH 405: Q67000–H427

4-bit-Arithmetic-Logic-Unit (ALU)

The FLH 401/405 are fast arithmetic logic units which perform either 16 binary arithmetic operations with 2 4-bit-words or 16 logic functions with 2 variables. The operating modes are selected by the function-select-inputs S and the mode control input M. The ALU will perform positive and negative logic if the pin-designations and the carry informations are interpreted correspondingly (see table below).

Logic operation mode: Mode control M = H-state. AND, NAND, OR, NOR, Exclusive-OR and 10 additional function can be realized.

Arithmetic operation mode: Mode control M = L-state. Calculations such as addition and subtraction are possible. By adding the look-ahead carry-generator FLH 411/415 to the circuit high-speed operations can be performed. The typical addition time for the FLH 401/405 is 24 ns for 4 bits. When the circuit is expanded to 16 bits by means of one FLH 411/415, a total addition time of 37 ns results, i. e. 2.2 ns per bit. The carry inputs C_I and the carry output C_{Q+4} can be connected in series if the delay time is not important. 12 ns delay time is required for each additional 4-bit-word. Thus the addition time of 2 8-bit-words is 36 ns. Subtractions are realized by means of the 1's compliment which is generated internally. The result A–B–1 requires an end-around carry.

The FLH 401/405 can also be used as a comparator. The output A = B assumes an H-state if words of equal magnitude are supplied to the inputs A and B. The output A = B has an open collector. Thus a comparison of more than 4 bits is possible by means of wired-AND-connection (formulae and resistance table see FLH 201). The carry output C_{Q+4} indicates the corresponding magnitude as follows:

	input C_I	output C_{Q+4}	magnitude
positive logic	H	H	$A \leqq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geqq B$
negative logic	L	L	$A \leqq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geqq B$

When used as a comparator, the function-select-inputs must be placed to subtraction mode $S_0S_1S_2S_3$ = LHHL.

Function-select-inputs S_3 S_2 S_1 S_0	Positive logic		
	Logic operation mode: M=H	Arithmetic operation mode: M=L	
		C_I=0; $\overline{C}_I$=1=H	$\overline{C}_I$=1; C_I=0=L
L L L L	F=$\overline{A}$	F=A	F=A PLUS 1
L L L H	F=$\overline{A+B}$	F=A+B	F=(A+B) PLUS 1
L L H L	F=$A\overline{B}$	F=A+$\overline{B}$	F=(A+$\overline{B}$) PLUS 1
L L H H	F=0	F=MINUS 1 (2's COMP)	F=ZERO
L H L L	F=$\overline{AB}$	F=A PLUS A$\overline{B}$	F=A PLUS A$\overline{B}$ PLUS 1
L H L H	F=$\overline{B}$	F=(A+B) PLUS A$\overline{B}$	F=(A+B) PLUS A$\overline{B}$ PLUS 1
L H H L	F=A$\overline{B}$+$\overline{A}$B	F=A MINUS B MINUS 1	F=A MINUS B
L H H H	F=A$\overline{B}$	F=A$\overline{B}$ MINUS 1	F=A$\overline{B}$
H L L L	F=$\overline{A}$+B	F=A PLUS AB	F=A PLUS AB PLUS 1
H L L H	F=$\overline{A\overline{B}+\overline{A}B}$	F=A PLUS B	F=A PLUS B PLUS 1
H L H L	F=B	F=(A+$\overline{B}$) PLUS AB	F=(A+$\overline{B}$) PLUS AB PLUS 1
H L H H	F=AB	F=AB MINUS 1	F=AB
H H L L	F=1	F=A PLUS A*	F=A PLUS A PLUS 1
H H L H	F=A+$\overline{B}$	F=(A+B) PLUS A	F=(A+B) PLUS A PLUS 1
H H H L	F=A+B	F=(A+$\overline{B}$) PLUS A	F=(A+$\overline{B}$) PLUS A PLUS 1
H H H H	F=A	F=A MINUS 1	F=A

Function-select-inputs S_3 S_2 S_1 S_0	Negative logic		
	Logic operation mode: M=H	Arithmetic operation mode: M=L	
		C_I=0=L	C_I=1=H
L L L L	F=$\overline{A}$	F=A MINUS 1	F=A
L L L H	F=$\overline{AB}$	F=AB MINUS 1	F=A$\overline{B}$
L L H L	F=$\overline{A}$+B	F=A$\overline{B}$ MINUS 1	F=A$\overline{B}$
L L H H	F=1	F=MINUS 1 (2's COMP)	F=ZERO
L H L L	F=$\overline{A+B}$	F=A PLUS (S+$\overline{B}$)	F=A PLUS (A+$\overline{B}$) PLUS 1
L H L H	F=$\overline{B}$	F=AB PLUS (A+$\overline{B}$)	F=AB PLUS (A+$\overline{B}$) PLUS 1
L H H L	F=$\overline{A\overline{B}+\overline{A}B}$	F=A MINUS B MINUS 1	F=A MINUS B
L H H H	F=A+$\overline{B}$	F=A+$\overline{B}$	F=(A+$\overline{B}$) PLUS 1
H L L L	F=$\overline{A}$B	F=A PLUS (A+B)	F=A PLUS (A+B) PLUS 1
H L L H	F=$\overline{A\overline{B}+\overline{A}B}$	F=A PLUS B	F=A PLUS B PLUS 1
H L H L	F=B	F=A$\overline{B}$ PLUS (A+B)	F=A$\overline{B}$ PLUS (A+B) PLUS 1
H L H H	F=A+B	F=A+B	F=(A+B) PLUS 1
H H L L	F=0	F=A PLUS A*	F=A PLUS A PLUS 1
H H L H	F=A$\overline{B}$	F=AB PLUS A	F=AB PLUS A PLUS 1
H H H L	F=AB	F=A$\overline{B}$ PLUS A	F=A$\overline{B}$ PLUS A PLUS 1
H H H H	F=A	F=A	F=A PLUS 1

*) Each bit is shifted to the more significant position.

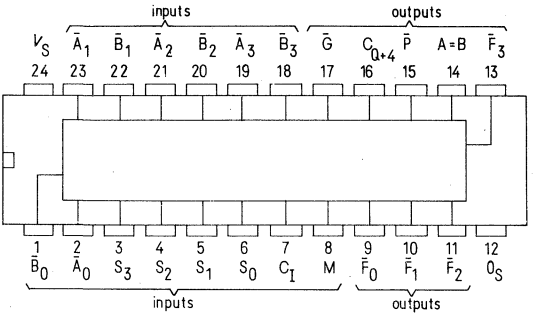
FLH 401
FLH 405

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75, V_{IH}=2.0 V V_{IL}=0.8 V, $-I_{QH}$=800µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
H-output current at A=B	I_{QH}	V_S=4.75 V, V_{IH}=2.0 V V_{IL}=0.8 V, V_{QH}=5.5 V			250	µA
DC noise margin	V_{nm}		0.4	1.0		V
H-input current at M	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
H-input current at $\overline{A}$ or $\overline{B}$	I_{IH}				120	µA
H-input current at S	I_{IH}				160	µA
H-input current at C_I	I_{IH}				200	µA
Input current, each input	$-I_I$	V_S=5.25 V, V_I=5.5 V			1	mA
L-input current at M	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
L-input current at $\overline{A}$ or $\overline{B}$	I_{IL}				4.8	mA
L-input current at S	$-I_{IL}$				6.4	mA
L-input current at C_I	$-I_{IL}$				8.0	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		94	150	mA

Logical data

Output load factor, H-signal	F_{QH}		20
each output L-signal	F_{QL}		10
Input load factor at M	F_I		1
Input load factor at $\overline{A}$ or $\overline{B}$	F_I		3
Input load factor at S	F_I		4
Input load factor at C_I	F_I		5



Pin configuration
top view

The pin designation has to be interpreted as follows:

for positive logic	for negative logic	function
A_3, A_2, A_1, A_0	$\overline{A}_3$, $\overline{A}_2$, $\overline{A}_1$, $\overline{A}_0$	A-inputs
B_3, B_2, B_1, B_0	$\overline{B}_3$, $\overline{B}_2$, $\overline{B}_1$, $\overline{B}_0$	B-inputs
S_3, S_3, S_1, S_0	S_3, S_2, S_1, S_0	function-select-inputs
C_I	C_I	carry input
M	M	mode control
F_3, F_2, F_1, F_0	$\overline{F}_3$, $\overline{F}_2$, $\overline{F}_1$, $\overline{F}_0$	outputs
A=B	A=B	comparator output
X	$\overline{P}$	carry propagate output for FLH 411/415
C_{Q+4}	C_{Q+4}	carry output
Y	$\overline{G}$	carry generate output for FLH 411/415

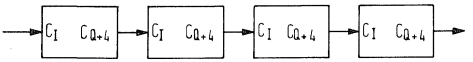
Delay times, V_S=5 V, T_A=25 °C

propagation delay	from input	to output	test condition	upper limit B	typ	lower limit A	unit
t_{PHL}	C_I	C_{Q+4}			12	18	ns
t_{PLH}	C_I	C_{Q+4}			13	19	ns
t_{PHL}	C_I	$\overline{F}$	M=0 V, operation mode SUM		13	19	ns
t_{PLH}	C_I	$\overline{F}$	or DIFF		12	18	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$	$\overline{G}$	M=0 V, S_0=S_3=4.5 V		13	19	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{G}$	S_1=S_2=0 V, operating mode SUM		13	19	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	$\overline{G}$	M=0 V, S_0=S_3=0 V		17	25	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{G}$	S_1=S_2=4.5 V, operating mode DIFF		17	25	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	$\overline{P}$	M=0 V, S_0=S_3=4.5 V,		13	19	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{P}$	S_1=S_2=0 V, operating mode SUM		17	25	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	$\overline{P}$	*M*=0 V, S_0=S_3=0 V,		17	25	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{P}$	S_1=S_2=4.5 V, operating mode DIFF		17	25	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	$\overline{F}$	M=0 V, S_0=S_3=4.5 V,		28	42	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{F}$	S_1=S_2=0 V, operating mode SUM		21	32	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	$\overline{F}$	M=0 V, S_0=S_3=0 V,		32	48	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{F}$	S_1=S_2=4.5 V, operating mode DIFF		23	34	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	$\overline{F}$	M=0 V, logic operation		32	48	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	$\overline{F}$	mode		23	34	ns
t_{PHL}	$\overline{A}$ „ $\overline{B}$	A=B	M=0 V, S_0=S_3=0 V,		35	50	ns
t_{PLH}	$\overline{A}$ „ $\overline{B}$	A=B	S_1=S_2=4.5 V, operating mode DIFF		32	48	ns

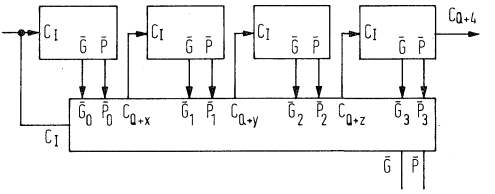
FLH 401
FLH 405
FLH 411
FLH 415

Typical applications of the ALU FLH 401/405 and the look-ahead carry-generator FLH 411/415

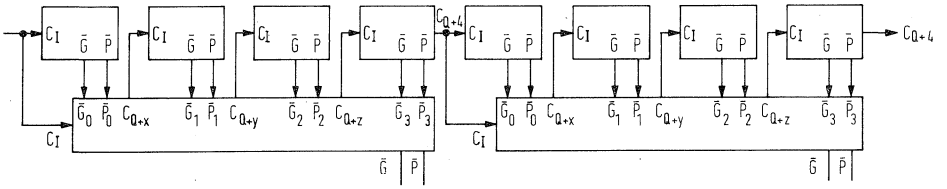
16-bit-ALU with ripple carry
4 FLH 401



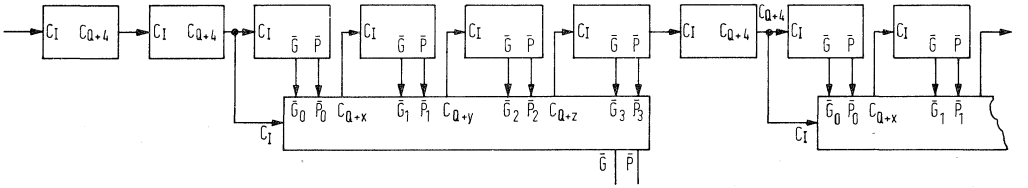
16-bit-ALU with look-ahead carry
4 FLH 401 and 1 FLH 411



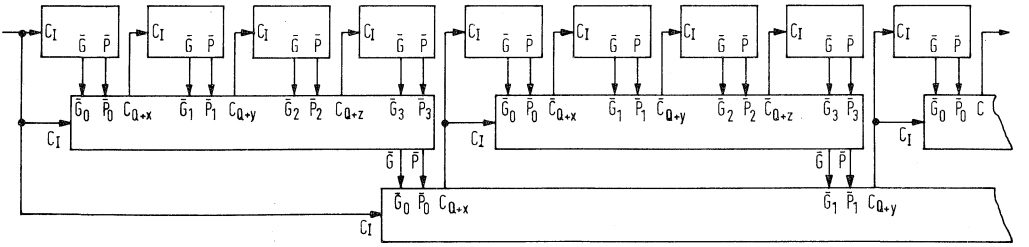
32-bit-ALU with look-ahed carry for 16 bits each
8 FLH 401 and 2 FLH 411



n-bit-ALU with combined ripple and look-ahead carry



64-bit-ALU with full look-ahead carry
16 FLH 401 and 5 FLH 411



Typical addition times

number of bits	total addition time ns	addition time per bit ns	number of circuit elements FLH 401	FLH 411	carry
4	24	6.0	1	–	
8	36	4.5	2	–	serial
12	48	4.0	3	–	serial
12	36	3.0	3	1	parallel
16	60	3.8	4	–	serial
16	36	2.2	4	1	parallel
32	120	3.8	8	–	serial
32	96	3.0	8	1	serial-parallel
32	72	2.2	8	2	serial-parallel
32	60	1.9	8	3	parallel
48	165	3.4	12	–	serial
48	148	3.1	12	1	serial-parallel
48	132	2.7	12	2	serial-parallel
48	108	2.2	12	3	serial-parallel
48	60	1.25	12	4	parallel
64	220	3.5	16	–	serial
64	192	3.0	16	2	serial-parallel
64	172	2.7	16	3	serial-parallel
64	144	2.2	16	4	serial-parallel
64	60	0.94	16	5	parallel

FLH 411 – 74182
FLH 415 – 84182

order numbers

FLH 411: Q67000–H486
FLH 415: Q67000–H501

Look-Ahead Carry-Generator for ALU

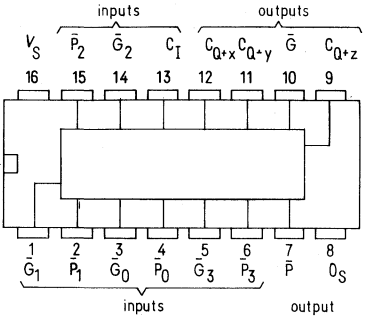
The FLH 411/415 are high-speed, look-ahead carry-generators for 4 binary adders. The units can be cascaded to n bits. The typical propagation delay is 13 ns.
The FLH 411/415 are in particular intended for the ALU FLH 401/405 and provide the carry operation for every 4 ALUs. To achieve full look-ahead carry propagation an additional FLH 411/415 must be connected in parallel to every 4 look-ahead carry-generators (see preceding pages).

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, V_{IL}=0.8V, $-I_{HQ}$=800µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current at C_I	I_{IH}				80	µA
H-input current at $\overline{P}_3$	I_{IH}				120	µA
H-input current at $\overline{P}_2$	I_{IH}				160	µA
H-input current at $\overline{P}_0$, $\overline{P}_1$ or $\overline{G}_3$	I_{IH}	V_S=5.25 V, V_{IH}=2.4V			200	µA
H-input current at $\overline{G}_0$ or $\overline{G}_2$	I_{IH}				360	µA
H-input current at $\overline{G}_1$	I_{IH}				400	µA
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
L-input current at C_I	$-I_{IL}$				3.2	mA
L-input current at $\overline{P}_3$	$-I_{IL}$				4.8	mA
L-input current at $\overline{P}_2$	$-I_{IL}$				6.4	mA
L-input current at $\overline{P}_0$, $\overline{P}_1$ or $\overline{G}_3$	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			8	mA
L-input current at $\overline{G}_0$ or $\overline{G}_2$	$-I_{IL}$				14.4	mA
L-input current at $\overline{G}_1$	$-I_{IL}$				16	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	40		100	mA
H-supply current	I_{SH}			27		mA
L-supply current	I_{SL}			45	72	mA

Logical data

Output load factor, each output	H-signal	F_{QH}			20	
	L-signal	F_{QL}			10	



Pin configuration
top view

Logic functions:

$C_{Q+x} = G_0 + P_0C_I$

$C_{Q+y} = G_1 + P_1G_0 + P_1P_0C_I$

$C_{Q+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_I$

$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$

$\overline{P} = \overline{P_3P_2P_1P_0}$

The pin-designations have to be interpreted as follows:

for positive logic	for negative logic	function
Y_0, Y_1, Y_2, Y_3	$\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$	carry-generate-input
X_0, X_1, X_2, X_3	$\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$	carry-propagate-input
C_I	C_I	carry-input
$\overline{C_{Q+x}}, \overline{C_{Q+y}}, \overline{C_{Q+z}}$	$C_{Q+x}, C_{Q+y}, C_{Q+z}$	carry-output
Y	$\overline{G}$	carry-generate-output
X	$\overline{P}$	carry-propagate-output

FLH 421 – 74180
FLH 425 – 84180

order numbers

FLH 421: Q67000–H299
FLH 425: Q67000–H453

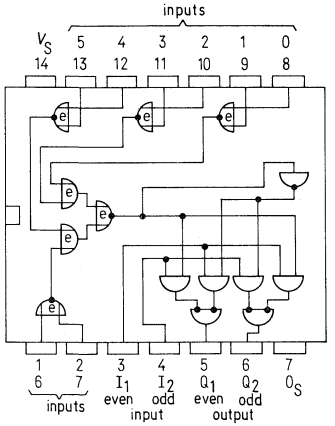
8-Bit-Parity-Generator

FLH 421/425 are parity generators and checkers. The odd and even outputs indicate if the 8-bit-information present at input 0 to 7 is odd or even. The circuit can be expanded serially to n bits by means of 2 control inputs.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, V_{IL}=0.8V, $-I_{IH}$=800µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, V_{IL}=0.8 V, I_{IL}=16 mA			0.4	V
H-input current each data input	I_{IH}	V_{IH}=2,4 V | V_S=5.25 V			40	µA
	I_I	V_I=5.5 V | V_S=5.25 V			1	mA
L-input current, each data input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
H-input current at I even and I odd	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			80	µA
	I_I	V_I=5.5 V | V_S=5.25 V			1	mA
L-input current at I even and I odd	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
Supply current	I_S	V_S=5.25 V		34	56	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay from data inputs to Q even	t_{PLH}	C_L=15 pF, R_L=400Ω, I odd grounded		40	60	ns
	t_{PHL}			45	68	ns
from data inputs to Q odd	t_{PLH}			32	48	ns
	t_{PHL}			25	38	ns
from data inputs to Q even	t_{PLH}	C_L=15 pF, R_L=400Ω, I even grounded		32	48	ns
	t_{PHL}			25	38	ns
from data inputs to Q odd	t_{PLH}			40	60	ns
	t_{PHL}			45	68	ns
from I even or I odd to Q even or Q odd	t_{PLH}	C_L=15 pF, R_L=400Ω		13	20	ns
	t_{PHL}			7	10	ns



Pin configuration
top view

Truth table

inputs			outputs	
Σ of H-signals at 0 to 7	I even	I odd	Q even	Q odd
even	H	L	H	L
odd	H	L	L	H
even	L	H	L	H
odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

X = L or H-signal

Logical data

		upper limit A
Output load factor, H-signal	F_{QH}	20
each output L-signal	F_{QL}	10
Input load factor		
at I even or I odd	F_I	2
remaining inputs	F_I	1

FLH 431 – 7485
FLH 435 – 8485

order numbers

FLH 431: Q67000–H494
FLH 435: Q67000–H508

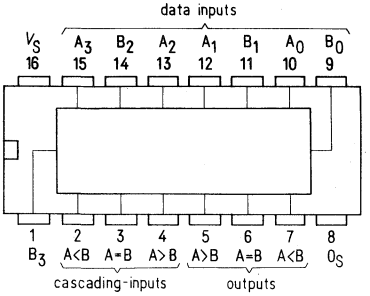
4-Bit-Comparator

The FLH 431/435 compare 2 binary-coded 4-bit-words (word A and B) and supply the information: A > B, A = B, A < B.
The circuit can be easily cascaded to compare words of n bits by means of 3 control inputs. No additional logic is required. The propagation delay increases for each additional 4-bit-word by the signal delay of 2 gates. Thus the comparison of 2 8-bit-words requires 38 ns typically. The typical delay of 4-bit-words is 24 ns.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
Input clamping voltage	$-V_I$	V_S=4.75 V, $-I_I$=12 mA			1.5	V
H-output voltage	V_{QH}	V_S=4.75V, $-I_{QH}$=400 µA V_{IH}=2 V, V_{IL}=0.8 V	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA V_{IH}=2 V, V_{IL}=0.8 V			0.4	V
H-input current, each input	I_{IH}	V_{IH}=2.4 V			120	µA
except A<B and A>B	I_I	V_I=5,5 V | V_S=5.25 V			1.0	mA
H-input current at	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
input A<B or A>B	I_I	V_I=5.5 V | V_S=5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V			4.8	mA
except A<B and A>B		V_{IL}=0.4 V				
L-input current at	$-I_{IL}$	V_S=5.25 V			1.6	mA
input A<B or A>B		V_{IL}=0.4 V				
Short circuit output current, each output	$-I_Q$	V_S=5.25	18		55	mA
Supply current	I_S	V_S=5.25 V		56	88	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay						
from input A or B to	t_{PLH}			17	26	ns
output A < B or A > B	t_{PHL}			20	30	ns
from input A or B to	t_{PLH}			23	35	ns
output A = B	t_{PHL}			20	30	ns
from input A < B or A = B	t_{PLH}	C_L=15 pF		7	11	ns
to output A > B	t_{PHL}	R_L=400 Ω		11	17	ns
from input A = B to	t_{PLH}			13	20	ns
output A = B	t_{PLH}			11	17	ns
from input A > B or A = B	t_{PLH}			7	11	ns
to output A < B	t_{PHL}			11	17	ns



Pin configuration
top view

Truth table

data inputs				cascading inputs			outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	A > B	A < B	A = B	A > B	A < B	A = B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H

X = L or H-signal

Logical data

		upper limit A
Output load factor each output	F_a	10
Input load factor at A < B or A > B	F_i	1
remaining inputs	F_i	3

FLH 441 – 74 H87
FLH 445 – 84 H87

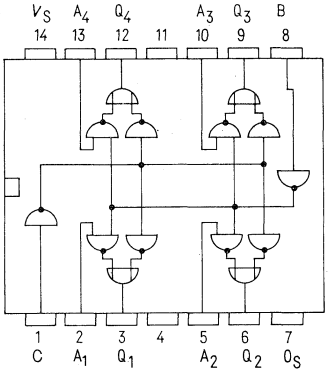
order numbers

FLH 441: Q67000–H324
FLH 445: Q67000–H510

4-Bit-Complement-Unit

The FLH 441/445 transfer 4-bit-binary-data present at the inputs A_1 to A_4 to the outputs in either true or complementary form as a function of the control lines B and C.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, V_{IL}=0.8 V, $-I_{QH}$=1 mA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, V_{IL}=0.8 V, I_{QL}=20 mA			0.4	V
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V,			50	µA
	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V,			2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_Q=0 V	40		100	mA
Supply current	I_S	V_S=5.25 V		54	89	mA
Delay times, V_S=5 V, T_A=25 °C						
Propagation delay from A to Q	t_{PHL}	C_L=25 pF, R_L=280 Ω		13	19	ns
	t_{PLH}			14	20	ns
from B and C to Q	t_{PHL}			17	25	ns
	t_{PLH}			17	25	ns
Logical data						
Output load factor, H-signal each output L-signal	F_{QH}				24	
	F_{QL}				12	
Input load factor, each input	F_I				1.25	



Pin configuration
top view

Truth Table

control-inputs		outputs			
B	C	Q_1	Q_2	Q_3	Q_4
L	L	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$
L	H	A_1	A_2	A_3	A_4
H	L	H	H	H	H
H	H	L	L	L	L

FLH 451 – 74 H183
FLH 455 – 84 H183

order numbers

FLH 451: Q67000–H495
FLH 455: Q67000–H511

Dual 1-Bit-Fulladder

The FLH 451/455 are a dual carry-save-fulladder for multiple-input-additions. They produce the true sum and carry for each bit.

Electrical characteristics
temperature ranges 1 and 5

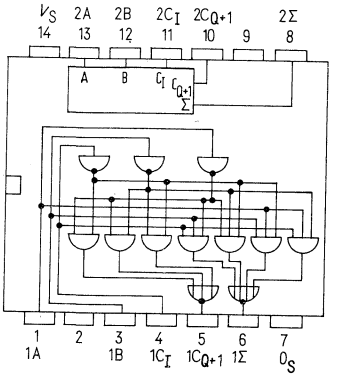
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, $-I_{QH}$=1 mA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IL}=0.8 V, I_{QL}=20 mA			0.4	V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			150	µA
	I_I	V_I=5.5 V | V_S=5.25 V			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			6	mA
Short circuit output current, each autput	$-I_Q$	V_S=5.25 V	40		100	mA
H-supply current	I_{SH}	V_S=5.25 V, V_{IH}=4.5 V		40		mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IL}=0 V		48	75	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PLH}	C_L=25 pF, R_L=280 Ω		10	15	ns
	t_{PHL}			12	18	ns

Logical data

Output load factor, H-signal, each output	F_{QH}				24	
L-signal	F_{QL}				12	
Input load factor, each input	F_I				3.75	



Pin configuration
top view

Truth table

inputs			outputs	
C_I	B	A	Σ	C_{Q+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

FLH 461 – 4934
FLH 465 – 49834
FLH 471 – 4935
FLH 475 – 49835

order numbers

FLH 461:	Q67000–H141
FLH 471:	Q67000–H142
FLH 465:	Q67000–H512
FLH 475:	Q67000–H513

FLH 461/465 Hexinverter with Expander Node and Open Collector Output

The inverters FLH 461/465 and FLH 471/475 have open-base-inputs. By means of fast switching diodes (e.g. BAY 61), the inverters can be expanded to n inputs. High input voltages may be applied if diodes with high breakdown voltages are used. Wired-AND-connections are possible with the FLH 471/475. Formulae and resistance tables see FLH 201.

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage*	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage*	V_{IL}	V_S=4.75 V			0.7	V
H-output voltage of FLH 471/475	V_{QH}	V_S=4.75 V, V_{IL}=0.7 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, I_{QL}=16 mA			0.4	V
H-output current of FLH 461/465, each output	I_{QH}	V_S=4.75 V, V_Q=5.5 V, V_{IL}=0.4 V			250	µA
L-input current	$-I_{IL}$	V_S=5.25 V, V_I=0 V			2	mA
Short circuit output current, FLH 471/475, each output	$-I_Q$	V_S=5.25 V, V_I=0.4 V	20		70	mA
H-supply current	I_{SH}	V_S=5.25 V, V_I=0 V		7.5	13	mA
L-supply current	I_{SL}	V_S=5.25 V, E = open		22.0	38	mA

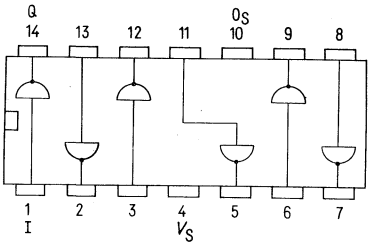
Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Propagation delay	t_{PHL}				40	ns
	t_{PLH}				40	ns

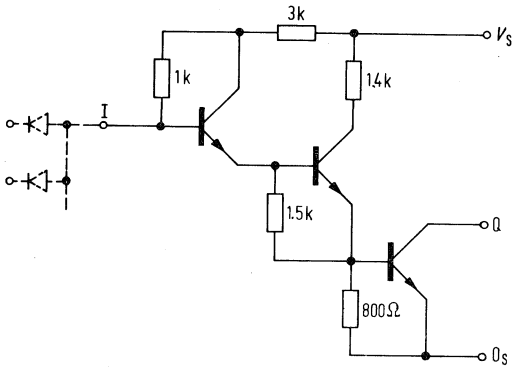
Logical data

Output load factor	F_Q				10	
Input load factor	F_{IL}				1.25	
	F_{IH}				depends on leakage current of external diodes	

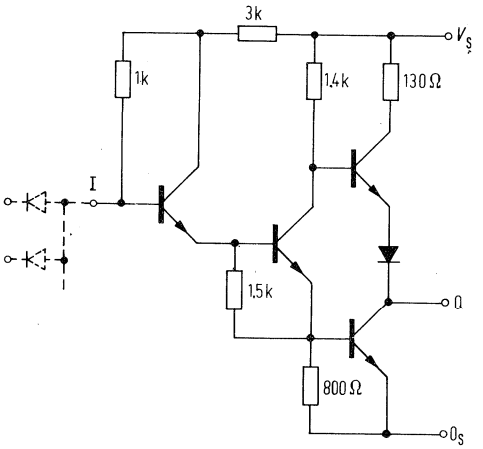
* with input diodes BAY 61



Pin configuration
top view



FLH 461/465
Schematic (each gate)



FLH 471/475
Schematic (each gate)

FLH 481 – 7406
FLH 485 – 8406
FLH 481 T – 7416
FLH 485 T – 8416

order numbers

FLH 481: Q67000–H396
FLH 481 T: Q67000–H400
FLH 485: Q67000–H440
FLH 485 T: Q67000–H443

Hexbuffer, Inverting with Open Collector Output

The buffer stages have open collector outputs with high breakdown voltages for high load currents
FLH 481/485: 30 V/40 mA
FLH 481/485 T: 15 V/30 mA.
The buffers can be used as level converters (e.g. TTL to MOS) or to drive small lamps and relais. Several outputs of a single package can be paralleled to increase the output load current.

Maximum ratings

		lower limit B	upper limit A	unit
H-output voltage FLH 481/485	V_{QH}	0	30	V
FLH 481 T/485 T	V_{QH}	0	15	V
L-output current	I_{QL}	0	40	mA

Electrical characteristics
temperature ranges 1 and 5

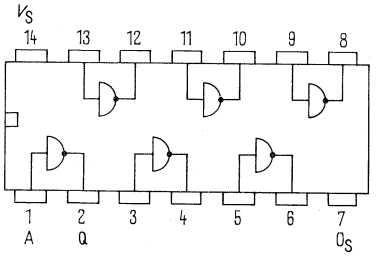
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	I_{QL}=16 mA | V_S=4.75 V			0.4	V
	V_{QL}	I_{QL}=40 mA | V_{IH}=2.0 V			0.7	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
each input	I_I	V_I=5.5 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
H-output current, each output	I_{QH}	V_S=4.75 V, V_{IL}=0.8 V, V_{QH}=V_{QHA}			250	µA
H-supply current	I_{SH}	V_S=5.25 V, V_{IL}=0 V		30	42	mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IH}=5.0 V		27	38	mA

Delay times, V_S=5 V, T_A=25 °C

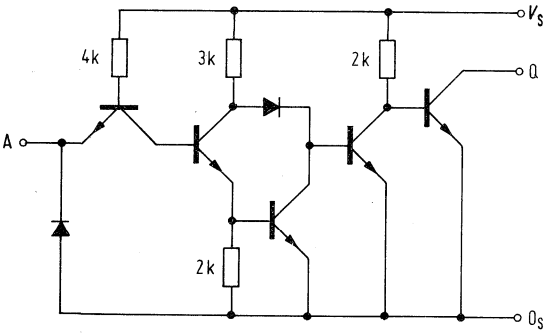
Propagation delay	t_{PLH}	C_L=15 pF		15	23	ns
	t_{PHL}	R_L=110 Ω		15	15	ns

Logical data

Output load factor	F_Q				10	
Input load factor	F_I				1	
Logic		Q=$\overline{A}$				



Pin configuration
top view



Schematic (each gate)

FLH 491 – 7407
FLH 495 – 8407
FLH 491 T – 7417
FLH 495 T – 8417

order numbers

FLH 491: Q67000–H397
FLH 491T: Q67000–H401
FLH 495: Q67000–H441
FLH 495T: Q67000–H444

Hexbuffer with Open Collector Output

The buffer stages have open collector outputs with high breakdown voltages for high load currents.
FLH 491/495: 30 V/40 mA
FLH 491/495T: 15 V/40 mA
The buffers can be used as level converters (e.g. TTL to MOS) or to drive small lamps and relais.
Several outputs of a single package can be paralleled to increase the output load current.
In addition the following maximum ratings apply:

Maximum ratings

		lower limit B	upper limit A	unit
H-output voltage FLH 491/495	V_{QH}	0	30	V
FLH 491T/495T	V_{QH}	0	15	V
L-output current	I_{QL}	0	40	mA

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	I_{QL}=16 mA | V_S=4.75 V			0.4	V
	V_{QL}	I_{QL}=40 mA | V_{IL}=0.8 V			0.7	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current,	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
each input	I_I	V_I=5.5 V			1.0	mA
L-input current,	$-I_{IL}$	V_S=5.25 V			1.6	mA
each input		V_{IL}=0.4 V				
H-output current,	I_{QH}	V_S=4.75 V, V_{IH}=2.0 V			250	µA
each output		V_{QH}=V_{QHA}				
H-supply current	I_{SH}	V_S=5.25 V		29	41	mA
		V_{IH}=5.0 V				
L-supply current	I_{SL}	V_S=5.25 V		21	30	mA
		V_{IL}=0 V				

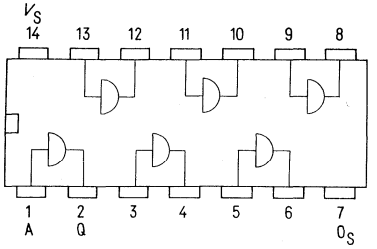
Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PLH}	C_L=15 pF		20	30	ns
	t_{PHL}	R_L=110 Ω		6	10	ns

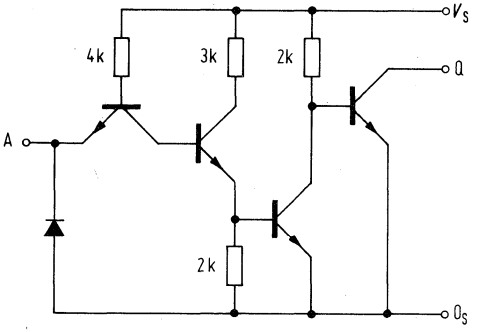
Logical data

Output load factor	F_Q			25
Input load factor	F_I			1

Logic Q=A



Pin configuration
top view



Schematic (each gate)

FLH 501 – 7412
FLH 505 – 8412

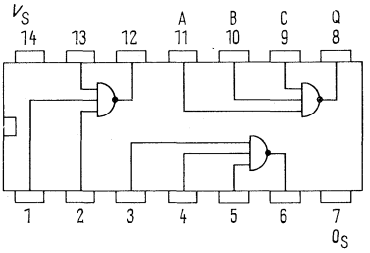
order numbers

FLH 501: Q67000–H526
FLH 505: Q67000–H527

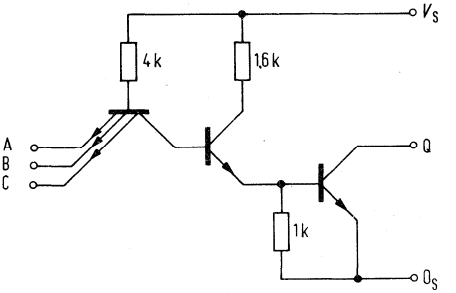
Triple 3-Input NAND-Gate with Open Collector Output

Formulae and resistance table for wired-AND-connections see FLH 201.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, I_{QL}=16 mA		0.22	0.4	V
DC-noise margin	V_{nm}		0.4	1.0		V
H-output current, each output	I_{QH}	V_S=4.75 V, V_Q=5.5 V, V_{IL}=0.4 V			250	µA
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
	I_I	V_I=5.5V			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IH}=5 V		9	16.5	mA
H-supply-current	I_{SH}	V_S=5.25 V, V_{IL}=0 V		3	6	mA
Delay times, V_S=5 V, T_A=25 °C						
Propagation delay	t_{PHL}	C_L=15 pF, R_L=400 Ω		7	15	ns
	t_{PLH}	C_L=15 pF, R_L=4 kΩ		35	45	ns
Logical data						
Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	
Logic		$Q=\overline{A\,B\,C}$				



Pin configuration
top view



Schematic
(each gate)

order numbers

FLH 511: Q67000–H497
FLH 515: Q67000–H518
FLH 521: Q67000–H489
FLH 525: Q67000–H519

FLH 511 – 7423
FLH 515 – 8423
FLH 521 – 7425
FLH 525 – 8425

Dual 4-Input NOR-Gate with Strobe and Expander Node

FLH 511, FLH 515 with expander nodes N_1 and N_2.
FLY 101, FLY 105 corresponding expander.
FLH 521, FLH 525 without expander nodes (pins 1 and 2 must not be connected).

Electrical characteristics
temperature ranges 1 and 5
pins 1 and 2 open

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
Input clamping voltage	$-V_I$	V_S=4.75 V, $-I_I$=12 mA			1.5	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IL}=0.8 V, $-I_{QH}$=800 µA	2.4	3.3		
L-output voltage	V_{QL}	V_S=4.75 V, V_{IL}=2.0 V, I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current at A, B, C, D	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
at strobe	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			160	µA
Input current	I_I	V_I=5.5 V			1.0	mA
L-input current at A, B, C, D	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
at strobe	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			6.4	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	20		55	mA
H-supply current	I_{SH}	V_S=5.25 V, V_{IL}=0 V		8	16	mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IH}=5.0 V		10	19	mA

Delay times, V_S=5 V, T_A=25 °C, pins 11 and 12 open

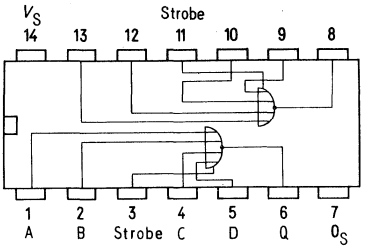
Propagation delay	t_{PHL}	C_L=15 pF, R_L=400 Ω		8	15	ns
	t_{PLH}			13	22	Ts

Electrical characteristics of the nodes N_1 and N_2 see AND/OR-gate FLH 151/155

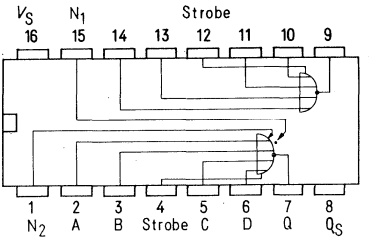
Note: Nodes N_1 and N_2 are used simultaneously for expansion.
If N_1 and N_2 are unused, they must not be connected or tied together.
Up to 4 FLY 101 and FLY 105 resp. may be connected to one FLH 511 and FLH 515 resp.

FLH 511
FLH 515
FLH 521
FLH 525

FLH 511, FLH 515

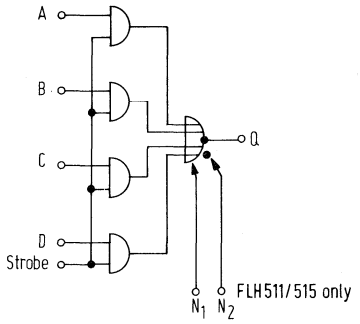


FLH 521, FLH 525



Pin configurations, top view

Block diagram (each gate)



Truth table

inputs					outputs
A	B	C	D	Strobe	Q
X	H	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	L	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

X = L- or H-signal

Logical data

		upper limit A
Output load factor, H-signal	F_{OH}	20
each output L-signal	F_{OL}	10
Input load factor at A, B, C, D	F_I	1
at strobe	F_I	4

Logic FLH 511/515: $Q = \overline{\text{strobe} + A + B + C + D + \text{exp.}}$

FLH 521/525: $Q = \overline{\text{strobe} + A + B + C + D}$

order numbers

FLH 531: Q67000–H416
FLH 535: Q67000–H520
FLH 541: Q67000–H493
FLH 545: Q67000–H521

FLH 531 – 7437
FLH 535 – 8437
FLH 541 – 7438
FLH 545 – 8438

Quadruple 2-Input NAND-Powergate

FLH 531/535 quadruple 2-input NAND-gate with Darlington output.
FLH 541/545 quadruple 2-input NAND-gate with open collector output for wired-AND-connections.
Fomulae and resistance table see FLH 201.

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage at FLH 531/535	V_{QH}	V_S=4.75 V, V_{IL}=0.8 V $-I_{QH}$=1.2 mA	2.4			V
H-output current each output of FLH 541/545	I_{QH}	V_S=4.75 V, V_{IL}=0.8 V, V_{QH}=5.5 V			250	µA
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, I_{QL}=48 mA		0.22	0.4	V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
	I_I	V_I=5.5 V | V_S=5.25 V			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output of FLH 531/535	$-I_Q$	V_S=5.25 V, V_{IL}=0 V	20		70	mA
H-supply current	I_{SH}	V_S=5.25 V, V_{IL}=0 V		9	15.5	mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IH}=5 V		34	54	mA

Delay times, V_S=5 V, T_A=25 °C

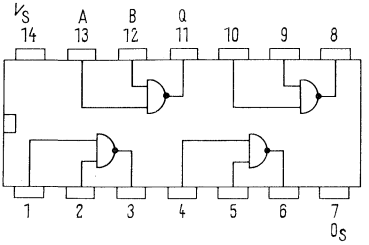
Propagation delay	t_{PLH}	C_L=15 pF, R_L=133 Ω		13	22	ns
of FLH 531/535	t_{PHL}			8	15	ns
Propagation delay	t_{PLH}			14	22	ns
of FLH 541/545	t_{PHL}			11	18	ns

Logical data

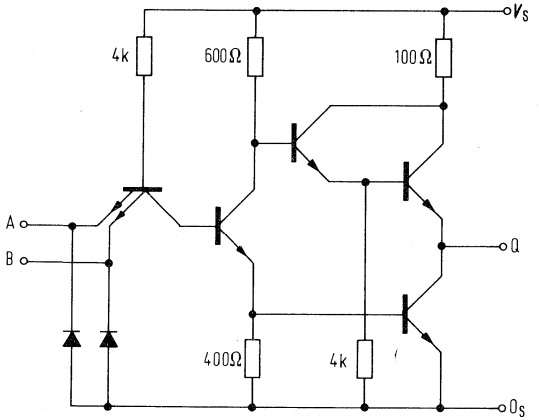
Output load factor, each output	F_Q				30	
Input load factor, each input	F_I				1	

Logic $Q=\overline{AB}$

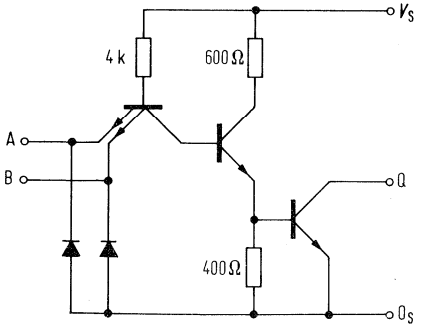
FLH 531
FLH 535
FLH 541
FLH 545



Pin configuration
top view



FLH 531, FLH 535
Schematic (each gate)



FLH 541, FLH 545
Schematic (each gate)

order numbers

FLH 551: Q67000–L12
FLH 555: Q67000–H448

FLH 551 – 7448
FLH 555 – 8448

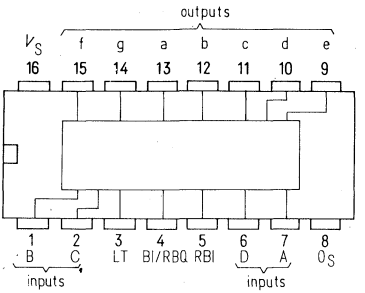
BCD-7-Segment-Decoder

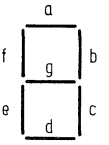
The FLH 551/555 transform BCD-words with 4 bits present at the inputs A, B, C, D into the 7-segment-code. The passive outputs a, b, c, d, e, f, g supply TTL active high data. Control functions are provided by means of three auxiliary inputs (BI, RBI, LT).
An L-signal at the ripple-blanking-input RBI suppresses the O-signal at the outputs.
When the blanking-input BI is supplied with an L-signal, all outputs assume an L-state. The ripple-blanking-output RBQ (internally connected with BI) provides an automatic O-suppression over several decades. An L-signal at the lamp-test-input LT forces all segment outputs into H-state.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage of the outputs a to g	V_{QL}	V_S=4.75 V, I_{QL}=6.4 mA		0.27	0.4	V
L-output voltage at output BI/RBQ	V_{QL}	V_S=4.75 V, I_{QL}=8 mA		0.3	0.4	V
H-output voltage of the outputs a to g	V_{QH}	V_S=5.25 V, $-I_{QH}$=400 µA	2.4	4.2		V
H-output voltage at output BI/RBQ	V_{QH}	V_S=4.75 V, $-I_{QH}$=200 µA	2.4	3.7		V
L-input current at input BI/RBQ	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			4.2	mA
L-input current at remaining inputs	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
H-input current at input BI/RBQ	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			104	µA
H-input current at remaining inputs	I_{IH}	V_{IH}=2.4 V | V_S=5.25 V			40	µA
	I_I	V_I=5.5 V			1	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V			4	mA
Supply current	I_S	V_S=5.25 V, outputs open		53	90	mA
Delay times, V_S=5 V, T_A=25 °C						
Propagation delay						
Input A to any output	t_{PLH}	C_L=15 pF, R_L=667 Ω			100	ns
	t_{PHL}				100	ns
From RBI to any output	t_{PLH}				100	ns
	t_{PHL}				100	ns
Logical data						
Output load factor at						
Output BI/RBQ	F_Q				5	
Outputs a to g H-signal	F_{QH}				10	
L-signal	F_{QL}				4	
Input load factor at						
Input BI/RBQ	F_I				2.6	
remaining inputs	F_I				1	

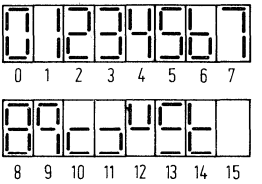
FLH 551
FLH 555

Pin configuration, top view





Segment identification



Output patterns

Truth table

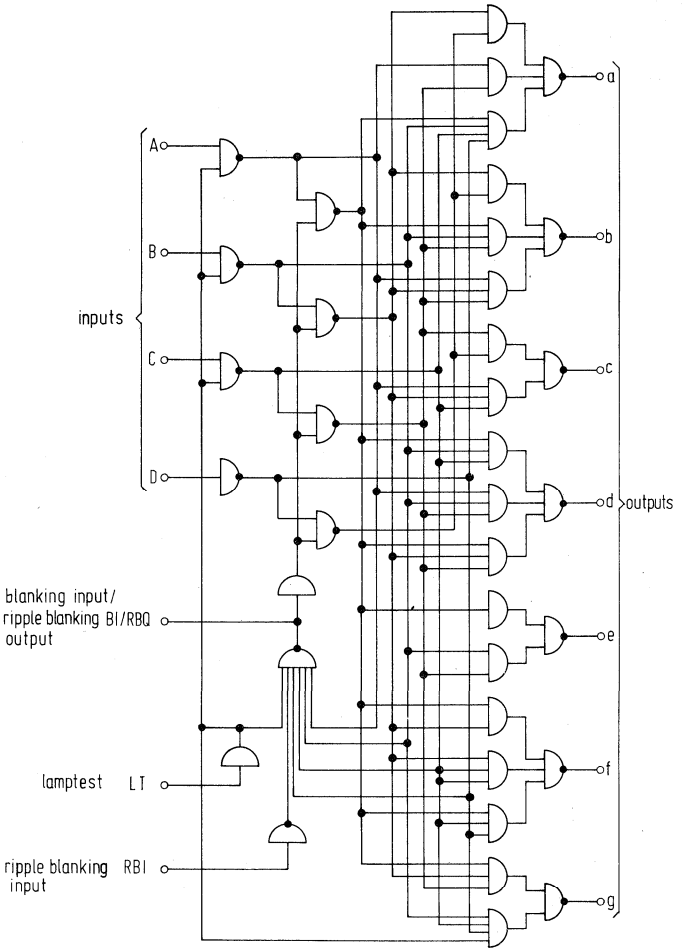
function	LT	RBI	D	C	B	A	BI/ RBQ	a	b	c	d	e	f	g
0[1]	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H
12	H	X	H	H	L	L	H	L	H	L	L	H	H	H
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L
BI[2]	X	X	X	X	X	X	L	L	L	L	L	L	L	L
RBI[3]	H	L	L	L	L	L	L	L	L	L	L	L	L	L
LT[4]	L	X	X	X	X	X	H	H	H	H	H	H	H	H

Notes:

X=H or L-signal

1) If 0-indication is desired, RBI must be supplied with an H-signal.
2) An L-signal at BI forces all segment outputs into L-state independent of the other input conditions.
3) If an L-signal is supplied to RBI and A, B, C, D, L-signals result at all outputs and RBQ (zero-condition).
4) An L-signal at LT switches all outputs to H only if BI/RBQ is supplied with an H signal regardless of the input condition at A, B, C, D, and RBI.

Block diagram



FLJ 101 – 7470
FLJ 105 – 8470

order numbers

FLJ 101: Q67000–J1
FLJ 105: Q67000–J80

3+3-Input JK-Flipflop

Supply voltage	V_S	typ. 5 V
L-output voltage	V_{QL}	typ. 0.23 V
H-output voltage	V_{QH}	typ. 3.30 V
DC noise margin	V_{nm}	typ. 1.0 V
Average supply current	I_S	typ. 13 mA
Output load factor	F_Q	upper limit 10
Average propagation delay	t_P	typ. 23 ns

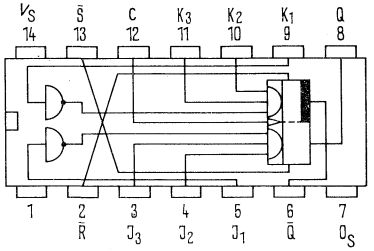
Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Notes

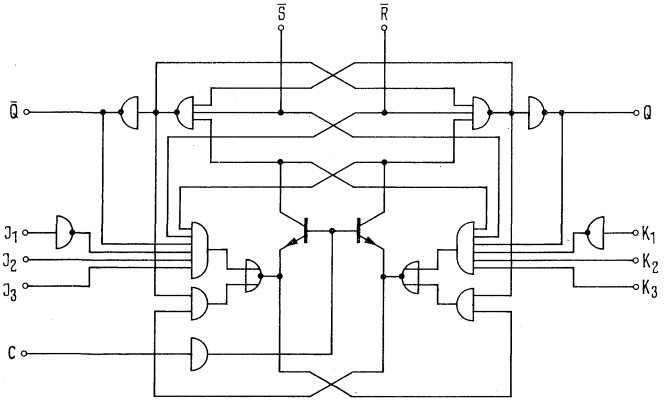
$J = \overline{J_1} \wedge J_2 \wedge J_3$
$K = \overline{K_1} \wedge K_2 \wedge K_3$
t_n = bit time before clock pulse
t_{n+1} = bit time after block pulse

For development recommended: **FLJ 341**



Pin configuration
top view

Block diagram



$\bar{S}$ = set input, $\bar{R}$ = reset input, C = clock input

FLJ 111 – 7472
FLJ 115 – 8472

order numbers

FLJ 111: Q67000–J2
FLJ 115: Q67000–J81

3+3-Input JK-Master-Slave-Flipflop

Electrical characteristics
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75	24	2.0			V
L-input voltage	V_{IL}	V_S=4.75				0.8	V
H-output voltage	V_{QH}	$-I_{QH}$=400 µA, V_S=4.75 V	24	2.4	3.5		V
L-output voltage	V_{QL}	I_{QL}=16 mA, V_S=4.75 V	24		0.22	0.4	V
DC noise margin	V_{nm}		24	0.4	1.0		V
H-input current at J1, J2, J3, K1, K2, K3	I_{IH}	V_{IH}=2.4 V	25			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V	25			1	mA
H-input current at R̄, S̄, or C	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V	25			80	µA
	I_I	V_I=5.5 V, V_S=5.25 V	25			1	mA
L-input current at J1, J2, J3, K1, K2, K3	$-I_{IL}$		26			1.6	mA
		V_S=5.25 V				3.2	mA
L-input current at S̄, R̄ or C	$-I_{IL}$	V_{IL}=0.4 V	26			3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_I=0 V	27	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=5 V	25		10	20	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{pC}			20			ns
Set pulse duration	t_{pS}			25			ns
Reset pulse duration	t_{pR}			25			ns
Setup time	t_S		29	t_{pT}			
Hold time	t_H			0			
Maximum clock frequency	f		29	15	20		MHz
Propagation delay from C to Q	t_{PHL}	C_1=15 pF, F_Q=10	29	10	25	40	ns
	t_{PLH}		29	10	16	25	ns
Propagation delay from R̄ or S̄ to Q	t_{PHL}		30		25	40	ns
	t_{PLH}		30		16	25	ns

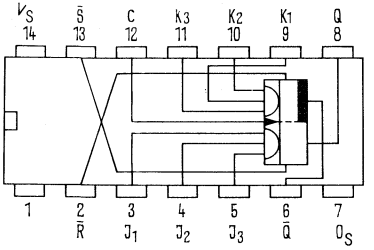
Logical data

Output load factor, each output	F_Q		10
Input load factor at J_1, J_2, J_3, K_1, K_2 or K_3	F_I		1
Input load factor at R̄, S̄ or C	F_I		2

For development recommendet: **FLJ 341**

FLJ 111
FLJ 115

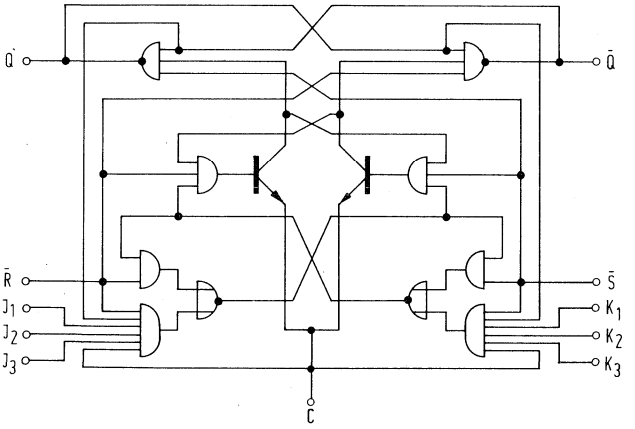
Pin configuration, top view



Clock pulse

(1) isolate slave from master
(2) enter signal from J and K into master
(3) disable inputs J and K
(4) transfer information from master to slave

Block diagram



$\bar{R}$ = reset input, $\bar{S}$ = set input, C = clock input

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

$J = J_1 \wedge J_2 \wedge J_3$
$K = K_1 \wedge K_2 \wedge K_3$
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at $\bar{R}$ sets Q to L – L-level at $\bar{S}$ sets Q to H – $\bar{R}$ and $\bar{S}$ operate independent of C.

FLJ 121 – 7473
FLJ 125 – 8473

order numbers

FLJ 121: Q67000–J3
FLJ 125: Q67000–J79

Dual JK-Master-Slave-Flipflop with Reset

Electrical characteristcs temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	24	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V				0.8	V
H-output voltage	V_{QH}	$-I_{QH}$=400 µA, V_S=4.75 V	24	2.4	3.5		V
L-output voltage	V_{QL}	I_{QL}=16 mA, V_S=4.75 V	24		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V, V_S=5.25 V	25			1	mA
H-input current at J or K	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V	25			40	µA
at R or T	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V	25			80	µA
L-input current at J or K	$-I_{IL}$	V_{IL}=0.4 V	26			1.6	mA
at $\overline{R}$ or C	$-I_{IL}$	V_{IL}=0.4 V	26			3.2	mA
Short circuit output current, each output	$-I_{QH}$	V_S=5.25 V, V_I=0 V	28	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=5 V	25		20	40	mA

Delay times, V_S=5 V, T_A=25 °C

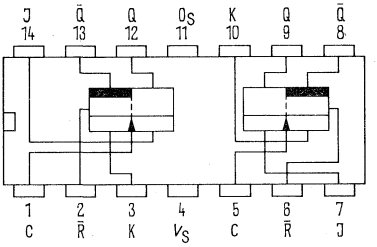
Clock pulse duration	t_{pC}			20			ns
Reset pulse duration	t_{pR}			25			ns
Setup time	t_S		29	t_{pT}			
Hold time	t_H			0			
Maximum clock frequency	f		29	15	20		MHz
Propagation delay from	t_{PHL}		29	10	25	40	ns
C to Q	t_{PLH}	C_1=15 pF, F_Q=10	29	10	16	25	ns
Propagation delay from	t_{PHL}		30		25	40	ns
$\overline{R}$ to Q	t_{PLH}		30		16	25	ns

Logical data

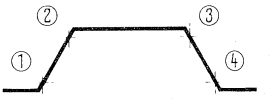
Output load factor, each output	F_Q		10
Input load factor			
at J or K	F_I		1
at $\overline{R}$ or C	F_I		2

For development recommended: **FLJ 521**

Pin configuration, top view

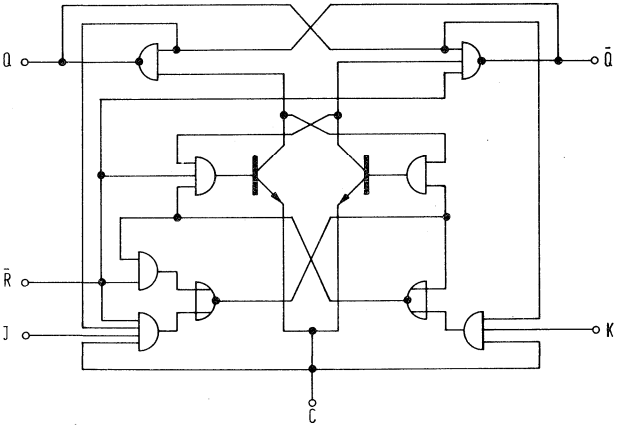


Clock pulse



(1) isolate slave from master
(2) enter signal from J and K into master
(3) disable inputs J and K
(4) transfer information from master to slave

Block diagram (one flipflop)



R̄ = Reset input, C = clock input

Truth table
(each flipflop)

t_n		t_{n+1}
J	K	Q
L	L	Q
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at R̄ sets Q to L – R̄ operates independent of C.

FLJ 131 – 7476
FLJ 135 – 8476

order number

FLJ 131: Q67000–J4
FLJ 135: Q67000–J82

Dual JK-Master-Slave-Flipflop with Set and Reset

Electrical characteristics temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	24	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V				0.8	V
Iutput voltage	V_{QH}	$-I_{QH}$=400 µA, V_S=	24	2.4	3.5		V
L-output voltage	V_{QL}	I_{QL}=16 mA, 4.75 V	24		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V, V_S= 5.25 V	25			1	mA
H-input current at J or K	I_{IH}	V_{IH}=2.4 V, V_S= 5.25 V	25			80	µA
at $\overline{R}$, $\overline{S}$ or C	I_{IH}	V_{IH}=2.4 V, V_S= 5.25 V	25			40	µA
L-input current at J or K,	$-I_{IL}$	V_{IL}=0.4 V, V_S= 5.25 V	26			1.6	mA
at $\overline{R}$, $\overline{S}$ or C	$-I_{IL}$	V_{IL}=0.4 V, V_S= 5.25 V	26			3.2	mA
Short circuit output current, each output	$-I_{QH}$	V_S=5.25 V, V_I=0 V	27	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=5.0 V	25		20	40	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{pC}			20			ns
Set pulse duration	t_{pS}			25			ns
Reset pulse duration	t_{pR}			25			ns
Setup time	t_S		29	t_{pT}			
Hold time	t_H			0			
Maximum clock frequency	f		29	50	20		MHz
Propagation delay from	t_{PHL}		29	10	25	40	ns
C to Q	t_{PLH}	C_1=15 pF, F_Q=10	29	10	16	25	ns
Propagation delay from	t_{PHL}		30		25	40	ns
$\overline{R}$ or $\overline{S}$ to Q	t_{PLH}		30		16	25	ns

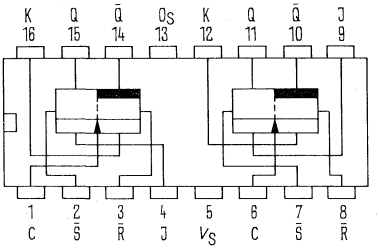
Logical data

Output load factor, each output	F_Q		10
Input load factor			
at J or K	F_I		1
at $\overline{R}$, $\overline{S}$ or C	F_I		2

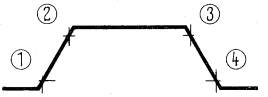
For development recommended: **FLJ 351**

FLJ 131
FLJ 135

Pin configuration, top view

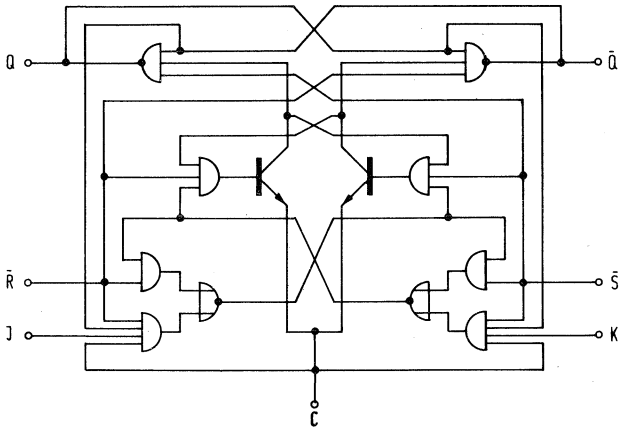


Clock pulse



(1) isolate slave from master
(2) enter signal from J and K into master
(3) disable inputs J and K
(4) transfer information from master to slave

Block diagram (one flipflop)



R̄ = rest input, S̄ = set input, C = clock input

Truth table
(each flipflop)

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at R̄ sets Q to L – L-level at S̄ sets Q to H – R̄ and S̄ operate independent of C.

FLJ 141 – 7474
FLJ 145 – 8474

order numbers

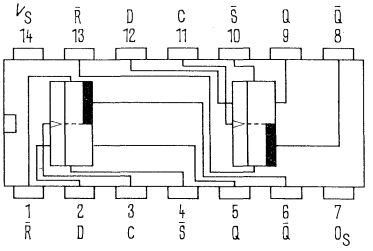
FLJ 141: Q67000–J9
FLJ 145: Q67000–J83

Dual D-Flipflop

The FLJ 141/145 have independent set and reset inputs. The information present at the D-input is transferred to the Q-output at the rising edge of the clock pulse as soon as the threshold voltage of the input transistor is reached. Afterwards the D-input is disabled again.

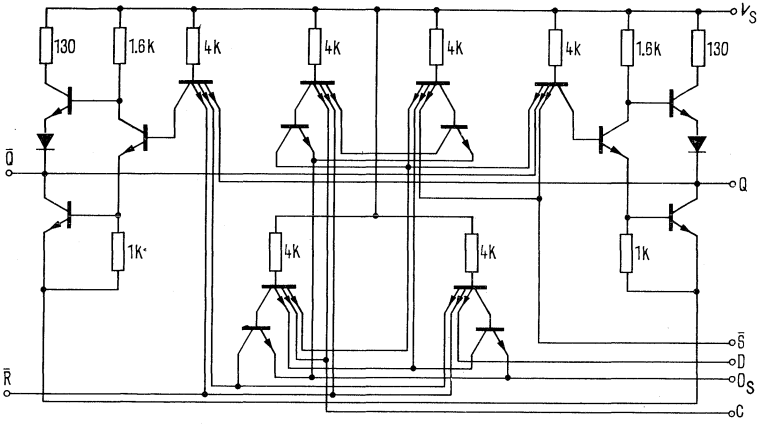
Electrical characteristics temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	31	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V				0.8	V
H-output voltage	V_{QH}	$-I_{QH}$=400 µA, V_S=	31	2.4	3.5		V
L-output voltage	V_{QL}	I_{QL}=16 mA, 4.75 V	31		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V, V_S=	32			1	mA
H-input current at D	I_{IH}	V_{IH}=2.4 V, V_S=	32			40	µA
at $\overline{S}$ or C	I_{IH}	V_{IH}=2.4 V, V_S=	32			80	mA
at $\overline{R}$	I_{IH}	V_{IH}=2.4 V, V_S= 5.25 V	32			120	µA
L-input current at D or $\overline{S}$	$-I_{IL}$	V_S=5.25 V	33			1.6	mA
at $\overline{R}$ or C	$-I_{IL}$	V_S=5.25 V	33			3.2	mA
at $\overline{R}$	$-I_{IL}$	V_{IL}=0.4 V	33			4.8	mA
Short circuit output current, each output	$-I_{QH}$	V_S=5.25 V, V_I=0 V	34	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=5 V	32		17	30	mA
Delay times, V_S=5 V, T_A=25 °C							
Clock pulse duration	t_{pC}			30			ns
Set pulse duration	t_{pS}			30			ns
Reset pulse duration	t_{pR}			30			ns
Maximum clock frequency	f		30a	15	25		MHz
Minimal setup time	t_S		30a		15	20	ns
Minimal hold time	t_H		30a		2	5	ns
Propagation delay from $\overline{R}$ or $\overline{S}$ to output	t_{PHL}	C_1=15 pF, F_Q=10	30			40	ns
from C to output	t_{PHL}	C_1=15 pF, F_Q=10	30a	10	20	40	ns
Propagation delay $\overline{R}$ or $\overline{S}$ from output	t_{PLH}		30			25	ns
from C to output	t_{PLH}		30a	10	14	25	ns
Logical data							
Output load factor, each output	F_Q					10	
Input load factor at D	F_I					1	
Input load factor at $\overline{S}$ or C	F_I					2	
Input load factor at $\overline{R}$	F_I					3	

FLJ 141
FLJ 145



Pin configuration
top view

Schematic (each flipflop)



D = data input, $\bar{R}$ = reset input, $\bar{S}$ = set input, C = clock input

Truth table
(each flipflop)

t_n	t_{n+1}	
D	Q	$\bar{Q}$
L	L	H
H	H	L

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at $\bar{R}$ sets Q to L – L-level at $\bar{S}$ sets Q to H – $\bar{R}$ and $\bar{S}$ operate independent of C.

FLJ 151 – 7475
FLJ 155 – 8475

order numbers

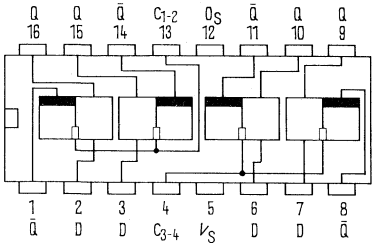
FLJ 151: Q67000–J5
FLJ 155: Q67000–J84

Quadruple D-Flipflop

The flipflops of the FLJ 151/155 have two stable states which are controlled by the clock. Any information present at the data-inputs D is transferred to the Q-outputs when the clock is at H-level. If the clock is at L-level, the D-input is disabled.

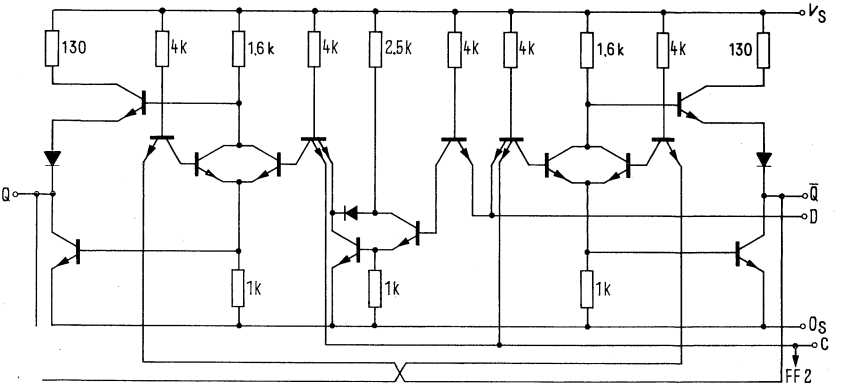
Electrical characteristics temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	36	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	37			0.8	V
H-output voltage	V_{QH}	$-I_{QH}$=400 µA | V_S=	36, 37	2.4			V
L-output voltage	V_{QL}	I_{QL}=16 mA | 4.75 V	36, 37			0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V | V_S	38			1.0	mA
H-input current at D	I_{IH}	V_{IH}=2.4 V | =5.25 V	38			80	µA
at C	I_{IH}	V_{IH}=2.4 V	38			160	µA
L-input current at D,	$-I_{IL}$	V_S=5.25 V	38			3.2	mA
at C	$-I_{IL}$	V_{IL}=0.4 V	38			6.4	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_I=0 V	39	57		18	mA
Supply current	I_S	V_S=5.25 V	40		32	53	mA
Delay times, V_S=5 V, T_A=25 °C							
H-setup time at D	t_{SH}				7	20	ns
L-setup time at D	t_{SL}				14	20	ns
Hold time	t_H			0	15		ns
Propagation delay from input D to output Q	t_{PHL}				14	25	ns
from input D to output $\overline{Q}$	t_{PHL}	C_1=15 pF, R_L=400 Ω			7	15	ns
from clock input C to output Q	t_{PHL}	C_1=15 pF, R_L=400 Ω			7	15	ns
from clock input C to output $\overline{Q}$	t_{PHL}				7	15	ns
Propagation delay from input D to output Q	t_{PLH}				16	30	ns
from input D to output $\overline{Q}$	t_{PLH}	C_1=15 pF, R_L=400 Ω			24	40	ns
from clock input C to output Q	t_{PLH}	C_1=15 pF, R_L=400 Ω			16	30	ns
from clock input C to output $\overline{Q}$	t_{PLH}				16	30	ns
Logical data							
Output load factor, each output	F_Q					10	
Input load factor at D	F_I					2	
Input load factor at C	F_I					4	

FLJ 151
FLJ 155



Pin configuration
top view

Schematic (each flipflop)



D = data input, C = clock input

Truth table
(each flipflop)

t_n	t_{n+1}	
D	Q	Q̄
H	H	L
L	L	H

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

FLJ 161 – 7490
FLJ 165 – 8490
FLJ 161 S – 7490S1
FLJ 165 S – 8490S1

order numbers

FLJ 161: Q67000–J10
FLJ 165: Q67000–J85
FLJ 161S: Q67000–J248
FLJ 165S: Q67000–J249

Decimal Counter

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	$-I_{QH}$ =400 µA; V_S =4.75 V	2.4			V
L-output voltage	V_{QL}	I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V			1	mA
H-input current at R_{01}, R_{02}, R_{91}, R_{92}	I_{IH}	V_{IH}=2.4 V; V_S =5.25 V			40	µA
H-input current at A	I_{IH}	V_{IH}=2.4 V; V_S =5.25 V			80	µA
H-input current at B	I_{IH}	V_{IH}=2.4 V; V_S =5.25 V			160	µA
L-input current at R_{01}, R_{02}, R_{91}, R_{92}	$-I_{IL}$	V_S=5.25 V			1.6	mA
L-input current at A	$-I_{IL}$	V_{IL}=0.4 V			3.2	mA
L-input current at B	$-I_{IL}$	V_{IL}=0.4 V			6.4	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V; V_I=0 V	18		57	mA
Supply current	I_S	V_S=5.25 V; V_I=4.5 V		32	53	mA

Delay times, V_S=5 V, T_A=25 °C

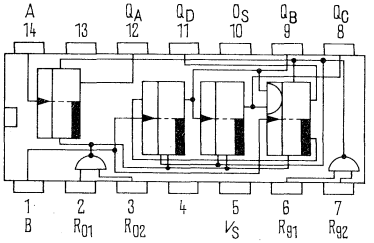
Clock pulse duration	t_{pC}		50			ns
Reset pulse duration	t_{pR}		50			ns
Maximum clock frequency	f	C_1=15 pF; R_L=400 Ω	10	18		MHz
Propagation delay from	t_{PHL}	C_1=15 pF; R_L=400 Ω		60	100	ns
A to Q_D	t_{PLH}	C_1=15 pF; R_L=400 Ω		60	100	ns

Logical data

Output load factor, each output	F_Q		10	
Input load factor, each R_{01}, R_{02}, R_{91} or R_{92}	F_I		1	
Input load factor at A	F_I		2	
Input load factor at B	F_I		4	

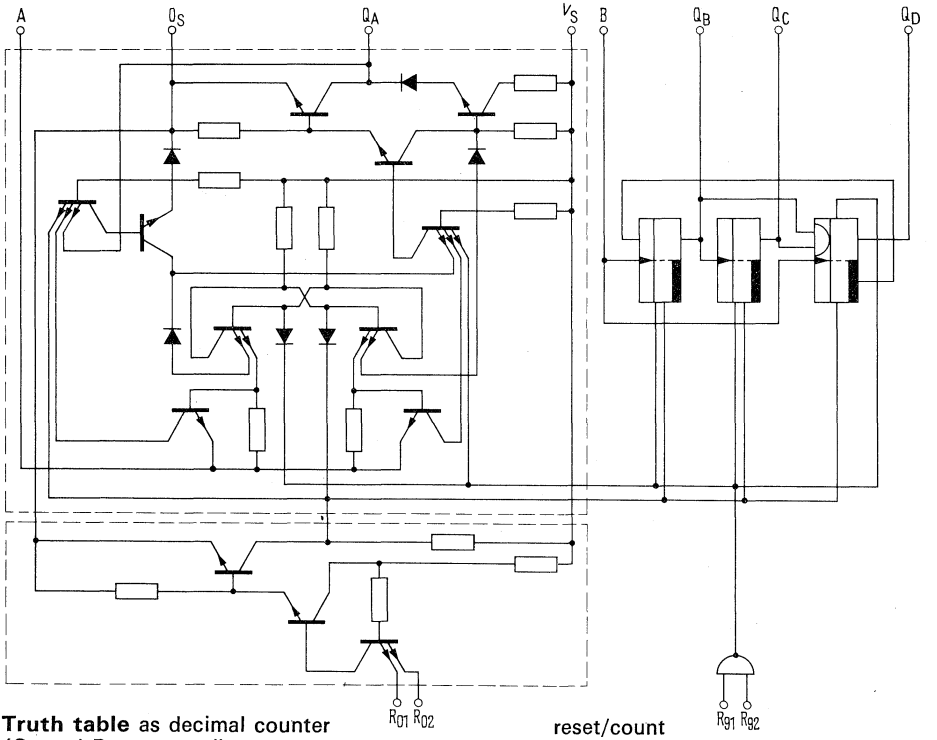
FLJ 161/165S: as FLJ 161/165, however maximum clock frequency 25 MHz

FLJ 161
FLJ 165



Pin configuration
top view

Schematic
A, B = clock input
R_{01}–R_{02} = reset inputs



Truth table as decimal counter
(Q_A and B connected)

sequence	0	1	2	3	4	5	6	7	8	9
Q_A	L	H	L	H	L	H	L	H	L	H
outputs Q_B	L	L	H	H	L	L	H	H	L	L
Q_C	L	L	L	L	H	H	H	H	L	L
Q_D	L	L	L	L	L	L	L	L	H	H

reset/count
(X = H or L-signal)

reset inputs R_{01}	R_{02}	R_{91}	R_{92}	outputs Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	count			
L	X	L	X	count			
L	X	X	L	count			
X	L	L	X	count			

FLJ 171 – 7492
FLJ 175 – 8492

order numbers

FLJ 171: Q67000–J33
FLJ 175: Q67000–J122

Divide-by-Twelve-Counter

The FLJ 171/175 contain a divide-by-two and a divide-by-six counter. When used as a divide-by-twelve-counter, Q_A and B have to be connected.

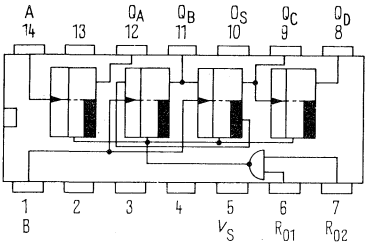
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V, V_S= 5.25 V			1	mA
H-input current at R_{01} or R_{02}	I_{IH}	V_{IH}=2.4 V, V_S= 5.25 V			40	µA
H-input current at A	I_{IH}	V_{IH}=2.4 V, V_S= 5.25 V			80	µA
H-input current at B	I_{IH}	V_{IH}=2.4 V, V_S= 5.25 V			160	µA
L-input current at R_{01}, R_{02}	$-I_{QL}$	V_S=5.25 V			1.6	mA
L-input current at A	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
L-input current B	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			6.4	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_Q=0 V	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=4.5 V		31	51	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{pC}		50			ns
Reset pulse duration	t_{pR}		50			ns
Maximum clock frequency	f	C_1=15 pF, R_L=400 Ω	10	18		MHz
Propagation delay from A to Q_D	t_{PHL}	C_1=15 pF, R_L=400 Ω		60	100	ns
	t_{PLH}	C_1=15 pF, R_L=400 Ω		60	100	ns

Logical data

Output load fctor, each output	F_Q				10	
Input load factor R_{01}, R_{02}	F_I				1	
Input load factor at A	F_I				2	
Input load factor at B	F_I				4	



Pin configuration
top view

Truth table

sequence	outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Notes:
Q_1 connected with B
To set all outputs to L, R_{01} and R_{02} must be supplied with an H-signal.

FLJ 181 – 7493
FLJ 185 – 8493

order numbers

FLJ 181: Q67000–J34
FLJ 185: Q67000–J123

4-Bit-Binary-Counter

The FLJ 181/185 contain a divide-by-two and a divide-by-eight counter. When used as a binary-counter, Q_A and B have to be connected.

Electrical characteristics
temperature ranges 1 and 5

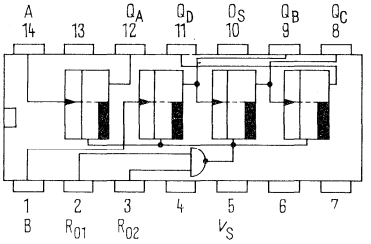
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{IH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
Input current, each input	I_I	V_I=5.5 V; V_S=5.25 V			1	mA
H-input current at R_{01} or R_{02}, at A or B	I_{IH}	V_{IH}=2.4 V; V_S=5.25 V			40	µA
	I_{IH}	V_{IH}=2.4 V; V_S=5.25 V			80	µA
L-input current at R_{01}, R_{02}	$-I_{IL}$	V_S=5.25 V			1.6	mA
at A or B	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_I=0 V	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=4.5 V		32	53	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{PC}		50			ns
Reset pulse duration	t_{PR}		50			ns
Maximum clock frequency	f	C_1=15 pF, R_L=400 Ω	10	18		MHz
Propagation delay from	t_{PHL}			75	135	ns
A to Q_D	t_{PLH}			75	135	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor at R_{01}, R_{02}	F_I				1	
at A or B	F_I				2	



Pin configuration
top view

Truth table

sequence	outputs			
	Q_4	Q_3	Q_2	Q_1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes:
Q_1 connected with B.
To reset all outputs to L, R_{01} and R_{02} must be supplied with an H-signal.

FLJ 191 – 7495 A
FLJ 195 – 8495 A

order numbers

FLJ 191: Q67000–J36
FLJ 195: Q67000–J256

4-Bit-Shiftregister, Reversible

The FLJ 191/195 have the following operating modes:
Right-shift-operation as serial register: mode control MC=L. Clock pulse at input C_1. Inputs A, B, C, D and C_2 are disabled.
Left-shift-operation: mode control MC=H. Clock pulse at C_2. Inputs SI and C_1 are disabled.
The registers are set to their initial condition by means of the parallel inputs A, B, C, D. For serial operation the following connections must be made:
Q_D with C, Q_B with B, and Q_C with A. D becomes the serial input.
Applications: serial-parallel and parallel-serial-converter, storage element.

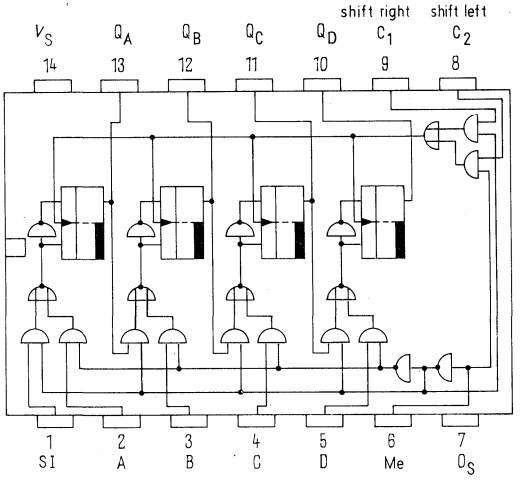
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current at A, B, C, D, and serial input SI	I_{IH}	V_{IH}=2.4 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1	mA
H-input current at mode control MC	I_{IH}	V_{IH}=2.4 V			80	µA
	I_I	V_I=5.5 V			1	mA
L-input current at A, B, C, D, and serial input SI	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
L-input current at mode control MC	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		50	85	mA

Logical data

Output load factor, each output	F_Q				10	
Input load factor at mode control MC	F_I				2	
Input load factor of the remaining inputs	F_I				1	

Delay times
V_S=5 V, T_A=25 °C

		test condition	lower limit B	typ.	upper limit A	unit
Clock pulse duration	t_{pC}		15	10		ns
Setup time	t_S		10			ns
at A, B, C, D, and SI						
Hold time	t_H		0			ns
at A, B, C, D and SI						
L-setup time at MC						
a) Shift right	t_{SLr}		15			ns
b) Shift left	t_{SLl}		5			ns
H-setup time at MC						
a) Shift right	t_{SHr}		5			ns
b) Shift left	t_{SHl}		15			ns
Maximum clock frequency	f	C_L=15 pF	25	36		MHz
Propagation delay from	t_{PHL}	R_L=400 Ω		18	27	ns
C to Q	t_{PLH}			21	32	ns



Pin configuration
top view

FLJ 201 – 74190
FLJ 205 – 84190

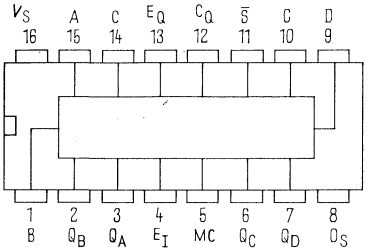
order numbers

FLJ 201: Q67000–J144
FLJ 205: Q67000–J198

Decimal Counter, Reversible with Set and Reset

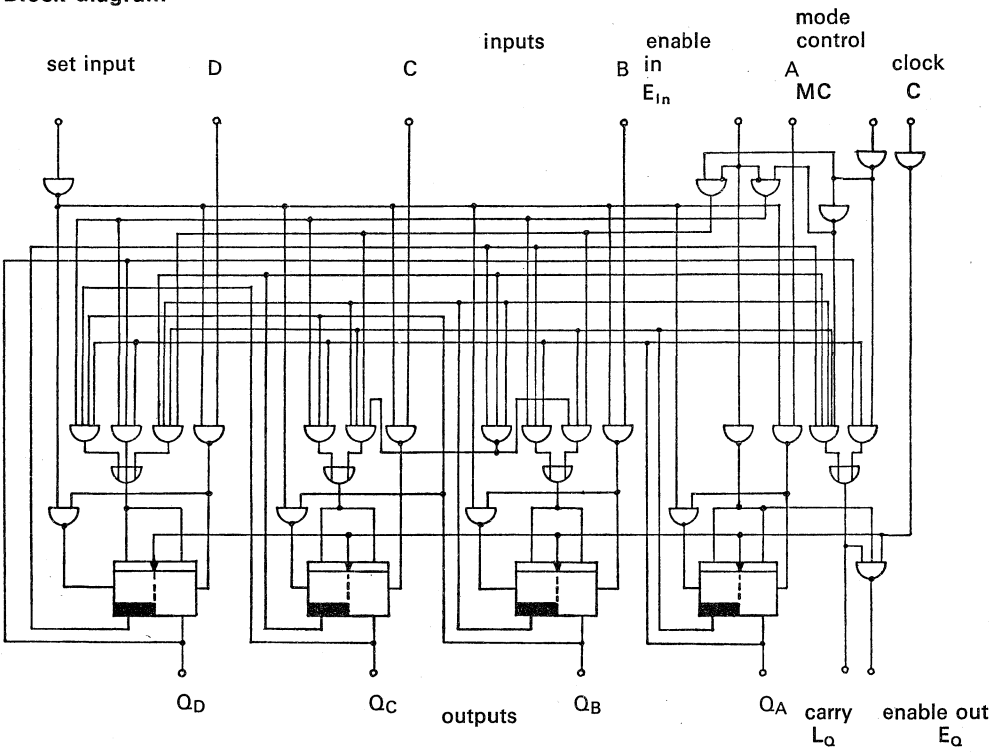
The FLJ 201/205 are reversible decimal counters. L-signal at enable E_I releases the counter. H-signal at E_I inhibits the counter. The operating mode is determined by the mode control input MC as follows: MC=L: count up; MC=H: count down. The initial condition of the counter is programmed independent of the clock input by means of the inputs A, B, C, D, and an L-signal at the set input $\overline{S}$. The counter can be operated as modulo-n-divider. Synchronous as well as asynchronous operation over several decades can be realized by means of the carry and enable outputs C_Q, E_Q which supply an H-signal and an L-signal respectively after the 9th clock pulse.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	$-I_{QH}$=800 µA | V_S	2.4			V
L-output voltage	V_{QL}	I_{QL}=16 mA | =4.75 V			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current,	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
each input	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current,	$-I_{IL}$	V_S=5.25 V			1.6	mA
each input		V_{IL}=0.4 V				
Short circuit output	$-I_Q$	V_S=5.25 V	18		55	mA
current, each output		V_Q=0 V				
Supply current	I_S	V_S=5.25 V		65	105	mA
Delay times, V_S=5 V, T_A=25 °C						
Clock pulse duration	t_{pC}		25			ns
Set pulse duration	t_{pS}		35			ns
Setup time at A, B, C, D	t_S		20			ns
Hold time at A, B, C, D,	t_H		0			
Maximum clock frequency	f		20	25		MHz
Propagation delay						
from $\overline{S}$ to Q	t_{PLH}			22	33	ns
	t_{PHL}			33	50	ns
from A, B, C, D to Q	t_{PLH}			14	22	ns
	t_{PHL}	C_L=15 pF		35	50	ns
from C to E	t_{PLH}	R_L=400 Ω		13	20	ns
	t_{PHL}			16	24	ns
from C to Q	t_{PLH}			16	24	ns
	t_{PHL}			24	36	ns
from C to carry C_Q	t_{PLH}			28	42	ns
	t_{PHL}			37	52	ns
Logical data						
Output load factor, each output	F_Q				10	
Input load factor, enable input	F_I				1	
remaining inputs	F_I				3	



Pin configuration
top view

Block diagram



FLJ 211 – 74191
FLJ 215 – 84191

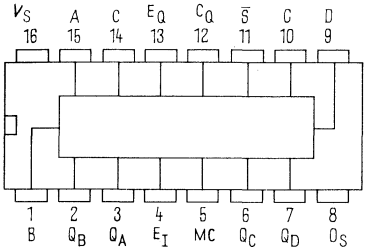
order numbers

FLJ 211: Q67000–J145
FLJ 215: Q67000–J199

Binary Counter, Reversible with Set and Reset

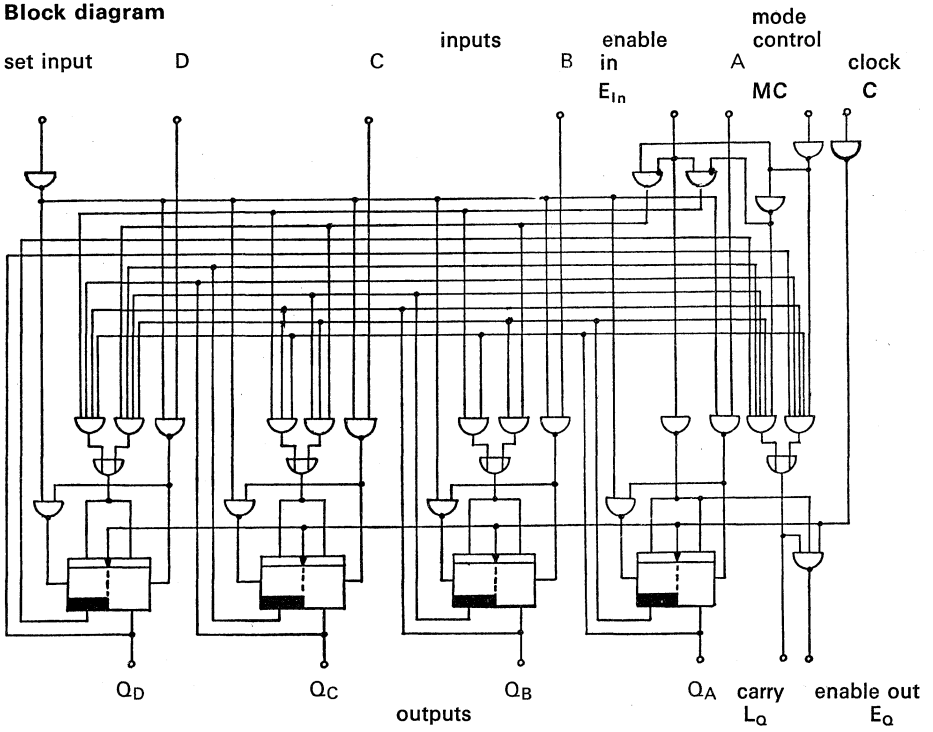
The FLJ 211/215 are reversible binary counters. L-signal at enable E_I releases the counter. H-signal at E_I inhibits the counter. The operating mode is determined by the mode control input MC as follows: MC=L: count up, MC=H: count down. The initial condition of the counter is programmed independent of the clock input by means of the inputs A, B, C, D and an L-signal at the set input $\overline{S}$. The counter can be operated as modulo-n-divider. Synchronous as well as asynchronous operation over several decades can be realized by means of the carry and enable outputs C_Q, E_Q which supply an H-signal and an L-signal respectively after the 15th clock pulse.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{OH}	$-I_{OH}$=800 µA | V_S	2.4			V
L-output voltage	V_{OL}	I_{OL}=16 mA | =4.75 V			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current,	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
each input	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_Q=0 V	18		55	mA
Supply current	I_S	V_S=5.25 V		65	105	mA
Delay times, V_S=5 V, T_A=25 °C						
Clock pulse duration	t_{pC}		25			ns
Set pulse duration	t_{pS}		35			ns
Setup time at A, B, C, C	t_S		20			ns
Hold time at A, B, C, D	t_H		0			
Maximum clock frequency	f		20	25		MHz
Propagation delay						
from $\overline{S}$ to Q	t_{PLH}			22	33	ns
	t_{PHL}			33	50	ns
from A, B, C, D to Q	t_{PLH}			14	22	ns
	t_{PHL}	C_L=15 pF		35	50	ns
from C to E	t_{PLH}	R_L=400 Ω				
	t_{PHL}			16	24	ns
from C to Q	t_{PLH}			16	24	ns
	t_{PHL}			24	36	ns
from C to carry C_Q	t_{PLH}			28	42	ns
	t_{PHL}			37	52	ns
Logical data						
Output load factor, each output	F_Q				10	
Input load factor, enable input	F_I				1	
remaining inputs	F_I				3	



Pin configuration
top view

Block diagram



FLJ 221 – 7491A
FLJ 225 – 8491A

order numbers

FLJ 221: Q67000–J32
FLJ 225: Q67000–J252

8-Bit-Shiftregister, Serial in/out

The FLJ 221/225 have serial inputs and outputs. The typical clock frequency is 18 MHz. The information is transferred at the rising edge of the clock pulse. The FLJ 221/225 is compatible with the flipflops FLJ 101/105 and FLJ 141/145.

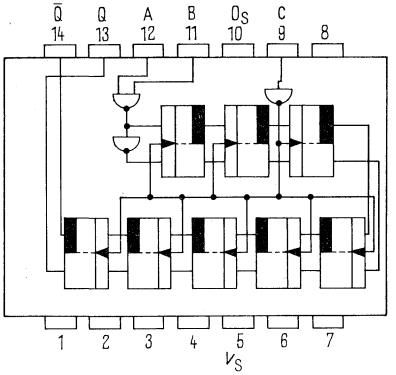
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V $-I_{QH}$=400 µA	2.4	3.5		V
L-output voltage	V_{QL}	V_S=4.75 V I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH} I_I	V_{IH}=2.4 V | V_S V_I=5.5 V | =5.25 V			40 1.0	µA mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V V_Q=0 V	18		57	mA
Supply current	I_S	V_S=5.25 V V_I=4.5 V		35	58	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{pC}		25			ns
Setup time	t_S		25			ns
Hold time	t_H		0			ns
Maximum clock frequency	f	C_L=15 pF R_L=400 Ω	10	18		MHz
Propagation delay from C to Q	t_{PHL}			27	40	ns
	t_{PLH}			24	40	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	



Pin configuration
top view

FLJ 231 – 7494
FLJ 235 – 8494

order numbers
FLJ 231: Q67000–J35
FLJ 235: Q67000–J200

4-Bit-Shiftregister, Parallel in, Serial out

The FLJ 231/235 are 4-bit-shiftregisters with serial and parallel inputs and serial output. The flipflops are set to its initial state either by set input S_1 or S_2. The inputs A_1, B_1, C_1, D_1 are enabled at S_1=H and S_2=L. For S_1=L and S_2=H A_2, B_2, C_2, D_2 are enabled. S_1 or S_2 and the reset input R must return to L before the first clock pulse. S_1, S_2, and R operate independent of the clock pulse. All flipflops are reset to Q=L if R switches to H.
Applications: Serial register, parallel-serial-converter with selective information gating.

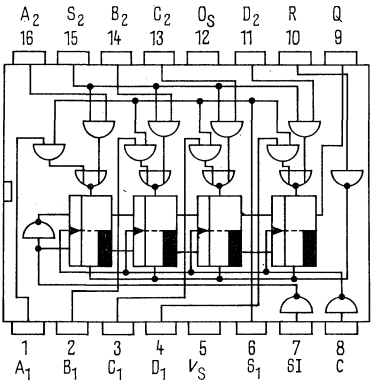
Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4	3.5		V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input except set inputs S_1 and S_2	I_{IH}	V_{IH}=2.4 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1	mA
H-input current at set inputs S_1 and S_2	I_{IH}	V_{IH}=2.4 V			160	µA
	I_I	V_I=5.5 V			1	mA
L-input current, each input except set inputs S_1 and S_2	$-I_{IL}$	V_S=0.4 V, V_{IL}=0.4 V			1.6	mA
L-input current at set inputs S_1 and S_2	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			6.4	mA
Short circuit output current	$-I_Q$	V_S=5.25 V				mA
Supply current	I_S	V_S=5.25 V		35	57	mA

Delay times, V_S=5 V, T_A=25 °C		test codition	lower limit B	typ.	upper limit A	unit
Clock pulse duration	t_{pC}		35			ns
Reset pulse duration	t_{pR}		30			ns
Set pulse duration	t_{pS}		30			ns
Setup time at SI						
H-signal	t_S		35			ns
L-signal	t_S		25			ns
Hold time at SI	t_H		0			ns
Maximum clock frequency	f		10			MHz
Propagation delay from	t_{PHL}	C_L=15 pF		25	40	ns
C to Q	t_{PLH}	R_L=400 Ω			40	ns
Propagation delay from	t_{PHL}			25	40	ns
R or S to Q	t_{PLH}				35	ns

Logical data

Output load factor	F_Q				10	
Input load factor	F_I				4	
each set input S_1 and S_2						
Input load factor	F_I				1	
of the remaining inputs						



Pin configuration
top view

SI = Serial input

FLJ 241 – 74192
FLJ 245 – 84192

order numbers

FLJ 241: Q67000–J174
FLJ 245: Q67000–J201

Decimal Counter with Clock Inputs for up and down Count

The FLJ 241/245 are synchronous, reversible decimal counters with set and reset inputs. The counters are reset to Q = L by R = H. The information present at the inputs A, B, C, D is transferred to the Q-outputs at $\overline{S}$ = L. Up and down-count is accomplished by separate clock inputs. While counting the unused clock input and the set input must be supplied with an H-signal and the reset input with an L-signal. Several counters are cascaded by connecting the carry and borrow outputs C_Q, B_Q with the corresponding clock inputs of the next stage.

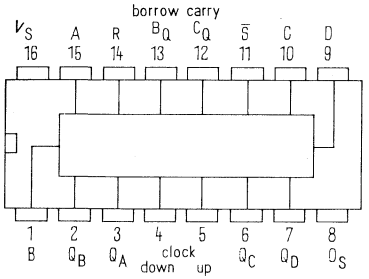
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S =5.25 V			40	µA
	I_I	V_I=5.5 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V V_Q=0 V	18		65	mA
Supply current	I_S	V_S=5.25 V		65	102	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{pC}		20			ns
Setup time at A, B, C, D	t_S		20			ns
Hold time at A, B, C, D	t_H		0			ns
Maximum clock frequency	f		25	32		MHz
Propagation delay from C to Q	t_{PHL}			31	47	ns
from C to C_Q or B_Q	t_{PHL}	C_L=15 pF R_L=400 Ω		16	24	ns
Propagation delay from C to Q	t_{PLH}			25	38	ns
from C to C_Q or B_Q	t_{PLH}			17	26	ns
Propagation delay from R or $\overline{S}$ to Q	t_{PHL}			22	35	ns
	t_{PLH}			29	40	ns

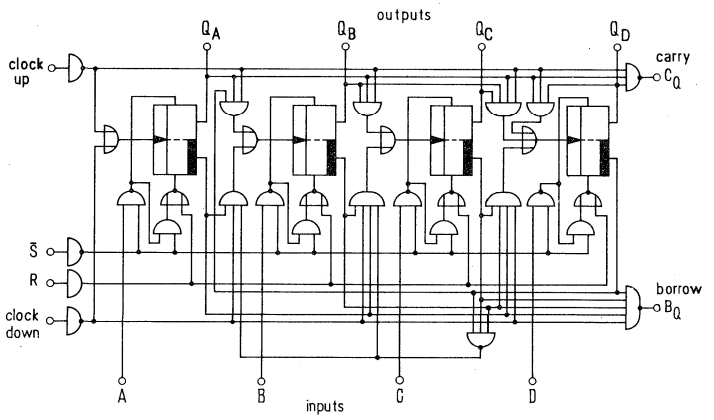
Logical data

Output load factor, each output	F_Q		10	
Input load factor, each input	F_I		1	



Pin configuration
top view

Block diagram



FLJ 251 – 74193
FLJ 255 – 84193

order numbers

FLJ 251: Q67000–J175
FLJ 255: Q67000–J202

Binary Counter with Clock Inputs for up and down Count

The FLJ 251/255 are synchronous, reversible binary counters with set and reset inputs. The counters are reset to Q = L by R = H. The information present at the inputs A, B, C, D is transferred to the Q-outputs at $\overline{S}$ = L. Up and down-count is accomplished by separate clock inputs. While counting the unused clock input and the set input must be supplied with an H-signal and the reset input with an L-signal. Several counters are cascaded by connecting the carry and borrow outputs C_Q, B_Q with the corresponding clock inputs of the next stage.

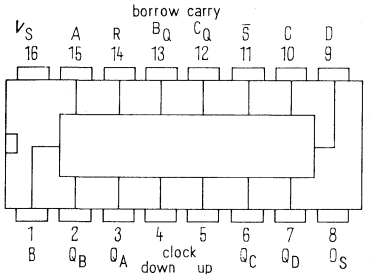
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_Q=0 V	18		65	mA
Supply current	I_S	V_S=5.25 V		65	102	mA

Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	f_{pC}		20			ns
Setup time at A, B, C, D	t_S		20			ns
Hold time at A, B, C, D	t_H		0			ns
Maximum clock frequency	f		25	32		MHz
Propagation delay from C to Q	t_{PHL}	C_L=15 pF, R_L=400 Ω		31	47	ns
from C to C_Q or B_Q	t_{PHL}			16	24	ns
Propagation delay from C to Q	t_{PLH}			25	38	ns
from C to C_Q or B_Q	t_{PLH}			17	26	ns
Propagation delay from R or $\overline{S}$ to Q	t_{PHL}			22	35	ns
	t_{PLH}			29	40	ns

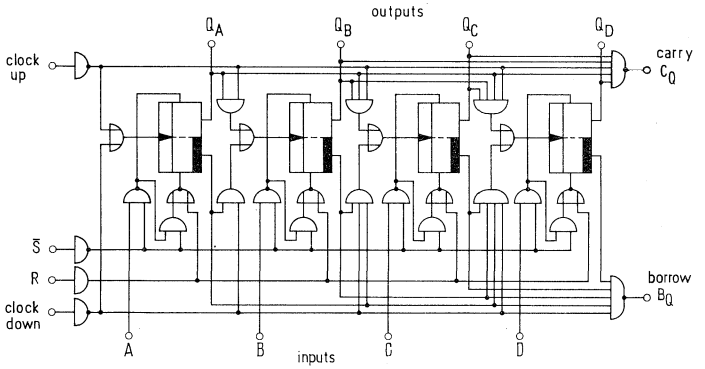
Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	



Pin configuration
top view

Block diagram



FLJ 261 – 7496
FLJ 265 – 8496

order numbers

FLJ 261: Q67000–J37
FLJ 265: Q67000–J203

5-Bit-Shiftregister, Parallel in/out

The FLJ 261/265 are 5-bit-shiftregisters with serial and parallel inputs and outputs. The flipflops are reset to Q = L independent of the clock pulse if the reset input $\overline{R}$ is supplied with an L-signal. The flipflops are set to Q = H by applying an H-signal to the inputs A through G and the set input S while $\overline{R}$ remains at H-level. The flipflops can be set simultaneously or independently. Set and reset inputs S and $\overline{R}$ must return to L and H respectively before the first clock pulse.
Applications: serial-parallel and parallel-serial-converters, registers, storage elements.

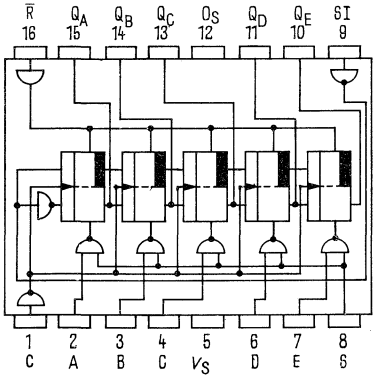
Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V $-I_{QH}$=400 µA	2.4	3.5		V
L-output voltage	V_{QL}	V_S=4.75 V I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
input except set input	I_I	V_I=5.5 V | =5.25 V			1.0	mA
H-input current	I_{IH}	V_{IH}=2.4 V | V_S			200	µA
at set input S	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current, each	$-I_{IL}$	V_S=5.25 V			1.6	mA
input except set input		V_{IL}=0.4 V				
L-input current	$-I_{IL}$	V_S=5.25 V			8.0	mA
at set input S		V_{IL}=0.4 V				
Short circuit output	$-I_Q$	V_S=5.25 V	18		57	mA
current, each output		V_Q=0 V				
Supply current	I_S	V_S=5.25 V		48	79	mA

Delay times, V_S=5 V, T_A=25 °C		test condition	lower limit B	typ.	upper limit A	unit
Clock pulse duration	t_{pC}		35			ns
Reset pulse duration	t_{pR}		30			ns
Set pulse duration	t_{pS}		30			ns
Setup time at SI	t_S		30			ns
Hold time at SI	t_H		0			ns
Maximum clock frequency	f		10			MHz
Propagation delay from C to Q	t_{PHL}	C_L=15 pF		25	40	ns
	t_{PLH}	R_L=400 Ω		25	40	ns
Propagation delay from $\bar{R}$ to Q	t_{PHL}				55	ns
from S to Q	t_{PLH}			28	35	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, at S	F_I				5	
remaining inputs	F_I				1	



Pin configuration
top view

SI = serial input

FLJ 271 – 74107
FLJ 275 – 84107

order numbers

FLJ 271: Q67000–J165
FLJ 275: Q67000–J222

Dual JK-Master-Slave-Flipflop

The flipflops are similar to the FLJ 121/125 except of the pin configuration.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current at J or K	I_{IH}	V_{IH}=2.4 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1.0	mA
H-input current at $\overline{R}$ or C	I_{IH}	V_{IH}=2.4 V			80	µA
	I_I	V_I=5.5 V			1.0	mA
L-input current at J or K	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
L-input current at $\overline{R}$ or C	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_I=0 V	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=5 V		20	40	mA

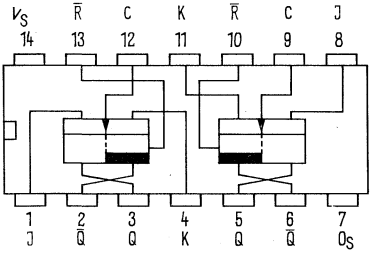
Delay times, V_S=5 V, T_A=25 °C

Clock pulse duration	t_{pC}		20			ns
Reset pulse duration	t_{pR}		25			ns
Setup time	t_S		t_{pT}			
Hold time	t_H		0			
Maximum clock frequency	f	R_L=400 Ω, C_L=15 pF	15	20		MHz
Propagation delay from C to Q	t_{PHL}		10	25	40	ns
	t_{PLH}		10	16	25	ns
Propagation delay from $\overline{R}$ to Q	t_{PHL}			25	40	ns
	t_{PLH}			16	25	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, at J or K	F_I				1	
Input load factor at $\overline{R}$ or C	F_I				2	

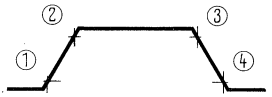
FLJ 271
FLJ 275



Pin configuration
top view

Block diagram see FLJ 121/125

Clock pulse



(1) isolate slave from master
(2) enter signal from J and K into master
(3) disable inputs J and K
(4) transfer information from master to slave

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at $\bar{R}$ sets Q to L – $\bar{R}$ operates independent of C.

FLJ 281 – 74104
FLJ 291 – 74105

order numbers

FLJ 281: Q6700–J241
FLJ 291: Q67000–J242

JK-Master-Slave-Flipflop with JK-Input
JK-Master-Slave-Flipflop with $\overline{J}$, $\overline{K}$, and JK-Inputs

The FLJ 281 has an additional JK-input to inhibit the flipflop. Due to slightly greater input capacitors of the J and K inputs, setup and hold times are prolonged. Thus the flipflops are in particular suited for slowly rising clock pulses. The FLJ 291 has additional $\overline{J}$, $\overline{K}$, and JK-inputs. The FLJ 291 is suitable for higher toggle frequencies than the FLJ 281 due to small input capacitors.
Data present at the J and K-inputs is accepted while the clock is at L-level. The data are transferred to the Q-outputs during the rising edge of the clock pulse.

Electrical characteristics
temperature range 1

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1.4	1.7	2.0	V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V $-I_{QH}$=1 mA	2.4	2.7		V
L-output voltage	V_{QL}	V_S=4.75 V I_{QL}=16 mA		0.2	0.4	V
H-input current at J, K, $\overline{J}$, $\overline{K}$	I_{IH}	V_S=5.25 V, V_{IH}=4.5 V		2	40	µA
H-input current at JK	I_{IH}	V_S=5.25 V, V_{IH}=4.5 V		4	80	µA
H-input current at $\overline{R}$, $\overline{S}$	I_{IH}	V_S=5.25 V, V_{IH}=4,5 V		8	120	µA
L-input current at J, K, $\overline{J}$, $\overline{K}$	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V		1.1	1.6	mA
L-input current at JK	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V		2.2	3.2	mA
L-input current at $\overline{R}$, $\overline{S}$	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V		3	4.8	mA
Supply current FLJ 281	I_S	V_S=5 V		15	24	mA
FLJ 291	I_S	V_S=5 V		17	28	mA

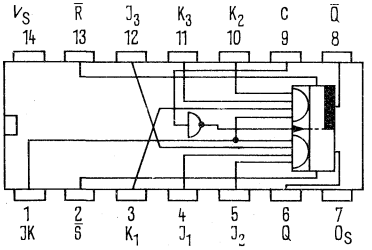
Delay times, V_S=5 V, T_{amb}=25 °C

Clock pulse duration referred to 1.5 V points	t_{pC}		15			ns
Set pulse duration	t_{pS}		20			ns
Reset pulse duration	t_{pR}		20			ns
Enable time FLJ 281	t_E				10	ns
FLJ 291	t_E				1	ns
Setup time FLJ 281	t_S		35			ns
FLJ 291	t_S		10			ns
Propagation delay from C to Q	t_{PLH} t_{PHL}	C_L=15 pF R_L=400 Ω		9 16	15 25	ns ns

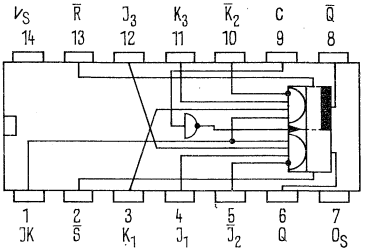
Logical data

Output load factor H-signal	F_{QH}		25
L-signal	F_{QL}		10
Input load factor at J, K, $\overline{J}$, $\overline{K}$	F_I		1
Input load factor at JK	F_I		2
Input load factor at $\overline{R}$, $\overline{S}$	F_I		3

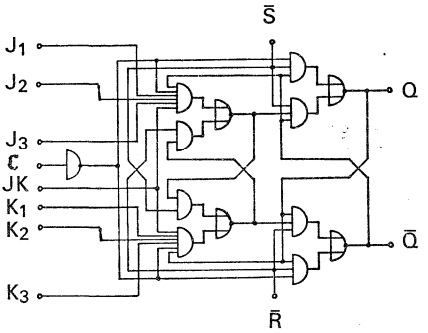
FLJ 281 Pin configuration
top view



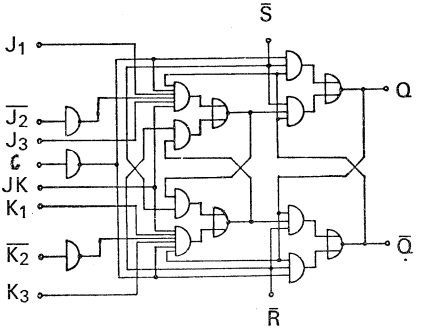
FLJ 291 Pin configuration
top view



FLJ 281 Block diagram



FLJ 291 Block diagram



Truth table

t_n			t_{n+1}
JK	J	K	Q
L*	X	X	Q_n
H	L*	L*	Q_n
H	L	H	L
H	H	L	H
H	H	H	$\overline{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
for FLJ 281: $J=J_1J_2J_3$
$K=K_1K_2K_3$
for FLJ 291: $J=J_1\overline{J}_2J_3$
$K=K_1\overline{K}_2K_3$

* L-levels must be applied while the clock is at L.
X=H or L-signal

L-level at $\overline{R}$ sets Q to L-signal. L-level at $\overline{S}$ sets Q to H-signal.
$\overline{R}$ and $\overline{S}$ operate independent of C.

FLJ 301 – 74100
FLJ 305 – 84100

order numbers

FLJ 301: Q67000–J164
FLJ 305: Q67000–J233

Eight D-Flipflops

The D-flipflop FLJ 301/305 are in particular suited as scratch pad memories. Any information present at the data-inputs D is transferred to the Q-outputs when the clock is at H-level. If the clock is at L-level, the D-input is disabled.

Electrical characteristics temperature ranges 1 and 5		test condition		lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V		2			V
L-input voltage	V_{IL}	V_S=4.75 V				0.8	V
H-output voltage	V_{QH}	$-I_{QH}$=400 µA	V_S= 4.75 V	2.4			V
L-output voltage	V_{QL}	I_{QL}=16 mA	V_S= 4.75 V			0.4	V
H-input current at D	I_{IH}	V_{IH}=2.4 V	V_S= 5.25 V			80	µA
	I_I	V_I=5.5 V	V_S= 5.25 V			1	mA
H-input current at C	I_{IH}	V_{IH}=2.4 V	V_S= 5.25 V			320	µA
	I_I	V_I=5.5 V	V_S= 5.25 V			1	mA
L-input current at D	$-I_{IL}$	V_{IL}=0.4 V	V_S= 5.25 V			3.2	mA
L-input current at C	$-I_{IL}$	V_{IL}=0.4 V	V_S= 5.25 V			12.8	mA
Short circuit output current, each output	$-I_Q$	V_Q=0 V	V_S= 5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		64		106	mA

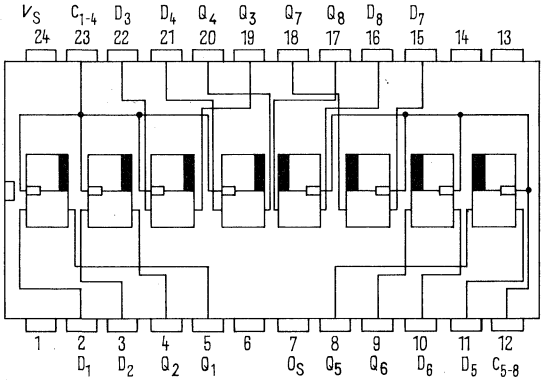
Delay times, V_S=5 V, T_{amb}=25 °C

H-setup time at D	t_S	C_L=15 pF, R_L=400 Ω			7	20	ns
L-setup time at D	t_S	C_L=15 pF, R_L=400 Ω			14	20	ns
H-hold time at D	t_H	C_L=15 pF, R_L=400 Ω		0	15		ns
L-hold time at D	t_H	C_L=15 pF, R_L=400 Ω		0	6		ns
Propagation delay from D to Q	t_{PHL}	C_L=15 pF, R_L=400 Ω			16	30	ns
	t_{PLH}	C_L=15 pF, R_L=400 Ω			14	25	ns
Propagation delay from C to Q	t_{PHL}	C_L=15 pF, R_L=400 Ω			16	30	ns
	t_{PLH}	C_L=15 pF, R_L=400 Ω			7	15	ns

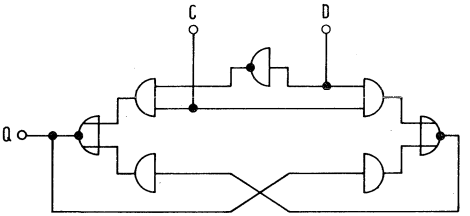
Logical data

Output load factor, each output	F_Q					10	
Input load factor at D	F_I					2	
Input load factor at C	F_I					8	

FLJ 301
FLJ 305



Pin configuration
top view



Block diagram (each flipflop)

Truth table (each flipflop)

t_n	t_{n+1}
D	Q
H	H
L	L

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

FLJ 311 – 74198
FLJ 315 – 84198
FLJ 321 – 74199
FLJ 325 – 84199
FLJ 461 – 74166
FLJ 465 – 84166

order numbers

FLJ 311:	Q67000–J244
FLJ 315:	Q67000–J235
FLJ 321:	Q67000–J245
FLJ 325:	Q67000–J237
FLJ 461:	Q67000–J282
FLJ 465:	Q67000–J300

Universal 8-Bit-Shiftregister, Reversible

The FLJ 311/315 are 8-bit-shiftregisters with the following operating modes: shift right or left, serial and parallel in and out, reset to L independent of the clock pulse and clock inhibit.
The FLJ 321/325 are similar to the FLJ 311/315 except that right shift operation is provided only.
The FLJ 461/465 are 8-bit-shiftregisters featuring right shift operation, serial and parallel inputs, serial outputs, independent reset inputs, and clock inhibit inputs.
Operating conditions of the registers are set forth by pulse diagrams.
Applications: storage and register elements, serial-parallel and parallel-serial-converters up to typical clock frequencies of 35 MHz.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	µA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		72	116	mA

Delay times, V_S=5 V, T_{amb}=25 °C, F_Q=10

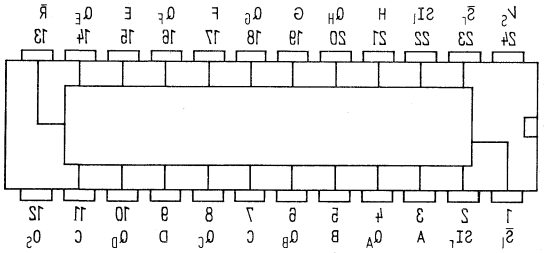
Maximum clock frequency	f		25	35		MHz
Clock or Reset pulse duration	$t_{pC,\,R}$		20			ns
Setup time	t_S		30			ns
Hold time	t_H		0			ns
Propagation delay from R to Q	t_{PHL}			23	35	ns
Propagation delay	t_{PHL}		8	20	30	ns
from C to Q	t_{PLH}		8	17	26	ns

Logical data

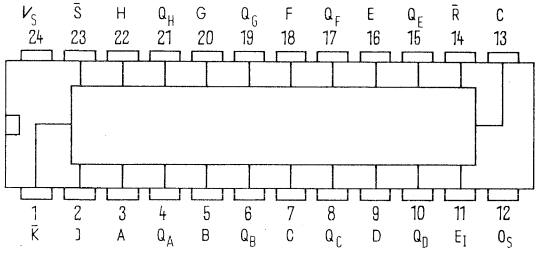
Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor, each input	F_I				1	

FLJ 311
FLJ 315
FLJ 321
FLJ 325
FLJ 461
FLJ 465

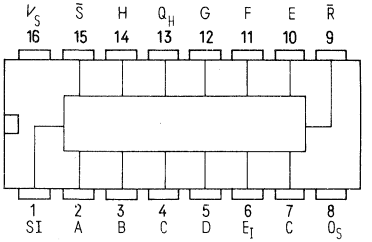
Pin configurations
top view



FLJ 311
FLJ 315

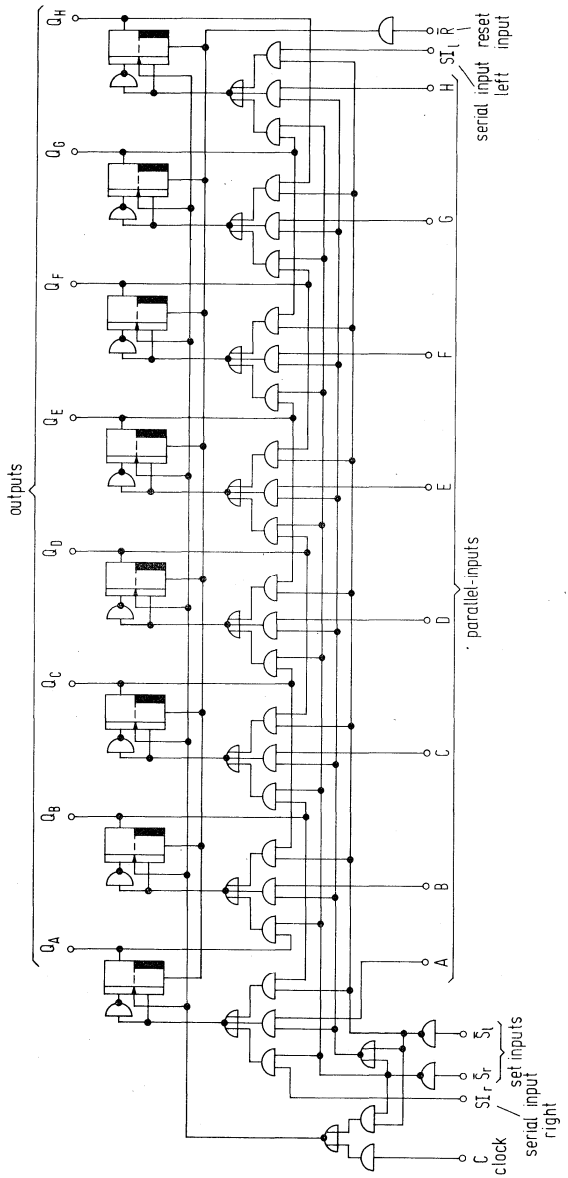


FLJ 321
FLJ 325



FLJ 461
FLJ 465

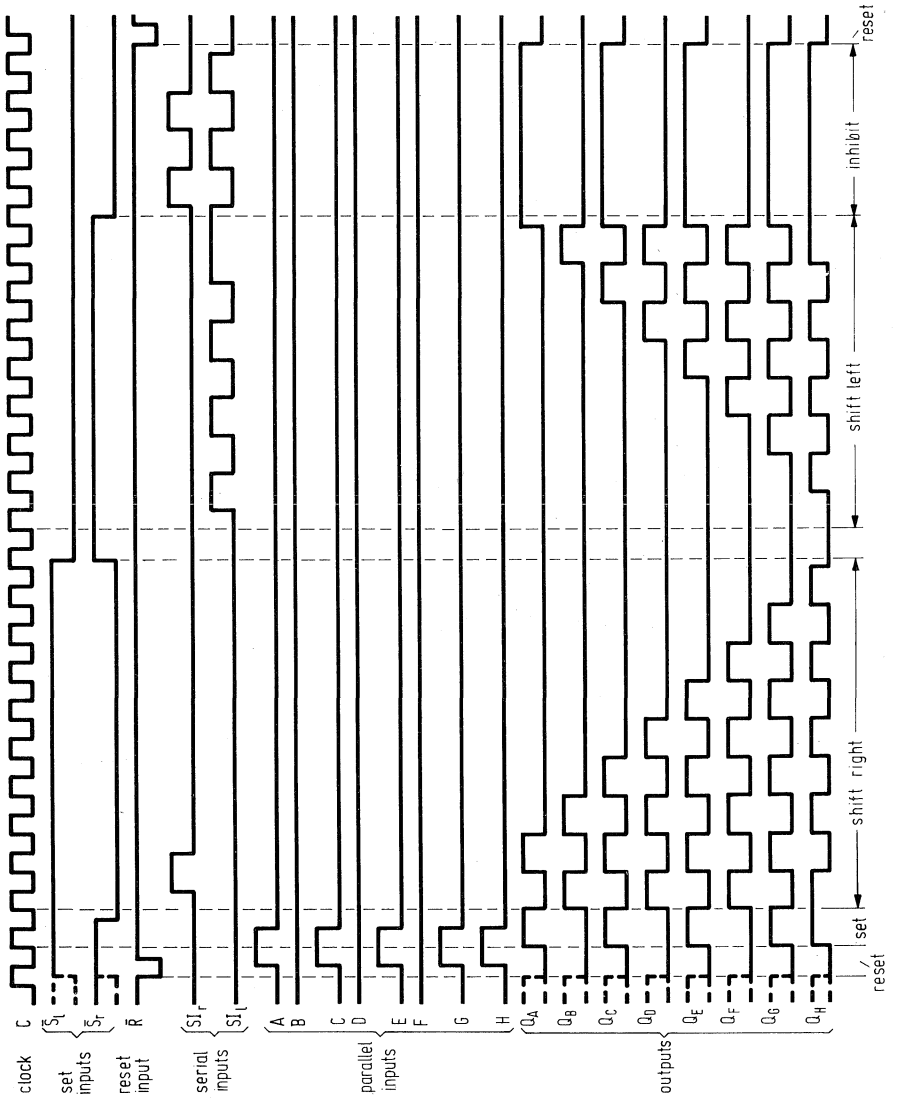
FLJ 311
FLJ 315



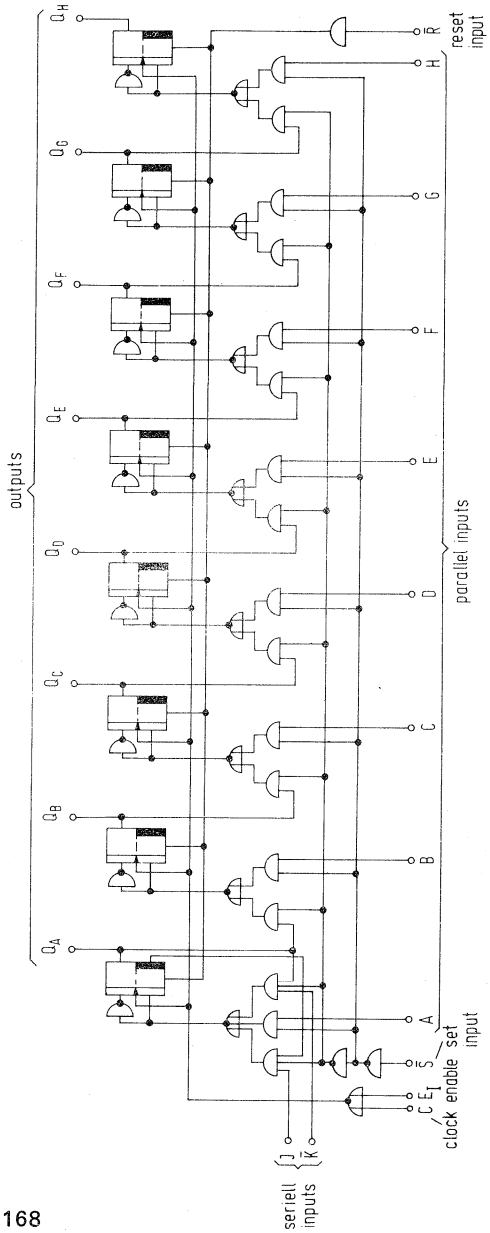
Truth table

set inputs $\bar{S}_r$	set inputs $\bar{S}_l$	operating modes
L	L	inhibit clock
L	H	shift right serial input SI_r
H	L	shift left serial input SI_l
H	H	parallel load inputs A through H

Pulse diagram



FLJ 321
FLJ 325



Block diagram

inputs at t_n		output Q_A at t_{n+1}
J	$\overline{K}$	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

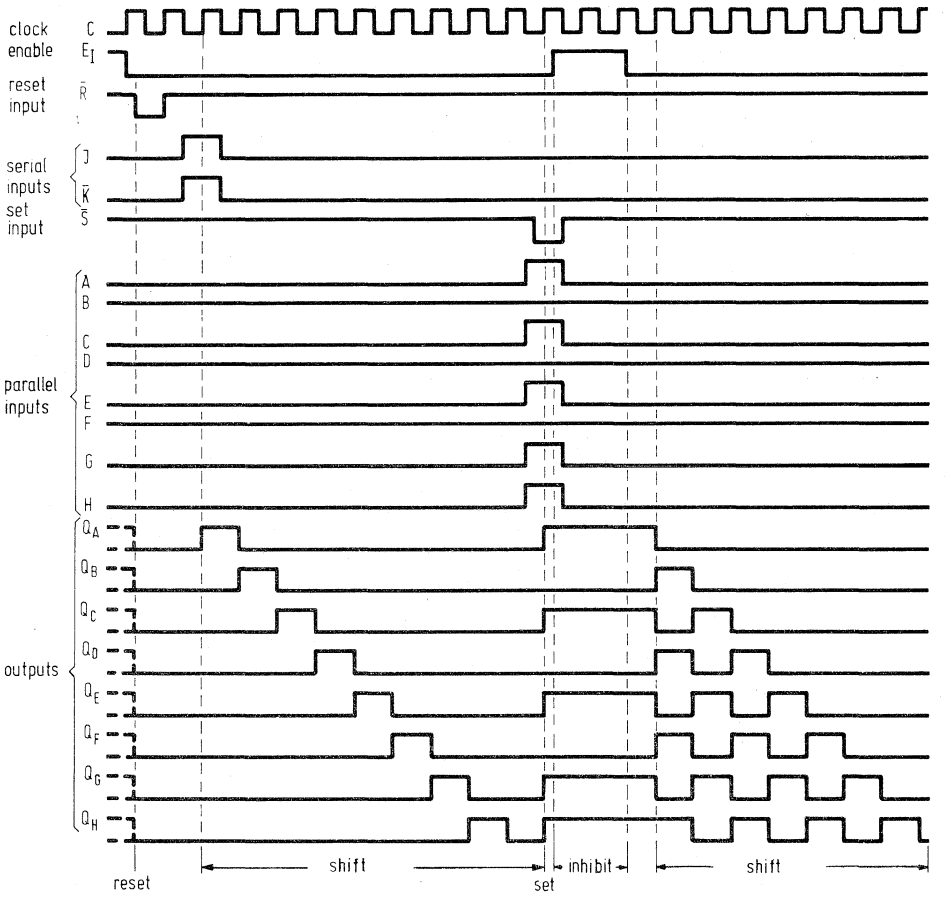
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

Truth table

set input $\overline{S}$	enable E_I	operating mode
H	L	shift right accept data from inputs J and $\overline{K}$
L	L	parallel load inputs A through H
X	H	register inhibited

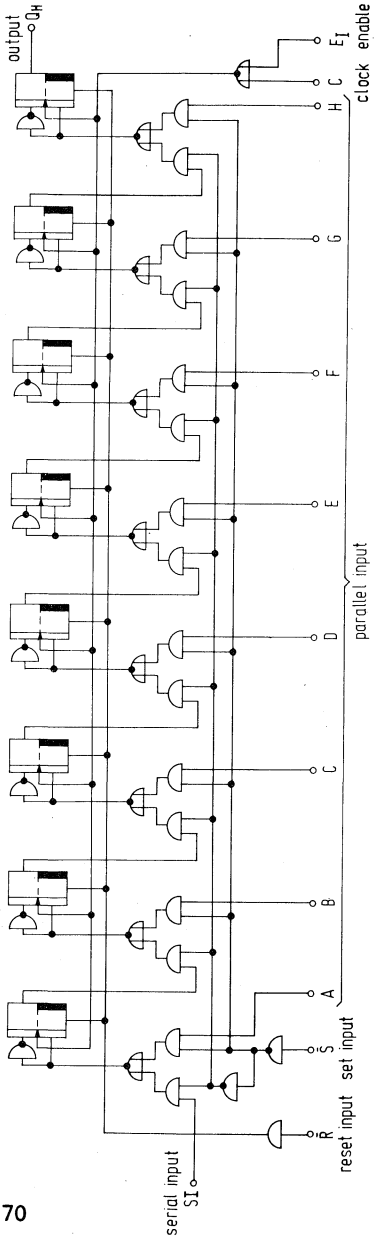
X = H or L-signal

Pulse diagram



FLJ 461
FLJ 465

Block diagram

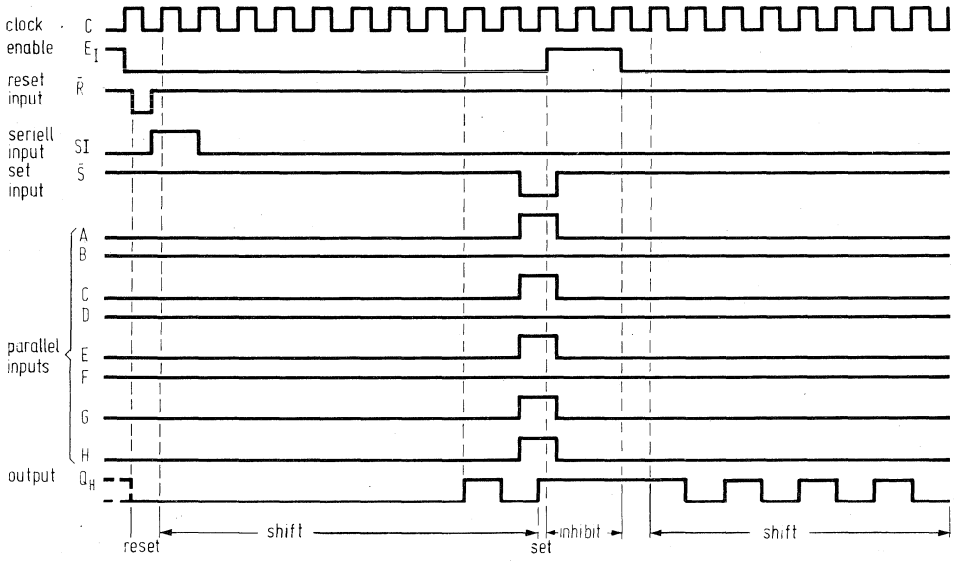


Truth table

clock C	enable input E_I	reset input $\bar{R}$	serial input SI	set input $\bar{S}$	parallel input A through H	operating mode
X	X	L	X	X	X	reset
1 pulse	L	H	L	L	data	parallel load
N pulses	L	H	X	H	X	shift
N pulses	L	H	data	H	X	serial load
X	H	H	X	X	X	inhibit

X = H or L-signal

Pulse diagram



FLJ 331 – 7497

order numbers
FLJ 331: Q67000–J240

Programmable 6-Bit-Rate Multiplier

The FLJ 331 performs fixed-rate or variable rate frequency division. The division ratio is selected by means of the inputs A through F as follows:

$f_Q = f_I \times \frac{M}{64}$, where $M = A \times 2^0 + B \times 2^1 + C \times 2^2 + D \times 2^3 + E \times 2^4 + F \times 2^4$.

The clock frequency is 32 MHz typically.
The divider is released by L-signal at the enable input E_I and the reset input R.
H-signal at the strobe disables the divider output Q.
Dividers are cascaded by connecting the enable output E_Q of the first stage to the enable input E_I and the strobe input of the second stages. $\bar{Q}$-outputs are crossconnected with the expander inputs N. The desired output frequency results at the outputs Q of each divider stage.
Applications: division, analog-digital and digital-analog-conversion.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			08	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current at C	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			80	µA
remaining inputs	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current at C	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
remaining inputs	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V		58		mA
L-supply current	I_{SL}	V_S=5.25 V		80	120	mA

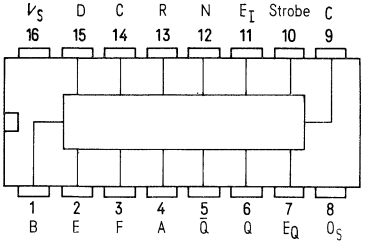
Delay times, V_S=5 V, T_{amb}=25 °C, F_Q=10

Maximum clock frequency	f		25	32		MHz
Clock pulse duration	t_{pC}		20			ns
Setup time	t_S		25			ns
Hold time	t_H		0			ns
Propagation delay from C to Q	t_{PLH}	C_L=15 pF, R_L=400 Ω		26	39	ns
	t_{PHL}	C_L=15 pF, R_L=400 Ω		20	30	ns
Propagation delay from strobe to Q	t_{PLH}	C_L=15 pF, R_L=400 Ω		19	30	ns
	t_{PHL}	C_L=15 pF, R_L=400 Ω		22	33	ns

Logical data

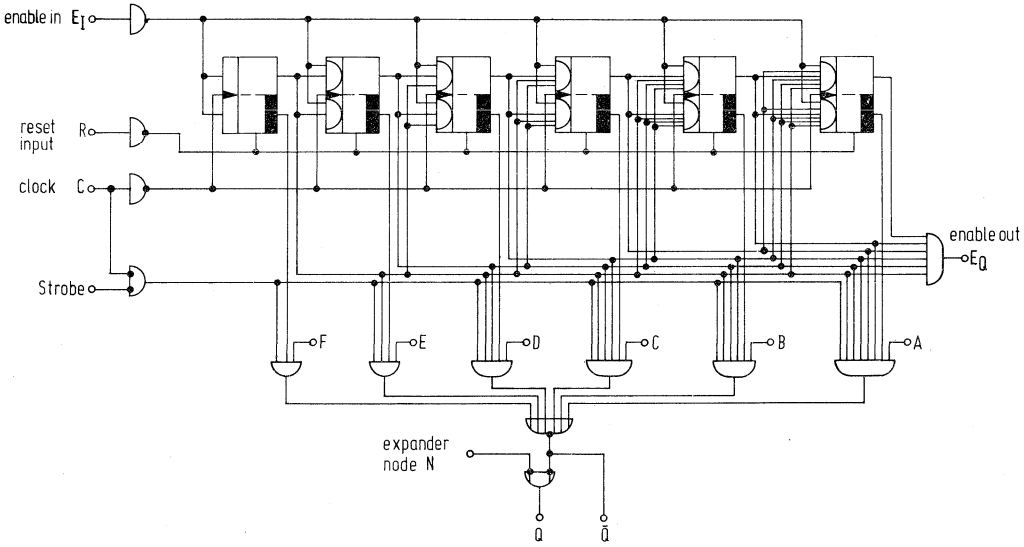
Output load factor	F_Q				10	
input load factor C-input	F_I				2	
remaining inputs	F_I				1	

FLJ 331



Pin configuration
top view

Block diagram



FLJ 331

Truth table

inputs											outputs		
reset input R	enable input E_I	strobe	binary division ratio						number of block pulses	Expander input N	Logic state or number of pulses		
			A	B	C	D	E	F			Q	$\bar{Q}$	E_Q
H	X	H	X	X	X	X	X	X	X	H	L	H	H
L	L	L	L	L	L	L	L	L	64	H	0	0	1
L	L	L	H	L	L	L	L	L	64	H	1	1	1
L	L	L	L	H	L	L	L	L	64	H	2	2	1
L	L	L	L	L	H	L	L	L	64	H	4	4	1
L	L	L	L	L	L	H	L	L	64	H	8	8	1
L	L	L	L	L	L	L	H	L	64	H	16	16	1
L	L	L	L	L	L	L	L	H	64	H	32	32	1
L	L	L	H	H	H	H	H	H	64	H	63	63	1
L	L	L	H	H	H	H	H	H	64	L	0	63	1[1]
L	L	L	L	L	H	L	H	L	64	H	20	20	1[2]

Notes:
X = H or L-signal
Inputs A through F can be varied as required.

[1]) The output Q can be disabled by means of the expander input N.

[2]) $f_Q = f_I \times \frac{M}{64} = f_I \times \frac{16 + 4}{64} = 0.3125 \times f_I$

order numbers

FLJ 341: Q67000–J224
FLJ 345: Q67000–J274

FLJ 341 – 74110
FLJ 345 – 84110

JK-Master-Slave-Flipflop with Data Lockout

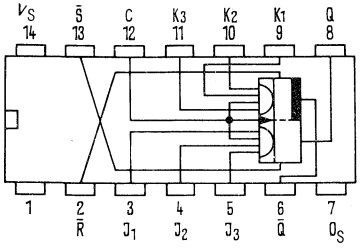
The FLJ 341/345 have a hold time t_H of 5 ns only. Thus the J- and K-signals may change during the clock pulse without causing an error information. The FLJ 341/345 are pin compatible with the FLJ 111/115.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75		5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current at JK	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
at $\overline{R}$ or $\overline{S}$	I_{IH}				80	µA
at C	I_{IH}				40	µA
L-input current at JK	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
at $\overline{R}$ or $\overline{S}$	$-I_{IL}$				3.2	mA
at C	$-I_{IL}$				4.8	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		20	34	mA

Delay times, V_S=5 V, T_{amb}=25 °C

Clock pulse duration	t_{pC}		25			ns
Set pulse duration	t_{pS}		25			ns
Reset pulse duration	t_{pR}		25			ns
Setup time	t_S		20			ns
Hold time	t_H		5			ns
Maximum clock frequency	f	C_L=15 pF, R_L=400 Ω	20	25		ns
Propagation delay	t_{PLH}		12	20		ns
from $\overline{S}$ or $\overline{R}$ to Q	t_{PHL}			18	25	ns
Propagation delay	t_{PLH}		10	20	30	ns
from C to Q	t_{PHL}		6	13	20	ns

FLJ 341
FLJ 345



Pin configuration
top view

Logical data

			upper limit A
Output load factor	H-signal	F_{QH}	20
	L-signal	F_{QL}	10
Input load factor			
JK-inputs		F_I	1
$\bar{R}$ and $\bar{S}$-inputs		F_I	2
C-input		F_I	3

Truth table

inputs at t_n J	K	outputs at t_{n+1} Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
J = J_1 J_2 J_3
K = K_1 K_2 K_3
L-level at $\bar{R}$ sets Q to L-signal
L-level at $\bar{S}$ sets Q to H-signal
$\bar{R}$ and $\bar{S}$ operate independent of C.

order numbers

FLJ 351: Q67000–J225
FLJ 355: Q67000–J289
FLJ 521: Q67000–J306
FLJ 525: Q67000–J376

FLJ 351 – 74111
FLJ 355 – 84111
FLJ 521 – 74115
FLJ 525 – 84115

Dual-JK-Master-Slave-Flipflop with Data Lockout

The FLJ 351/355 and FLJ 521/525 have a hold time t_H of 5 ns only. Thus the J- and K-signals may change during the clock pulse without causing an error information.
The FLJ 521/525 have reset inputs $\bar{R}$. The function of the FLJ 521/525 corresponds to the FLJ 121/125 except of the hold time t_H.
The FLJ 351/355 have set and reset inputs $\bar{S}$ and $\bar{R}$. The function of the FLJ 351/355 corresponds to the FLJ 131/135 except of the hold time t_H.

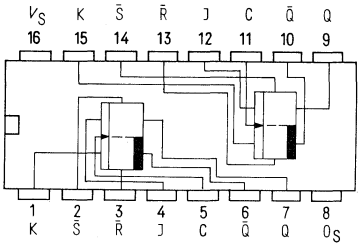
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75		5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current at JK	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
at $\bar{R}$ or $\bar{S}$	I_{IH}				80	µA
at C	I_{IH}				120	µA
L-input current at JK	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
at $\bar{R}$ or $\bar{S}$	$-I_{IL}$				3.2	mA
at C	$-I_{IL}$				4.8	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		28	41	mA

Delay times

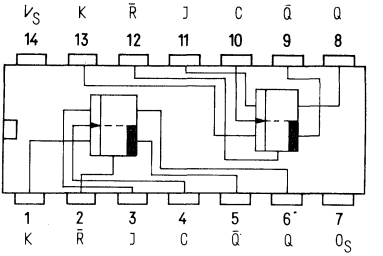
Clock pulse duration	t_{pC}		25			ns
Set pulse duration	t_{pS}		25			ns
Reset pulse duration	t_{pR}		25			ns
Setup time	t_S		0			ns
Hold time	t_H		30			ns
Maximum clock frequency	f		20	25		ns
Propagation delay	t_{PLH}			12	18	ns
from $\bar{S}$ or $\bar{R}$ to Q	t_{PHL}	C_L=15 pF, R_L=400 Ω		21	30	ns
Propagation delay	t_{PLH}		6	12	17	ns
from C to Q	t_{PHL}		10	20	30	ns

FLJ 351
FLJ 355
FLJ 521
FLJ 525

FLJ 351/355



FLJ 521/525



Pin configurations, top view

Logical data

			upper limit A
Output load factor	H-signal	F_{QH}	20
	L-signal	F_{QL}	10
Input load factor			
JK-inputs		F_I	1
$\bar{R}$ and $\bar{S}$ inputs		F_I	2
C-input		F_I	3

Truth table

inputs at t_n		outputs at t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
$J = J_1J_2J_3$
$K = K_1K_2K_3$

L-level at $\bar{R}$ sets Q to L-signal.
FLJ 321/325: L-signal at $\bar{S}$ sets Q to H-signal.
$\bar{R}$ and $\bar{S}$ operate independent of C.

order numbers

FLJ 361: Q67000–J275
FLJ 365: Q67000–J290
FLJ 371: Q67000–J276
FLJ 375: Q67000–J291

FLJ 361 – 74118
FLJ 365 – 84118
FLJ 371 – 74119
FLJ 375 – 84119

RS-Flipflops

FLJ 361/365: Six RS-flipflops with common reset input.
FLJ 371/375: Six RS-flipflops with seperate reset inputs.
Application: Storage elements.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IL}=0.8 V, $-I_{QH}$=800 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, I_{QL}=16 mA		0.22	0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current at $\bar{S}_1$ to $\bar{S}_6$ and $\bar{R}_1$ to $\bar{R}_6$	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
					1	mA
H-input current at $\bar{R}$	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			200	µA
L-input current at $\bar{S}_1$ to $\bar{S}_6$ and $\bar{R}_1$ to $\bar{R}_6$	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
L-input current at $\bar{R}$	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			8	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		30	60	mA

Delay times, V_S=5 V, T_{amb}=25 °C, F_Q=10

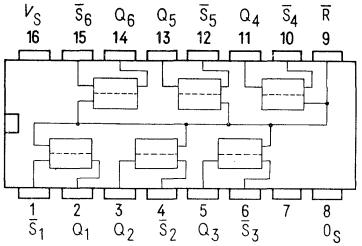
Propagation delay from $\bar{R}$ to Q	t_{PLH}	C_L=15 pF, R_L=100 Ω		18	29	ns
from $\bar{S}$ to Q	t_{PHL}	C_L=15 pF, R_L=100 Ω		18	17	ns

Logical data, each flipflop

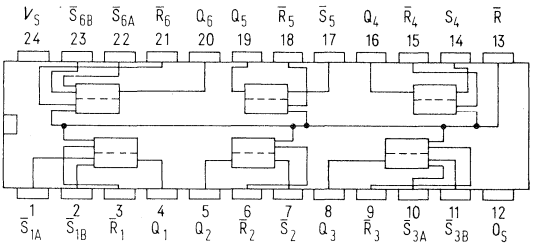
Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor $\bar{S}_1$ to $\bar{S}_6$ and $\bar{R}_1$ to $\bar{R}_6$	F_I				1	
$\bar{R}$	F_I				5	

FLJ 361 – 74118
FLJ 365 – 84118
FLJ 371 – 74119
FLJ 375 – 84119

FLJ 361/365



FLJ 371/375



Pin configurations, top view

Truth table, each flipflop

set inputs		reset inputs		output	
		separate	common		
$\bar{S}$ or $\bar{S}_A$	S_B[1])	$\bar{R}$[1])	$\bar{R}$	Q	
X	L	X	X	H	} valid for
H	H	L	X	L	} FLJ 371/375 only
L	X	X	X	H	
H	H	X	L	L	
H	H	H	H	store	

X = H or L-signal
[1]) FLJ 371/375 only

order numbers

FLJ 381: Q67000–J283
FLJ 385: Q67000–J292
FLJ 391: Q67000–J284
FLJ 395: Q67000–J293

FLJ 381 – 74196
FLJ 385 – 84196
FLJ 391 – 74197
FLJ 395 – 84197

Decimal Counter with Set and Reset for 50 MHz

The FLJ 381/385 can be preset by means of the data inputs A, B, C, D while the set input $\overline{S}$ is supplied with an L-signal. The counters are suitable for the following applications:
Decimal counter: C_2 and Q_A are connected, the clock pulse is supplied to C_1.
Biquinary counter: C_1 and Q_D are connected, the clock pulse is applied at C_2.
The counter supplies a symmetrical output pulse at Q_A in divide-by-ten applications.
Divide-by-two and divide-by-five counters: No connections are required. C_1 and C_2 operate independently. Set and reset functions remain common.
The FLJ 391/395 can be preset by means of the data inputs A, B, C, D while the set input $\overline{S}$ is supplied with an L-signal. The counters are suitable for the following applications:
4-bit-binary-counter: C_2 and Q_A are connected, the clock pulse is supplied to C_1.
3-bit-binary-counter: C_1 and Q_A are not used, the clock pulse is supplied to C_2.
Divide-by-two and divide-by-eight counters: C_1 and C_2 operate independently. Set and reset functions remain common.

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75		5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	$-V_{IL}$	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current					80	µA
at R, C_1, C_2 (FLJ 381/395)	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
at A, B, C, D, S	I_{IH}					
at C_2 (FLJ 381/385)	I_{IH}				120	µA
L-input current						
at A, B, C, D, $\overline{S}$	$-I_{IL}$				1.6	mA
at R, C_2 (FLJ 391/395)	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
at C_1	$-I_{IL}$				4.8	mA
at C_2 (FLJ 381/385)	$-I_{IL}$				6.4	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		48	59	mA

Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Maximum clock frequency						
at C_1	f		50	70		MHz
at C_2	f		25			MHz
Input pulse duration at C_1	t_{pC}		10			ns
at $\overline{R}$	t_{pR}		15			ns
at $\overline{S}$ and C_2	$t_{pS,C}$		20			ns
Setup time	t_S		15			ns
Hold time	t_H		20			ns

FLJ 381
FLJ 385
FLJ 391
FLJ 395

Propagation delay FLJ 381/385		test condition	lower limit B	typ.	upper limit A	unit
from C_1 to Q_A	t_{PLH}			7	12	ns
	t_{PHL}			10	15	ns
from C_2 to Q_B	t_{PLH}			12	18	ns
	t_{PHL}			14	21	ns
from C_2 to Q_C	t_{PLH}			24	36	ns
	t_{PHL}			28	42	ns
from C_2 to Q_D	t_{PLH}	C_L=15 pF, R_L=400 Ω		14	21	ns
	t_{PHL}			12	18	ns
from A, B, C, D, to Q_A, Q_B, Q_C, Q_D	t_{PLH}			16	24	ns
	t_{PHL}			25	38	ns
from $\bar{S}$ to any output	t_{PLH}			22	33	ns
	t_{PHL}			24	36	ns
from $\bar{R}$ to any output	t_{PHL}			25	37	ns
FLJ 391/395						
from C_1 to Q_A	t_{PLH}			7	12	ns
	t_{PHL}			10	15	ns
from C_2 to Q_B	t_{PLH}			12	18	ns
	t_{PHL}			14	21	ns
from C_2 to Q_C	t_{PLH}			24	36	ns
	t_{PHL}			26	42	ns
from C_2 to Q_D	t_{PLH}	C_L=15 pF, R_L=400 Ω		36	54	ns
	t_{PHL}			42	63	ns
from A, B, C, D, to Q_A, Q_B, Q_C, Q_D	t_{PLH}			16	24	ns
	t_{PHL}			25	36	ns
from $\bar{S}$ to any output	t_{PLH}			22	33	ns
	t_{PHL}			24	36	ns
from $\bar{R}$ to any output	t_{PHL}			25	37	ns

Logical data

Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor						
at A, B, C, D, and $\bar{S}$	F_I				1	
at $\bar{R}$-input	F_I				2	
at clock C_1	F_I				3	
at clock C_2 FLJ 381/385	F_I				4	
FLJ 391/395	F_I				2	

Truth tables

FLJ 381/385

Decimal counter (C_2 connected with Q_A)

clock pulses at C_1	outputs Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

FLJ 381/385

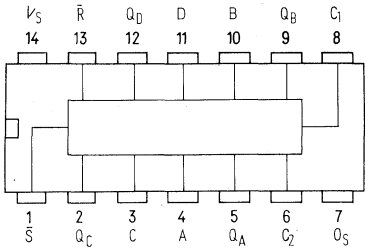
Biquinary counter (C_1 connected with Q_D)

clock pulses at C_2	outputs Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

FLJ 391/395

Binary counter (C_2 connected with Q_A)

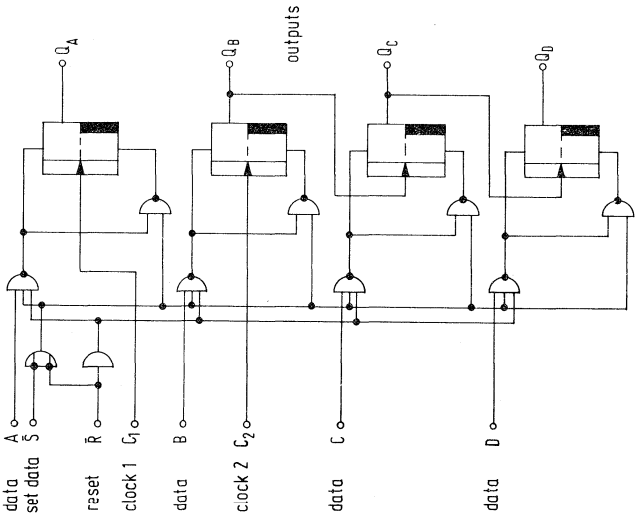
clock pulses at C_1	outputs Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H



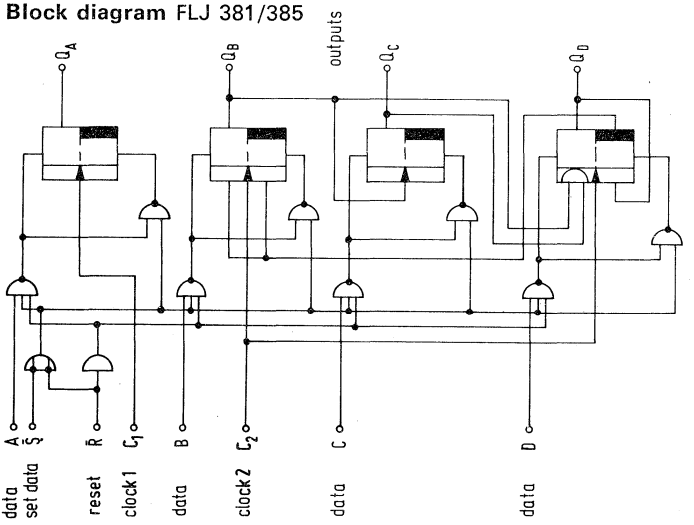
Pin configuration
top view

L-signal at $\bar{R}$ sets Q-outputs to L-signal.
L-signal at $\bar{S}$ sets Q-outputs to the respective data inputs.

Block diagram FLJ 391/395



Block diagram FLJ 381/385



order numbers
see next page

FLJ 401 – 74160 **FLJ 421** – 74162
FLJ 405 – 84160 **FLJ 425** – 84162
FLJ 411 – 74161 **FLJ 431** – 74163
FLJ 415 – 84161 **FLJ 435** – 84163

Synchronous Counters

FLJ 401/405: Synchronous decimal counters with synchronous set input and asynchronous reset input.
FLJ 421/425: Synchronous decimal counters with synchronous set and reset inputs.
FLJ 411/415: Synchronous binary counters with synchronous set input and asynchronous reset input.
FLJ 431/435: Synchronous binary counters with synchronous set and reset inputs.

The counters are in particular suited for high-speed counting system. Counters are cascaded by connecting C_Q of the first stage with E_{I2} of the next stage.
The clock frequency is 32 MHz typically. The function of the counters is shown by pulse diagrams.

Electrical characteristics
temperature ranges 1 and 5

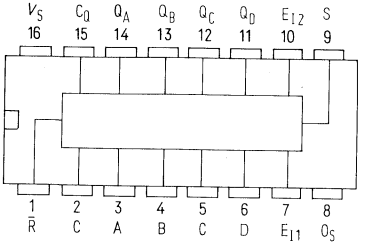
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=5.75 V	2.0			V
L-input voltage	V_{IL}	V_S=5.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current at C and E_{I2}	I_{IH}	V_S=5.25 V,			80	µA
remaining inputs	I_{IH}	V_{IH}=2.4 V			40	µA
L-input current at C and E_{I2}	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
remaining inputs	$-I_{IL}$				1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	57		18	mA
H-supply current	I_{SH}	V_S=5.25 V		59	93	mA
L-supply current	I_{SL}			63	101	mA

Delay times, V_S=5 V, T_{amb}=25 °C

Maximum clock frequency	f		25	32		MHz
Clock pulse duration	t_{pC}		25			ns
Reset pulse duration	t_{pR}		20			ns
Setup time	t_S		20			ns
Hold time	t_H		0			ns
Propagation delay						
from C to C_Q	t_{PLH}			23	35	ns
	t_{PHL}			23	23	ns
from C to Q	t_{PLH}	C_L=15 pF, R_L=400 Ω		13	20	ns
	t_{PHL}			15	23	ns
from E_{I2} to C_Q	t_{PLH}			8	13	ns
	t_{PHL}			10	15	ns
from $\bar{R}$ to Q	t_{PHL}			20	30	ns

order numbers

FLJ 401: Q67000–J277	FLJ 421: Q67000–J278
FLJ 405: Q67000–J294	FLJ 425: Q67000–J296
FLJ 411: Q67000–J273	FLJ 431: Q67000–J279
FLJ 415: Q67000–J295	FLJ 435: Q67000–J297



Pin configuration
top view

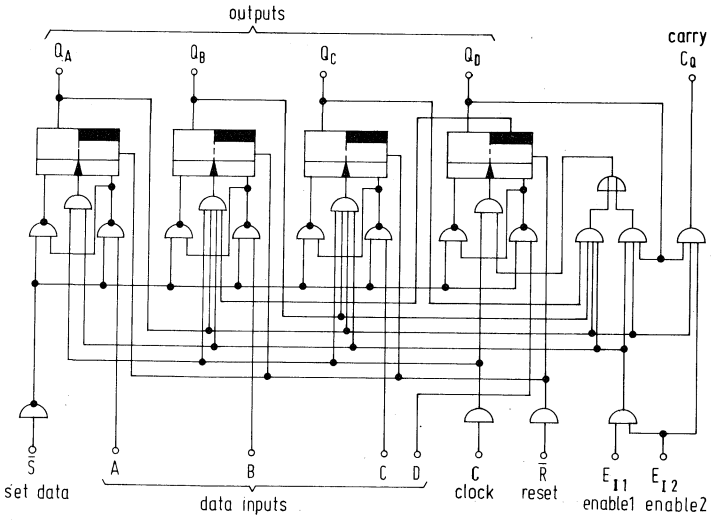
Truth table

		upper limit A
Output load factor H-signal	F_{QH}	20
L-signal	F_{QL}	10
Input load factor at C or E_{I2}	F_I	2
remaining inputs	F_I	1

block diagram

FLJ 401/405
FLJ 421/425

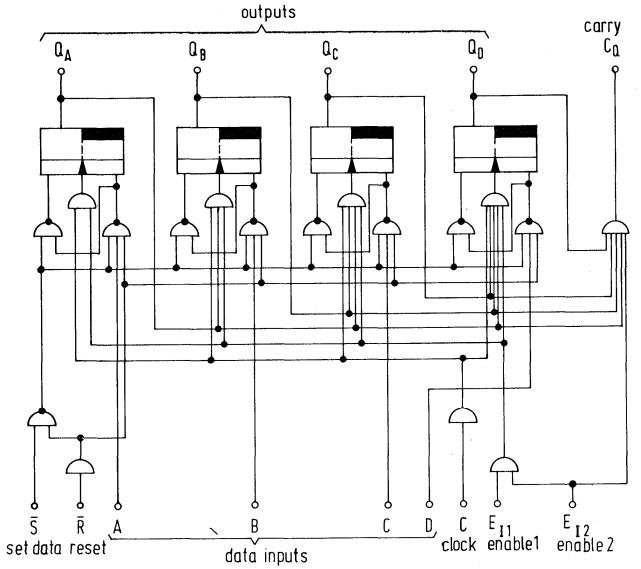
The clear function of the FLJ 421/425 is synchronous as shown for the FLJ 411/415 on the following page.



Block diagram

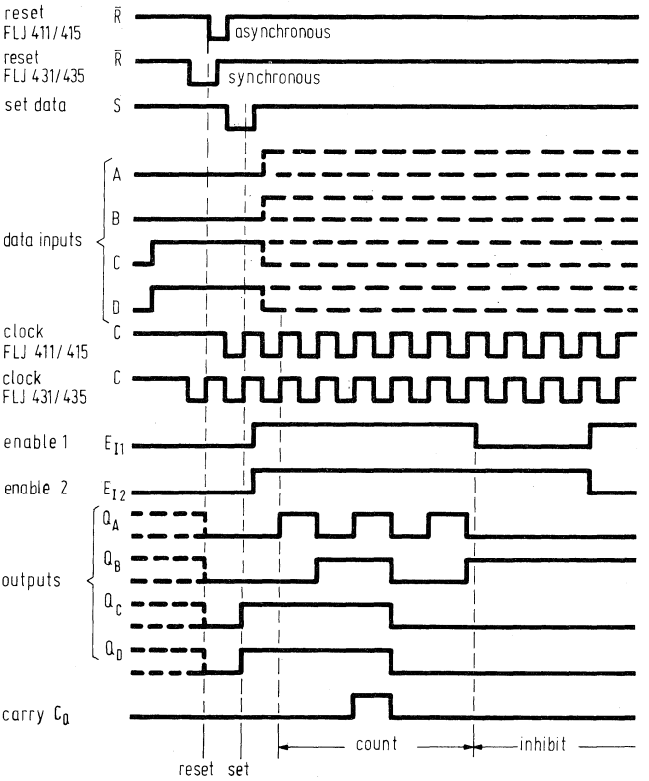
FLJ 411/415
FLJ 431/435

The clear function of the FLJ 411/415 is asynchronous as shown for the FLJ 401/405 on the preceding page.



FLJ 411
FLJ 415
FLJ 431
FLJ 435

Pulse diagram



Set, reset, count, and inhibit conditions

The following sequence is shown: reset to Q=LLLL
set to ABCD=$Q_AQ_BQ_CQ_D$=LLHH (12)
count from 13 to 2
inhibit

Order numbers

FLJ 441: Q67000–J280
FLJ 445: Q67000–J298

FLJ 441 – 74164
FLJ 445 – 84164

8-Bit Shiftregister, Parallel out

The FLJ 441/445 accept data at the serial inputs A and B and shift the data during the rising edge of the clock pulse. The information is available in parallel at the outputs Q_A through Q_H. Applications: storage element, serial-parallel-converter up to clock frequencies of 36 MHz typically.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{OH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=8 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	9		27.5	mA
Supply current C=L	I_{SL}	V_S=5.25 V		30		mA
C=H	I_{SH}	V_S=5.25 V		37	54	mA

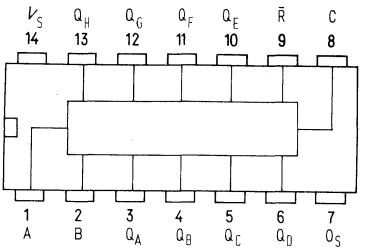
Delay times, V_S=5 V, T_A=25 °C, F_Q=5

Maximum clock frequency	f	C_L=15 pF, R_L=800 Ω	25	36		MHz
Clock pulse duration	t_{pC}		20			ns
Setup time	t_S		15			ns
Hold time	t_H		0			ns
Propagation delay						
from $\overline{R}$ to Q	t_{PHL}	C_L=15 pF, R_L=800 Ω		24	36	ns
	t_{PHL}	C_L=50 pF, R_L=800 Ω		28	42	ns
from C to Q	t_{PLH}	C_L=15 pF, R_L=800 Ω	8	17	27	ns
	t_{PLH}	C_L=50 pF, R_L=800 Ω	10	20	30	ns
from C to Q	t_{PHL}	C_L=15 pF, R_L=800 Ω	10	21	32	ns
	t_{PHL}	C_L=50 pF, R_L=800 Ω	10	25	37	ns

Logical data

Output load factor H-signal	F_{QH}		10	
L-signal	F_{QL}		5	
Input load factor, each input	F_I		5	

FLJ 441
FLJ 445



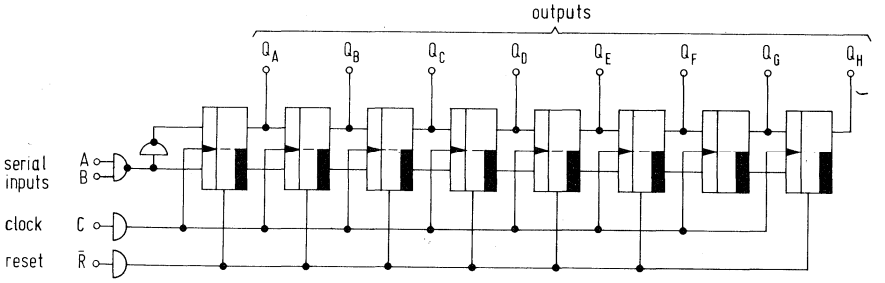
Pin configuration
top view

Truth table

serial inputs at t_n		outputs at t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

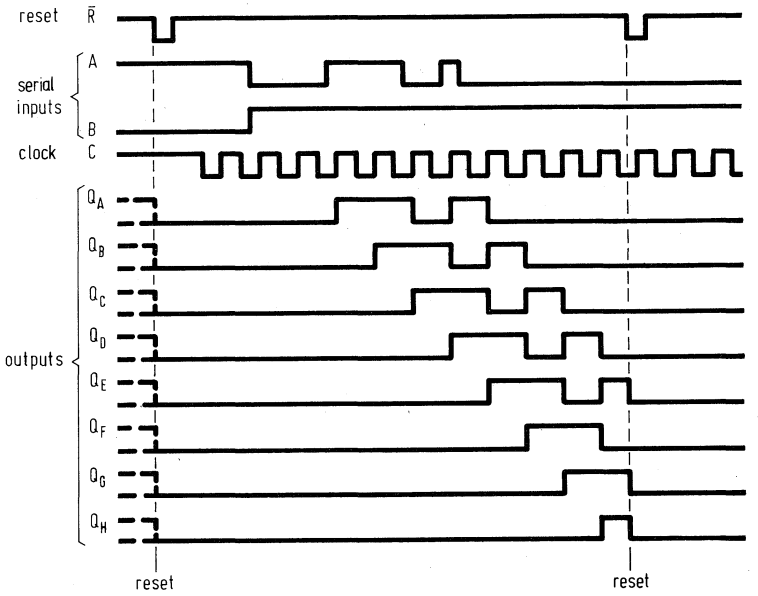
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

block diagram



Pulse diagram

For reset, inhibit, and shift operation



FLJ 451 – 74165
FLJ 455 – 84165

order numbers

FLJ 451: Q67000–J281
FLJ 455: Q67000–J299

8-Bit Shiftregister, Parallel in

The shiftregisters FLJ 451/455 accept parallel data from the input A through H independent of the clock pulse while set input $\bar{S}$ is at L-level. An H-level at $\bar{S}$ enables the serial input J. Data is accepted at the succeeding clock pulse. The information is supplied serially at the output Q_H.
An H-signal at the enable input E_I inhibits the clock input.
Applications: storage element, parallel-serial-converter.

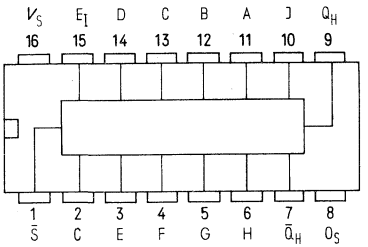
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5,5 V			1	mA
H-input current at $\bar{S}$	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			80	µA
remaining inputs	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current at $\bar{S}$	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4V			3.2	mA
remaining inputs	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4V			1.6	mA
Short circuit output current	$-I_Q$	V_S=5.25 V	18		55	mA
Supply current	I_S	V_S=5.25 V		42	63	mA

Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Maximum clock frequency	f	C_L=15 pF, R_L=400 Ω	20	26		MHz
Clock pulse duration	t_{pC}		25			ns
Set pulse duration	t_{pS}		15			ns
Setup time						
at enable input E_I	t_S		30			ns
at parallel inputs A to H	t_S		10			ns
at serial input J	t_S		20			ns
at set input $\bar{S}$	t_S		45			ns
Hold time	t_H		0			ns
Propagation delay						
from $\bar{S}$ to any output	t_{PLH}			21	31	ns
	t_{PHL}			27	40	ns
from C to any output	t_{PLH}	C_L=15 pF, R_L=400 Ω		16	24	ns
	t_{PHL}	C_L=15 pF, R_L=400 Ω		21	31	ns
from H to output Q	t_{PLH}			11	17	ns
	t_{PHL}			24	35	ns

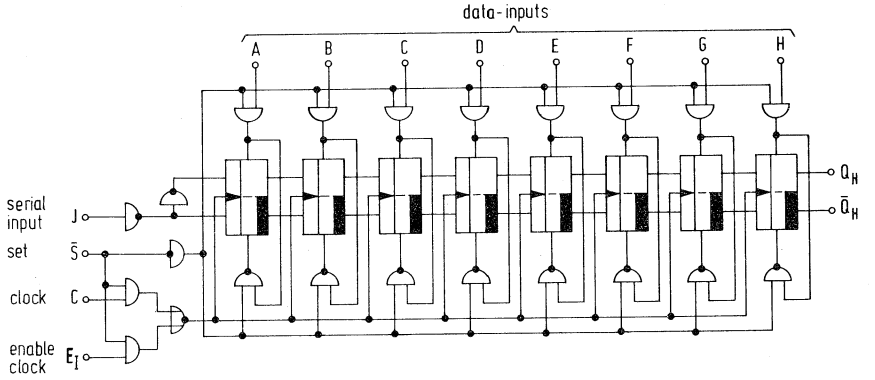
Logical data

Output load factor H-signal	F_{QH}		20	
L-signal	F_{QL}		10	
Input load factor at $\bar{S}$	F_I		2	
remaining inputs	F_I		1	

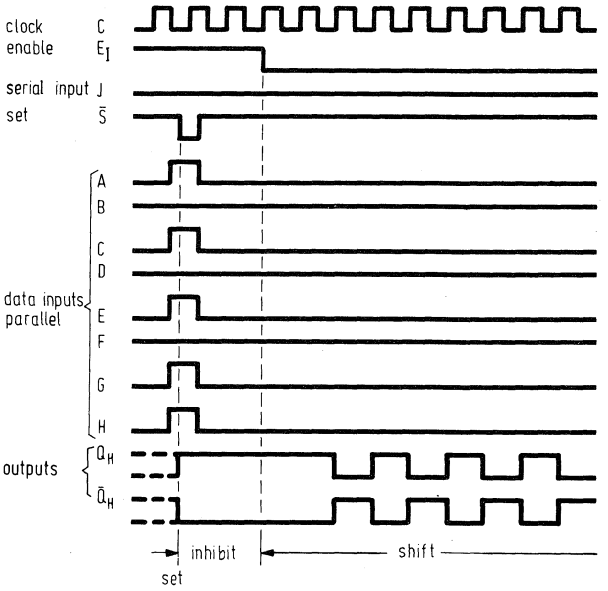


Pin configuration
top view

Block diagram



Pulse diagram



■ Not for new development.

List of sales organisations and representatives

■ Not for new development.

Type designation code for integrated circuits

The type designation code is composed as follows:

Analog	T		AA 15	1	S
Digital	FL	H	10	5	
	family designation	function	number	temperature	version

The family designation runs: FL, FZ, GD, etc.
Solitary digital types are designated SA, SB, etc, and mixed analog digital types UA, UB, etc.

The function letter indicates:

H combinatorial logic
J sequential logic (static)
K monostable circuit
L level converter
N sequential logic (dynamic)
Q read-write memory
R read-only memory
S sense amplifier with digital output
Y miscellaneous

The serial number runs from 10 to 99.

The version letter indicates that these circuits differ electrically or mechanically from the original type (e. g. TAA 151: V_S = 7 V and TAA 151 S: V_S = 12 V).

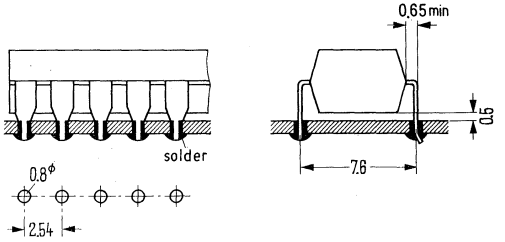
The temperature code number gives the ambient temperature range as follows:

code number	temperature range
0	range not indicated
1	0 to 70 °C or wider
2	—55 to 125 °C or wider
3	—10 to 85 °C or wider
4	15 to 55 °C or wider
5	—25 to 70 °C or wider
6	—40 to 85 °C or wider

General mounting instructions

1. Plastic dual-in-line package

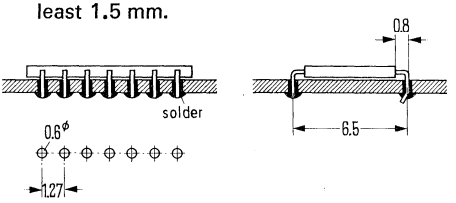
Plastic packages are soldered on the side of the printed circuit board opposite to the case, the pins are vertically bent and fit into holes at an equal distance of 7.6 × 2.54 mm and a diameter of 0.7 to 0.9 mm.
The distance between the package and the printed circuit board is determined by shoulders (see picture).
After inserting the package into the printed circuit board two or more pins should be bent at an angle of app. 30 °C. Thus the package need not be held down while soldering.
The maximum allowable solder times are with iron soldering 265 °C (max. 10s) and with dip soldering 240 (max. 4s).



2. Flat package

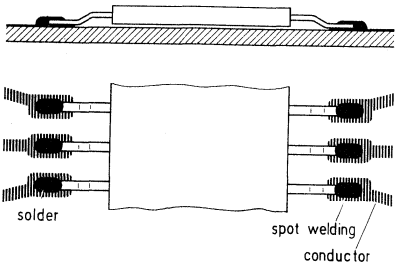
a) Soldering on the side of the printed board opposite to the case.
After bending the leads vertically the case is inserted into holes of 0.6 to 0.8 mm diameter in the printed circuit board. The distance of the bend from the case may not be below 0.8 mm (see picture 1).
After inserting the case into the printed circuit board two or more leads should be bent at an angle of app. 30 °C (see picture 1). Thus the case need not be held down while soldering. The leads should be clipped before soldering.
Iron or dip soldering may be applied.
Solder time $t_{max} \leqq 2$ s at a solder temperature $T = 300$ °C, and $t_{max} \leqq 5$ s at $T = 250$ °C.

b) Connection on the case side of the printed circuit board.
In this case no holes are necessary. The leads are connected to the printed circuit by iron soldering or spot welding.
Solder time $t_{max} \leqq 7$ s at a solder temperature $T = 350$ °C, $t_{max} \leqq 12$ s at $T = 300$ °C, and $t_{max} \leqq 15$ s at $T = 250$ °C whereby the minimal soldering distance from the case must be at least 1.5 mm.



bending radius 0.1 mm

picture 1



picture 2

3. TO 5 and similar cases with 8, 10, and 12 pins

The position of the case is arbitrary. The pins may be bent up to a minimal distance of 1.5 mm from the case. The hole diameter must be 0.5 to 0.6 mm.
The pins should be clipped before soldering.
Iron or dip soldering may be applied.

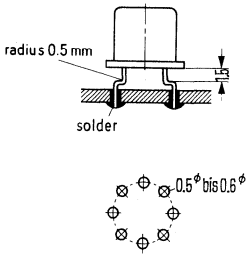
The maximum solder times are with dip soldering:

t_{max} = 5 s for 250 °C solder temperature
t_{max} = 4 s for 300 °C solder temperature

and with iron soldering

t_{max} = 15 s for 250 °C iron temperature
t_{max} = 12 s for 300 °C iron temperature
t_{max} = 8 s for 350 °C iron temperature (not valid for MOS-circuits)

With MOS-circuits particular care has to be taken that no currents flow from iron and solder bath respectively to the printed circuit board. It is therefore recommended to ground the circuit connections to be soldered, the iron and solder bath respectively.
The MOS-circuits must be protected from static charges during preparation and insertion into the printed circuit board. The MOS-circuits may by no means taken out or inserted into the printed circuit board while the supply voltage is on.



Glossary of Terms

1. For digital integrated circuits except MOS-circuits

b	pulse duration
B	bandwidth
f	frequency
F_I	input load factor
F_O	output load factor
F_{OH}	H-output load factor
F_{OL}	L-output load factor
I_I	input current
I_{IH}	H-input current
I_{IL}	L-input current
I_{N1}, I_{N2}	input current of a node
I_O	output leakage current, output short circuit current
I_{OH}	H-output current
I_{OL}	L-output current
I_{SH}	H-supply current
I_{SL}	L-supply current
P	power consumption
R_L	collector load resistor, load resistor
T_{amb}	ambient temperature
t_d	pulse delay time
t_H	hold time
t_I	input pulse duration
t_n	bit time before clock pulse
t_{n-1}	bit time after clock pulse
t_P	average propagation delay
t_{PD}	pair delay
t_{PHL}	propagation delay from H to L
t_{PLH}	propagation delay from L to H
t_{pR}	reset pulse duration
t_{pS}	set pulse duration
t_{pC}	clock pulse duration
t_O	output pulse duration
t_{THL}	fall time from H to L
t_{TLH}	rise time from L to H
T_S	storage temperature
t_S	setup time
t_{SH}	H-setup time
t_{SHI}	H-setup time, left shift
t_{SHr}	H-setup time, shift right
t_{SL}	L-setup time
t_{SLI}	L-setup time, left shift
t_{SLr}	L-setup time, right shift
V_{BE}	base-emmitter voltage
V_I	input voltage
V_{IH}	H-input voltage
V_{IL}	L-input voltage
V_{nm}	DC-noise margin
V_{nv}	noise voltage
V_O	output voltage

V_{QH}	H-output voltage
V_{QL}	L-output voltage
$\overline{V_{QH}}$, $\overline{V_{QL}}$	complementary output voltage
V_S	supply voltage

2. For analog integrated circuits

Comparison Tables for Integrated Circuits

1. Digital integrated circuits

Type No.	Manufacturer	Siemens Type No.	Type No.	Manufacturer	Siemens Type No.
SN 4929 N	TI	FLH 251	SN 7442 N	TI	FLH 281
SN 4930 N	TI	FLH 321	SN 7443 N	TI	FLH 361
SN 4931 N	TI	FLH 331	SN 7444 N	TI	FLH 371
SN 4932 N	TI	FLJ 481	SN 7445 N	TI	FLL 111
SN 4934 N	TI	FLH 461	SN 7446 N	TI	FLL 121
SN 4935 N	TI	FLH 471	SN 7446 AN	TI	FLL 121 U
SN 49700 N	TI	FLL 131	SN 7447 N	TI	FLL 121 T
SN 49701 N	TI	FLL 141	SN 7447 AN	TI	FLL 121 V
SN 49702 N	TI	FLJ 491	SN 7448 N	TI	FLH 551
SN 49700 NS1	TI	FLL 131 T	SN 7450 N	TI	FLH 151
SN 49703 N	TI	FLH 641	SN 7451 N	TI	FLH 161
SN 49704 N	TI	FLJ 501	SN 7453 N	TI	FLH 171
SN 49705 N	TI	FLJ 511	SN 7454 N	TI	FLH 181
SN 7400 N	TI	FLH 101	SN 7460 N	TI	FLY 101
SN 7401 N	TI	FLH 201	SN 7470 N	TI	FLJ 101
SN 7401 NS1	TI	FLH 201 S	SN 7472 N	TI	FLJ 111
SN 7401 NS3	TI	FLH 201 T	SN 7473 N	TI	FLJ 121
SN 7402 N	TI	FLH 191	SN 7474 N	TI	FLJ 141
SN 7402 NS1	TI	FLH 191 S	SN 7475 N	TI	FLJ 151
SN 7403 N	TI	FLH 291	SN 7476 N	TI	FLJ 131
SN 7403 NS1	TI	FLH 291 S	SN 7480 N	TI	FLH 221
SN 7403 NS3	TI	FLH 291 T	SN 7481 N	TI	FLQ 111
SN 7404 N	TI	FLH 211	SN 7482 N	TI	FLH 231
SN 7405 N	TI	FLH 271	SN 7483 N	TI	FLH 241
SN 7405 NS1	TI	FLH 271 S	SN 7484 N	TI	FLQ 121
SN 7405 NS3	TI	FLH 271 T	SN 7485 N	TI	FLH 431
SN 7406 N	TI	FLH 481	SN 7486 N	TI	FLH 341
SN 7407 N	TI	FLH 491	SN 74 H 87 N	TI	FLH 441
SN 7408 N	TI	FLH 381	SN 7488 N	TI	FLR 101
SN 7409 N	TI	FLH 391	SN 7489 N	TI	FLQ 101
SN 7410 N	TI	FLH 111	SN 7490 N	TI	FLJ 161
SN 7411 N	TI	FLH 581	SN 7490 NS1	TI	FLJ 161 S
SN 7412 N	TI	FLH 501	SN 7491 AN	TI	FLJ 221
SN 7413 N	TI	FLH 351	SN 7492 N	TI	FLJ 171
SN 7415 N	TI	FLH 591	SN 7493 N	TI	FLJ 181
SN 7416 N	TI	FLH 481 T	SN 7494 N	TI	FLJ 231
SN 7417 N	TI	FLH 491 T	SN 7495 N	TI	FLJ 191
SN 7420 N	TI	FLH 121	SN 7496 N	TI	FLJ 261
SN 7422 N	TI	FLH 611	SN 7497 N	TI	FLJ 331
SN 7423 N	TI	FLH 511	SN 74100 N	TI	FLJ 301
SN 7425 N	TI	FLH 521	SN 74104 N	TI	FLJ 281
SN 7426 N	TI	FLH 291 U	SN 74105 N	TI	FLJ 291
SN 7427 N	TI	FLH 621	SN 74107 N	TI	FLJ 271
SN 7430 N	TI	FLH 131	SN 74110 N	TI	FLJ 341
SN 7437 N	TI	FLH 531	SN 74111 N	TI	FLJ 351
SN 7438 N	TI	FLH 541	SN 74115 N	TI	FLJ 521
SN 7440 N	TI	FLH 141	SN 74118 N	TI	FLJ 361

Type No.	Manufac-turer	Siemens Type No.	Type No.	Manufac-turer	Siemens Type No.
SN 74119 N	TI	FLJ 371	SN 74167 N	TI	FLJ 471
SN 74121 N	TI	FLK 101	SN 74170 N	TI	FLQ 131
SN 74122 N	TI	FLK 111	SN 74174 N	TI	FLJ 531
SN 74123 N	TI	FLK 121	SN 74175 N	TI	FLJ 541
SN 74132 N	TI	FLH 601	SN 74180 N	TI	FLH 421
SN 74141 N	TI	FLL 101	SN 74181 N	TI	FLH 401
SN 74142 N	TI	FLL 151	SN 74182 N	TI	FLH 411
SN 74145 N	TI	FLL 111 T	SN 74 H 183 N	TI	FLH 451
SN 74150 N	TI	FLY 111	SN 74184 N	TI	FLH 561
SN 74151 N	TI	FLY 121	SN 74185 AN	TI	FLH 571
SN 74153 N	TI	FLY 131	SN 74187 N	TI	FLR 111
SN 74154 N	TI	FLY 141	SN 74190 M	TI	FLJ 201
SN 74155 N	TI	FLY 151	SN 74191 N	TI	FLJ 211
SN 74156 N	TI	FLY 161	SN 74192 N	TI	FLJ 241
SN 74157 N	TI	FLY 171	SN 74193 N	TI	FLJ 251
SN 74160 N	TI	FLJ 401	SN 74194 N	TI	FLJ 551
SN 74161 N	TI	FLJ 411	SN 74195 N	TI	FLJ 561
SN 74162 N	TI	FLJ 421	SN 74196 N	TI	FLJ 381
SN 74163 N	TI	FLJ 431	SN 74197 N	TI	FLJ 391
SN 74164 N	TI	FLJ 441	SN 74198 N	TI	FLJ 311
SN 74165 N	TI	FLJ 451	SN 74199 N	TI	FLJ 321
SN 74166 N	TI	FLJ 461	SN 74200 N	TI	FLQ 141

The series SN 8400 N corresponds to the Siemens series FL 105. The desired type number is derived from the series SN 7400 N.
E. g. SN 8401 N = FLH 205 etc.

TI = Texas Instruments

Other suppliers of the 74-series use identical numbers with different prefix.
E. g. DM 7400 National Semiconductor
N 7400 Signetics

Type No.	Manufac-turer	Siemens Type No.
MOS-circuits		
MEM 1000	GI	GDH 146
MEM 1002	GI	GDH 116
MEM 1008	GI	GDH 136
MEM 1013	GI	GDH 126
MEM 1014	GI	GDH 106
MEM 1015	GI	GDJ 106
MEM 1055	GI	GDJ 116
MEM 2048	GI	GDR 106
MEM 3005 PP	GI	GRJ 126
MEM 3008 PS	GI	GDJ 136
MEM 3012 SP	GI	GDJ 146
MEM 3016-2	GI	GDJ 156
MEM 3021	GI	GDJ 186
MEM 3032	GI	GDJ 166
MEM 3064 S	GI	GDJ 176
MEM 3064 B	GI	GDN 116
MEM 3100 A	GI	GDN 106
MEM 3128	GI	GDN 126
RA-6-4803	GI	GEJ 102
SS-6-8212	GI	GEJ 112
EA 1204 pL 5 R 256	GI	FDN 141 A
EA 1205 pL 5 R 256	GI	FDN 151 A
1101, 11011	GI	GDQ 101
RO-1-2048	GI	GDR 101-1000
RO-1-2240	GI	GDR 101-2000
EA-3001	GI	GDR 101-3000

Type No.	Manufac-turer	Siemens Type No.
Analog integrated circuits		
MC 1709 CG	Mot	TAA 521
MC 1709 CL	Mot	TAA 521 A
MC 1709 G	Mot	TAA 522
MC 1741 CG	Mot	TBA 221
MC 1741 G	Mot	TBA 222
OM 200	V	TAA 131
SN 5510 L	TI	TAA 722
SN 7510 L	TI	TAA 721
SN 72709 L	TI	TAA 521
SN 72709 N	TI	TAA 521 A
SN 52709 L	TI	TAA 522
SN 72741 L	TI	TBA 221
SN 52741 L	TI	TBA 222
TAA 263	V	TAA 141
TAA 293	V	TAA 151
TAA 380	Ph	(TBA 120)
TAA 450	Ph	(TBA 120)
TAA 570	Ph	(TBA 120)
TAA 640	Ph	(TBA 120)
TAA 661	SGS	(TBA 120)
TAA 710	ITT	(TBA 120)
TOA 2709 V	TEC	TAA 521
TOA 2709 P	TEC	TAA 521 A
TOA 1709 V	TEC	TAA 522
TOA 2741 V	TEC	TBA 221
TOA 1741 V	TEC	TBA 112
µA 709	FSC	TAA 522
µA 709 C	FSC	TAA 521
µA 741	FSC	TBA 222
µA 741 C	FSC	TBA 221

GI = General Instrument
Mot = Motorola
V = Valvo
TI = Texas Instrument
Ph = Philips
TEC = Transitron
FSC = Fairchild

Digital Integrated Circuits

General Information on Digital Integrated Circuits

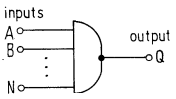
I. Logic Data and Symbols

1. Logic Levels

According to DIN 41785, sheet 4 for digital microcircuits the two possible values of binary electrical digits are given by L (Low) and H (High). The values of the L-range are defined as closer to $-\infty$, and the values of the H-range as closer to $+\infty$.
The logic symbols 0 and 1, or **O** and **L**, or log. 1 and log. 0 as well as positive or negative logic definitions are not used any longer.

2. Gate Symbols

2.1 NAND-Gate

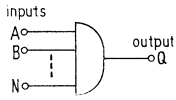


Truth table for a 2-input NAND-gate
(e. g. 1/4 FLH 101)

inputs A	B	output Q
L	L	H
L	H	H
H	L	H
H	H	L

Logic function: $Q = \overline{AB \ldots . N}$
Definition: An output signal will be present unless A and B and .... and N are pesent.

2.2 AND-Gate

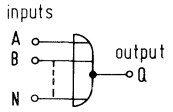


Truth table for a 2-input AND-gate
(e. g. 1/4 FLH 381)

inputs A	B	output Q
L	L	L
L	H	L
H	L	L
H	H	H

Logic function: $Q = AB \ldots . N$
Definition: An output signal will be present if A and B and .... and N are present.

2.3 NOR-Gate



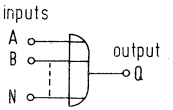
Truth table for a 2-input NOR-gate
(e. g. 1/4 FLH 191)

inputs A	B	output Q
L	L	H
L	H	L
H	L	L
H	H	L

Logic function: $Q = \overline{A + B + ... + N}$

Definition: An output signal will be present if A or B or .... or N are not present.

2.4 OR-Gate



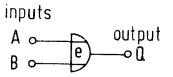
Truth table for a 2-input OR-gate
(e. g. 1/4 FLH 631)

inputs A	B	output Q
L	L	L
L	H	H
H	L	H
H	H	H

Logic function: $Q = A + B + ... + N$

Definition: An output signal will be present if A or B or .... or N are present.

2.5 Exclusive-OR-Gate



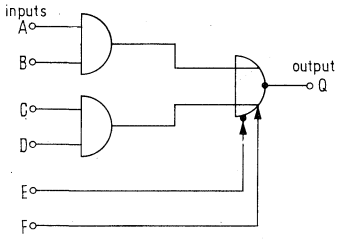
Truth table for a 2-input exclusive-OR-gate
(e. g. 1/4 FLH 341)

inputs A	B	output Q
L	L	L
L	H	H
H	L	H
H	H	L

Logic function: $Q = A\bar{B} + \bar{A}B$

Definition: An output signal will be present if only A or only B is present.

2.6 AND/OR-Gate, inverting



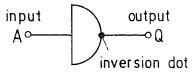
Truth table for a 2 + 2-input AND/OR-gate (e. g. 1/2 FLH 151)

inputs A	B	C	D	output Q
L	L	L	L	H
H	L	L	L	H
L	H	L	L	H
H	H	L	L	L
L	L	H	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	L	L
L	L	L	H	H
H	L	L	H	H
L	H	L	H	H
H	H	L	H	L
L	L	H	H	L
H	L	H	H	L
L	H	H	H	L
H	H	H	H	L

N_1 and N_2 are expander nodes. Additional AND/OR-functions can be realized with an expander connected to N_1 and N_2 .

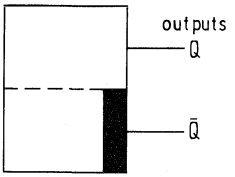
Logic function: $Q = \overline{AB + CD + \text{exp.}}$

2.7 Inverter

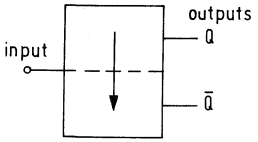


Logic function: $Q = \overline{A}$

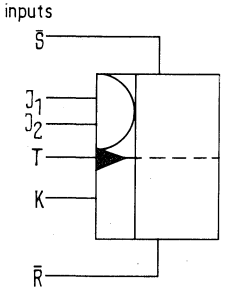
3. Flipflop Symbols



bistable circuit (flipflop) with defined output state (complementary outputs)

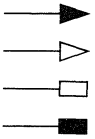


monostable circuit (monoflop) with an input acting upon both outputs. The arrow indicates the output which is high when the circuit is stable.



J_1 J_2 and K are information inputs
J_1 and J_2 are AND-connected
J and K-inputs are gated by clock input C
$\bar{R}$ and $\bar{S}$ are independent reset and set inputs

The arrow at the clock input shows the gating mode as follows:



action at the output occurs when the input rises from L to H
action at the output occurs when the input falls from H to L
action while the input is high
action while the input is low

4. Flipflop Classification according to the Logic Function

4.1 D-Flipflop (Delay-Flipflop)

The D-flipflop has an input (indicated with a D) the logic state of which is transferred into the flipflop. It is controlled by a clock pulse. The information stored during the clock pulse is retained until the next clock pulse. Only then any new information is accepted by the D-input.

4.2 JK-Flipflop

The JK-flipflop has information inputs indicated with a J and K. They are gated by the clock input and determine the output state Q of the flipflop.
At J = L and K = L the Q-output is retained in its original state. At J = H and K = H the flipflop switches at every clock pulse to its complementary state (binary divider). Q = L results at J = L and K = H independent of the preceding output state. For J = H and K = L the defined output state is Q = H.
Most JK-flipflops have additional $\bar{R}$ and $\bar{S}$ inputs with which the flipflop can be operated independent of the clock pulse. In this way it is possible to select the initial state of the flipflop. $\bar{R}$ and $\bar{S}$ indicates that set or reset action is at L-level only.
The following tables show the function of the different types of flipflops.

4.3 Truth Tables for Flipflops

inputs		output Q	
D or J	K	D-Flipflop	JK-Flipflop
L	L	L	Q_n
L	H		L
H	L	H	H
H	H		$\bar{Q}_n$
t_n		t_{n+1}	

inputs		outputs	
$\bar{R}$	$\bar{S}$	Q	$\bar{Q}$
L	H	L	H
H	L	H	L
L	L	undefined	
H	H	Q_n	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

II. General Information on Quality Levels of Digital Integrated Circuits

1. The quality of integrated circuits of the TTL, LSL, and ECL-series are defined by the following statements:

1.1 Maximum ratings as well as upper and lower distribution boundary of typical characteristics.

1.2 Maximum amount of circuits which do not comply with the ratings given under 1.1. These acceptable quality levels or AQL-levels are based on final production testing in accordance with the AQL-table ABC-STD-105 D, inspection level II (see also paragraph II. 4).

2. Defects

A defect is indicated if an actual value measured does not correspond to the data sheet. The defects are classified into type and extent.

2.1 Type of defect
- A Mechanical defects of case and connections
- B Electrical defects

2.2 Extent of defect
- A Critical defects: any defect causing functional failure.
- B Gradual defects: defects which still permit functional applications.

3. The defects and the corresponding AQL-values are stated in the table below.

defect	AQL-levels for: TTL	LSL	ECL	note
3.1 Mechanical defect	0.65	0.65	0.65	1
A Critical defect	0.25	0.25	0.25	1
B Gradual defect	0.65	0.65	0.65	1
3.2 Electrical defects	1.0			1
3.2.1 Static parameters of data sheet within the temperature range	0.65 or 0.1	1.0	0.65	1, 4, 2
A Critical defects	0.15	0.15	0.25	1, 2
B Gradual defects	0.65	1.0	0.65	1, 2
3.2.2 Switching parameters at 25 °C	1.0	1.5	0.65	3

Notes: 1 group-AQL = sum of defects of all parameters
2 TTL-circuits are available with AQL = 0.1 at a small surcharge on request
3 AQL for TTL and LSL = defect of a single parameter; group-AQL for ECL
4 valid for LSL and ECL at 25 °C

4. Incoming Inspection

Test procedures at the manufacturer's are intended to make incoming inspection unnecessary. If the buyer still requires inspection, it is recommended to use test procedures in accordance with AQL-table ABC-STD-105 D.

General Information on the TTL-Series FL 100

1. Description of the Static Characteristics

1.1 Maximum Ratings

The maximum ratings stated in the data sheets are absolute limits which must be observed. The integrated circuit may be destroyed if a single value is exceeded.
Maximum ratings are valid at 25 °C unless noted otherwise.

1.2 Electrical Characteristics

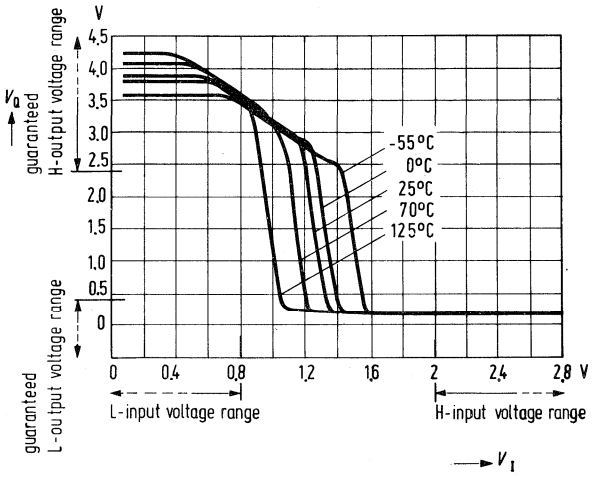
The electrical characteristics are defined by typical values which result from a statistical analysis of a determined manufacturing period. These typical values are valid at T_A = 25 °C and recommended supply voltage V_S. Typical values are mostly supplemented by distribution boundaries under worst-case conditions. Furthermore it is important to notice that the logic parameters V_I and V_Q are referred to input and output respectively.

1.3 Characteristic Functions

The characteristic functions define the typical operating conditions of a circuit. The most important characteristic functions of typical TTL-gates of the FL 100 series are compiled in the following.

1.3.1 Transfer function

The transfer function of a gate shows the output voltage as a function of the input voltage.



test circuit

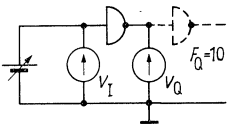


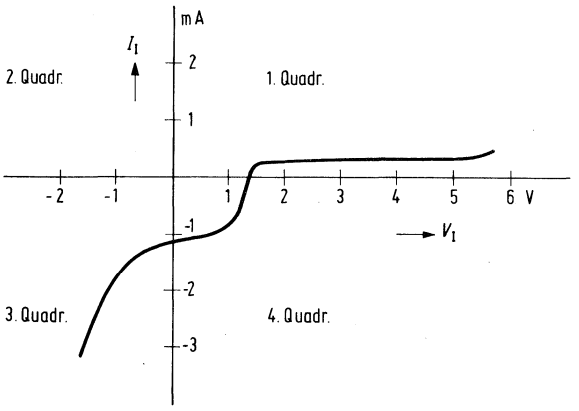
Fig. 1 Transfer function of a NAND-gate: $V_Q = f(V_I)$ at F_Q = 10 and V_S = 5 V

The slope of the transfer function depends on the load and the temperature. All NAND and NOR-gates are characterized by qualitatively similar transfer functions. Unused inputs of NAND-gates must be left open or connected to an H-level. Unused inputs of NOR-gates must be supplied with an L-level. The magnitudes of the typical logic levels as well as the noise margin can be derived from the transfer function.

1.3.2 Input characteristic

The input characteristic defines input current and voltage.

Figure 2 shows the typical input characteristic of a gate at room temperature. The input characteristic is devided into 3 ranges by the corresponding quadrants. The 1st quadrant characterises the H-range. The input transistor is reverse biased. The typical breakdown voltage of the base-emitter-region is approximately 8 to 9 V. To ensure safe operation the maximum input voltage is limited to V_I = + 5.5 V. This voltage is an absolute limit between any input and ground as well as between two inputs of the same gate.



test circuit

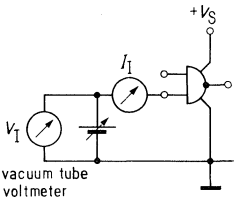
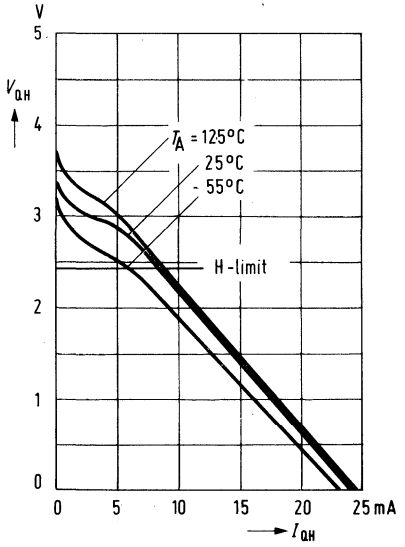


Fig. 2 Input characteristic of a gate input $I_I = f(V_I)$ at V_S = 5 V

The input current of 10 μA typically flows into the input (reverse current).
The input transistor starts conducting at a threshold voltage of $V_I \sim 1.5$ V. The input current reverses its direction. The input transistor is now foreward biased (4th quadrant). The substrate diode starts conducting at negative input voltages. The input current increases rapidly (3rd quadrant). In order not to exceed the total power dissipation of a gate (approx. 0.5 W per package), DC-input voltages are limited to $-V_I > 1.5$ V and DC-input current to $-I_I > 30$ mA.
The input characteristic is independent of the load as the gate circuit does not include any feedback.

1.3.3 Output characteristics

The output state of a gate is defined by the input condition. Two output characteristics exist for every output, one for the H-state (figure 3) and one for the L-state (figure 4).
The characteristics are functions of the temperature and the load.
If the output is connected to TTL-inputs at H-level relatively small load currents result. The output current required by 10 normalized loads is 400 μA at H-level. The output voltage is reduced by 0.1 V only by this current. The output current I_{QH} is supplied by the gate output.
TTL-outputs are often used to drive loads such as NPN-transistors. The possible base current can be derived from figure 3. If higher currents are required, the power gate FLH 141 must be used.



test circuit

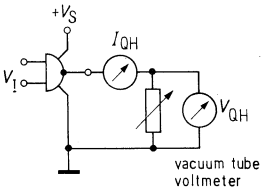
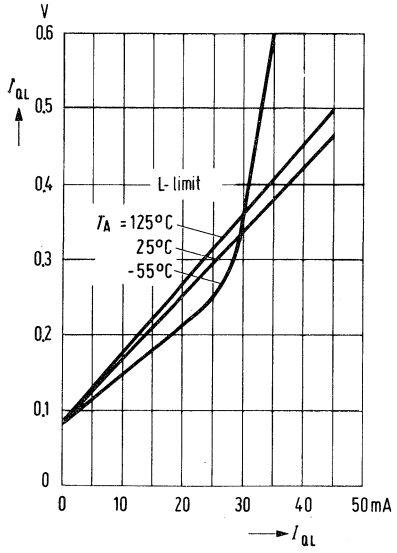


Fig. 3 Output characteristic of the H-state of a gate output $V_{QH} = f(I_{QH})$ at $V_I = 0.4$ V and $V_S = 5$ V.

The L-current is sunk by the gate output, i.e. I_{QL} becomes negative. The guaranteed output voltage is $V_{QL} < 0.4$ V (L-limit) at an output current of 16 mA. The typical input current can be derived from the input characteristic figure 2 with 1 mA. If 10 inputs are connected to an output a typical output voltage of $V_{QL} = 0.2$ V results according to figure 4.
An output can sink more current at L-state than it can supply at H-state. If high drive currents are required, it is therefore more advantageous to use a PNP-transistor stage. A base current of up to 16 mA is thus possible at each output. Drive currents up to 48 mA per output can be realized with the power gate FLH 141.



test circuit

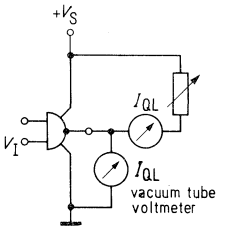


Fig. 4 Output characteristic of the L-state of a gate output $V_{QL} = f(I_{QL})$ at $V_I = 2.4$ V and $V_S = 5$ V.

1.4 Logical Data

1.4.1 Input load factor

The input load factor defines the currents required by a single input at H-state as well as L-state. The upper limit of the L-input current per input is 1.6 mA at 0.4 V. The upper limit of the H-input current per input is 40 μA at 2.4 V. These values define the normalised load factor $F_I = 1$. They are valid within the entire operating temperature range.
$F_I = 3$ means for example an L-input current of $-I_{IL} = 3 \times 1.6$ mA = 4.8 mA and an H-input current of $I_{IH} = 3 \times 40$ μA = 120 μA. Input load factors of 2, 3, and more can be found with flipflops (R, S, and C-inputs) and more complex integrated circuits. Load facors have to be observed during circuit layout as the output load factor of the driving output may not be exceeded.

1.4.2 Output load factor

The output load factor defines how many normalized loads $F_I = 1$ can be driven by a single output. Unless otherwise noted, the output load factor is $F_Q = 10$ for standard outputs and $F_Q = 30$ for power outputs. Quite often the H-output load factor is higher than the L-output load factor. In this way it is possible to connect unused inputs of the same gate in parallel without accounting for an additional load.

2. Description of the Dynamic Characteristics

2.1 Propagation Delay and Transition Time

Propagation delay and transition time of the circuits used in a system determine the maximum operational frequency. Capacitive loading of the outputs and long connection lines increase the delay and thus reduce the speed.
The dynamic noise immunity can be derived from the transition time of the output signal. The noise immunity increases with the length of the transition time.
The propagation delay time t_{PLH} is measured between input and output voltage if the output rises from L to H. The propagation delay time t_{PHL} is determined while the output switches from H to L.
Reference points for the propagation delay time are the levels 1.5 V. The transition times t_{TLH} and t_{THL} of the output pulse are measured between the 10% and 90% values.

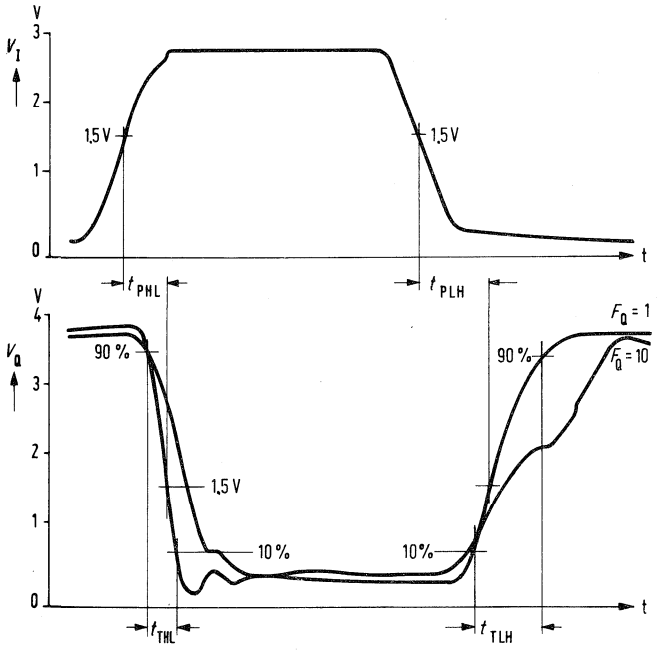


Fig. 5 Switching characteristics of a typical gate at 25 °C

Figures 6 and 7 show typical propagation delay times as a function of the ambient temperature for various capacitive loads at $V_S = 5$ V and $F_O = 10$.

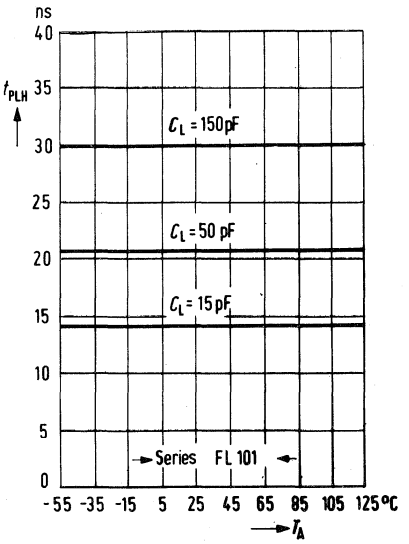


Fig. 6 Propagation delay time $t_{PLH} = f(T_A)$

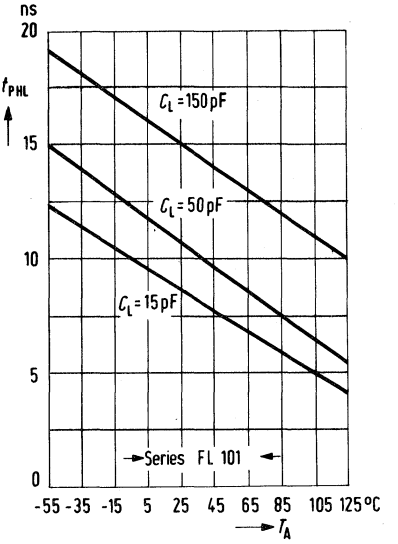


Fig. 7 Propagation delay time $t_{PHL} = f(T_A)$

The average propagation delay time t_p is given by:

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

t_p of a typical FL 100-gate is approximately 10 ns. The average propagation delay time states how much signal delay must be assumed for one gate. Figure 8 shows the average propagation delay as a function of the ambient temperature for various capacitive loads at $V_S = 5$ V.

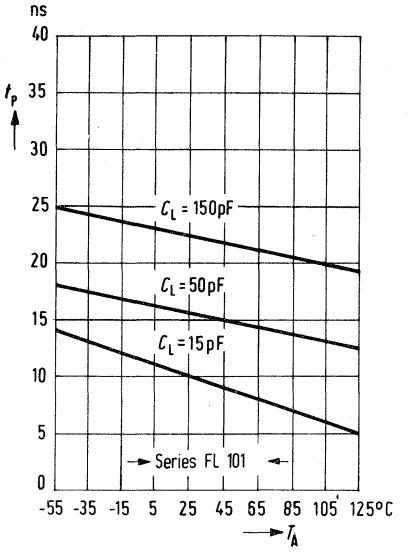


Fig. 8 Average propagation delay time $t_p = f(T_A)$

2.2 Pair-Delay

The pair-delay states the signal delay which is caused by two gates connected in series. The output signal is in phase with the input signal, however delayed by one propagation delay time from H to L plus one propagation delay time from L to H. Thus follows:

$$t_{PD} = t_{PHL} + t_{PLH} = 2\,t_p$$

The pair-delay is directly proportional to the duty cycle of the clock pulse of synchronous systems.

2.3 Conclusions

The transition time exhibits an almost exponential slope. This is due to the time constant being a product of the output resistance and the capacitive load. The slope of the leading edge is steeper than the slope of the trailing edge. This is caused by the output resistance R_{QL} being lower than R_{QH} (approximately 15 Ω compared to 70 Ω).
Any connection line as well as every TTL-input represent a capacitive load. Assuming an approximate input capacitance of 2 pF for each input, a load of 20 pF results at the maximum output loading factor $F_Q = 10$. This is the reason why the transition time is a function of the load factor and the capacitive load respectively.
A capacitive load is charged with a current of approximately 25 mA and discharged with approximately 50 mA.
These current spikes have to be taken into consideration when designing the power supply. The width of the supply and ground lines on the printed circuit board is of particular importance in order to avoid supply voltage transients.
In addition it is recommended to use tantalum buffer capacitors of 1 µF/35 V for every 4 to 6 integrated circuits.
The supply voltage conductors should have a minimum width of 3 mm for boards of 100 x 160 mm. A common ground plane preferably with a mesh structure is most suitable for TTL-circuits due to a very low line inductivity.

3. Noise Immunity

3.1 Static Noise Immunity

The static noise immunity characterizes the behavior of a system disturbed by noise-pulses which last longer than the average propagation delay time. Noise-pulses with transition times much longer than the signal propagation delay time can also be considered to be static noise. The static noise immunity defines the upper limit of a noise voltage which does not influence the logic state of a gate.
The typical values of the static noise immunity or noise margin are derived from the transfer function (figure 1). The lower limit of the H-output voltage is 2.4 V and the upper limit of the L-output voltage is 0.4 V. The typical noise margin results if the difference is formed between the actual output voltages and the threshold voltage V_T required to control a gate input. The following typical values result for the series FL 100 referred to the output at $F_Q = 100$ and $V_S = 5$ V:

H-level: $V_{nmH} = V_{QH} - V_T = 3.9 - 1.3 = 2.6$ V
L-level: $V_{nmL} = V_T - V_{QL} = 1.3 - 0.25 = 1.05$ V

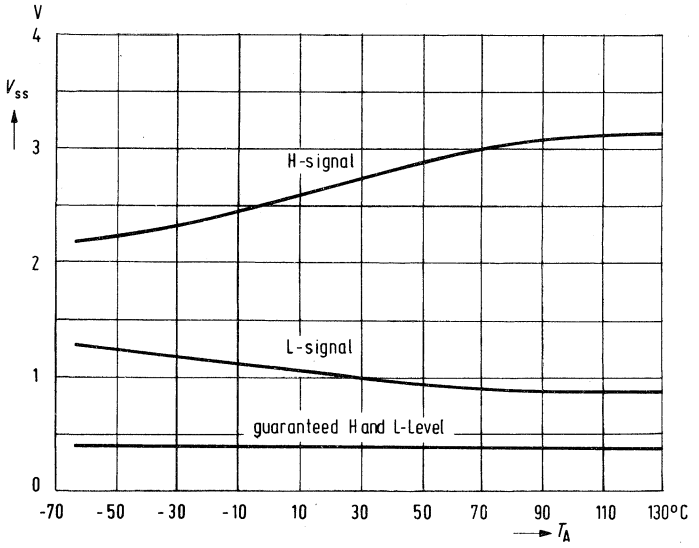


Fig. 9 Noise margin at H and L-level as a function of the ambient temperature

The typical values of the noise margin are affected by the transfer function. Therefore a minimum is guaranteed under worst-case conditions:

H-level: $V_{nmH} = V_{QH} - V_{IH} = 2.4 - 2.0 = 0.4$ V
L-level: $V_{nmL} = V_{IL} - V_{QL} = 0.8 - 0.4 = 0.4$ V

The noise voltage coupled into the conductor path of an output to the input of another gate may be 0.4 V at both logic levels, and no change of state will take place. The guaranteed noise margin of 0.4 V is valid at the maximum output load factor over the full temperature range and an adverse supply voltage variation (worst-case conditions).
Figure 10 shows a level diagramm for a chain of NAND-gates. The corresponding voltage limits from which the guaranteed noise margin is derived is given below.

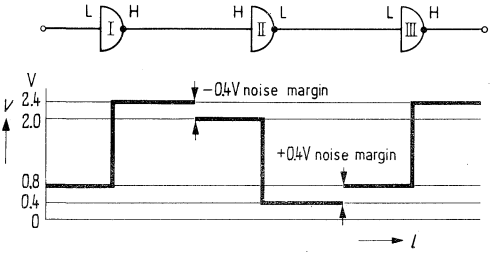


Fig. 10 Guaranteed noise margin

3.2 Dynamic Noise Immunity

The dynamic noise immunity characterizes the behaviour of a system disturbed by noise pulses of a shorter duration than the signal propagation delay time. In this case the energy of the noise pulse — pulse amplitude and duration — determines if a change of the logic state will take place. The practical aspects of the dynamic noise immunity are the input noise immunity and the noise immunity against capacitively coupled noise. The sources of capacitively coupled noise are either cross talk (system noise) or foreign noise.

3.2.1 Input noise immunity

The limits of pulse amplitude and duration of a noise pulse depend on the propagation delay time t_p of a gate. The amplitude of noise-pulses with a duration $b \gg t_p$ may not exceed the static noise margin. The noise amplitude may become greater than the static noise margin at $b < {}^1/_2\, t_p$.

The dynamic noise immunity of a gate is measured by means of an approximately rectangular noise pulse. The time integral of the rectangular pulse is directly proportional to the noise energy. The pulse duration is measured at 1.5 V. Now the noise immunity is examined by means of varying amplitude V_n and duration b of the rectangular noise pulse (figure 11).

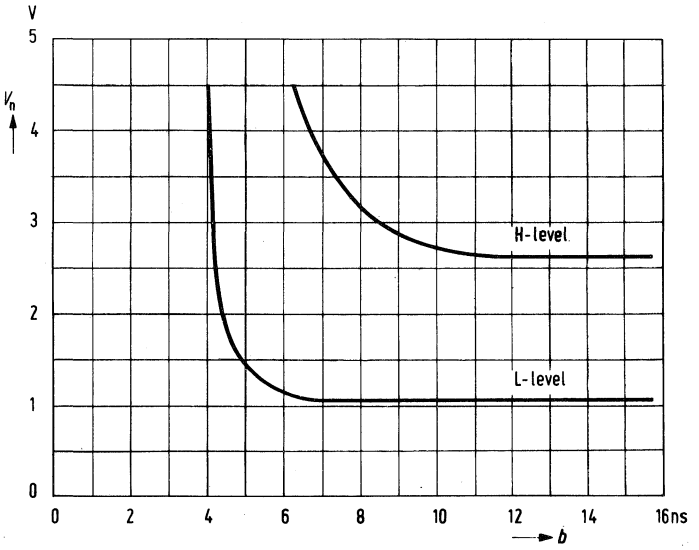


Fig. 11 Typical boundary characteristics of the dynamic noise immunity of gates at $T_A = 25$ °C, $V_S = 5$ V and $F_Q = 10$

The following criterions have to be observed when the dynamic noise immunity is determined. An H-level can only be disturbed by a negative noise pulse and an L-level only by a positive one. The boundary curves indicate that the noise amplitude is relatively high for very short pulses compared with the amplitude of longer lasting noise pulses. The noise amplitude reaches the level of the static noise immunity at a pulse duration approximately equal to the signal propagation delay time. Thus the gate can be compared with a low-pass filter.

3.2.2 Capacitively coupled noise

The push-pull output stage generally used with TTL-circuits has a low output resistance in both logic states ($R_{QL} \sim 15\,\Omega$ and $R_{QH} \sim 70\,\Omega$). This has the advantage that noise-pulses coupled into connection lines of two gates die away rapidly.
Voltages and currents with steep transitions on a signal line influence neighboring conductor paths (cross talk).
Cross talk in a digital system is never an abrupt on and off-function as the resistance of the noise source cannot be neglected.
Figure 12 shows how the noise source is formed by two gates. The amplitude of the noise voltage is thus approximately constant between 3.8 and 4 V as the gate GI' switches only between the L and H-levels. The critical case for a signal line being at H-level exists, when the induced noise voltage changes from H to L, because the output of the gate GI' switches to L-signal.
By varying the capacitance C the noise immunity against capacitive cross talk can be demonstrated. No noise is indicated up to coupling capacitors of 1 nF at H-level.
System cross talk of a signal line being at L-level is so small that it can be regarded as unsignificant.

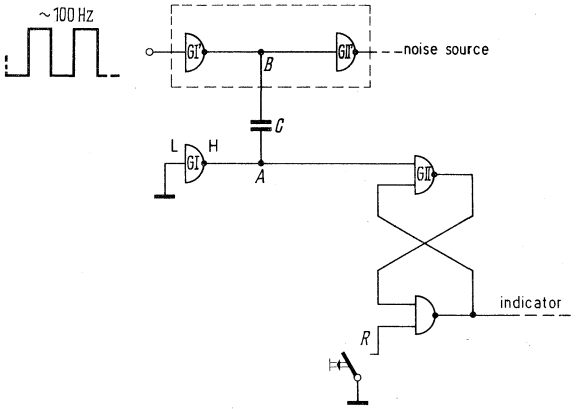


Fig. 12 Circuit to generate and measure system cross talk in short connection lines at H-level

General Information on the TTL-Series FL 100

FL 100 is a series of monolithic integrated circuits. The devices are manufactured by the epitaxial planar process combined with the buried layer technique.

The following Maximum Ratings apply for any Type

		lower limit B	upper limit A	unit
Supply voltage	V_S	–0.5	7.0	V
Input voltage	V_I	–1.5	5.5[1])	V
Differential voltage between 2 inputs	V_I		5.5[1])	V
Output voltage, unless otherwise noted	V_Q	–0.8	5.5[1])	V
Temperature range for FL 101 (range 1)	T_A	0	70	°C
Temperature range for FL 105 (range 5)	T_A	–25	85	°C
Storage temperature	T_S	–65	150	°C

[1]) If these voltage limits cannot be ensured, the corresponding currents must be limited to 1 mA.

Notes

Typical values given in the data sheets refer to V_S = 5 V and T_A = 25 °C. Input and output voltages and currents are always stated per input and output respectively. Not more than one output should be shortened at the same time.
The series FL 100 is available in plastic dual-in-line packages. Outline drawings are at the end of the chapter FL 100.
The series will be continued progressively.

Application notes:

Input signals for gates: Rise and fall times should be below 1 µs, pulse duration greater than 30 ns. Unused inputs can be connected to used inputs of the same gate.
Input signals for flipflops: Edgetriggerd flipflops should have clock pulses with rise and fall times below 250 ns. Shiftregisters and couters employing D-flipflops should have clock pulses with a rise time of at least 25 ns.
Counters and shift registers with master-slave-flipflops require clock-pulses with rise and fall times below 200 ns.
Besides the STANDARD SERIES FL 100 (7400), we supply a HIGH SPEED SERIES (74H00) and a LOW POWER SERIES (74L00). Ceramic dual-in-line packages, flat packages and temperature range –55 to 125 °C is available on request. Please ask your nearest Siemens representative for more information (register see end of book).

FLH 101 – 7400
FLH 105 – 8400

order numbers

FLH 101: Q67000-H1
FLH 105: Q67000-H155

Quadruple 2-input NAND-Gate

Electrical characteristics
temperature ranges 1 and 5

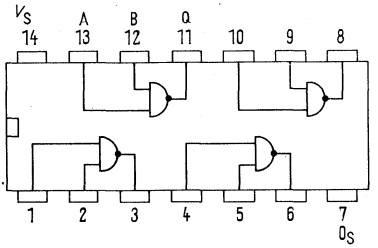
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	2			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=400 µA	2	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA	1		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	3			40	µA
	I_I	V_I=5.5 V | =5.25 V	3			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	4			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	5	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I =0 V	6		4	8	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5 V	6		12	22	mA

Delay times, V_S=5 V, T_A=25 °C

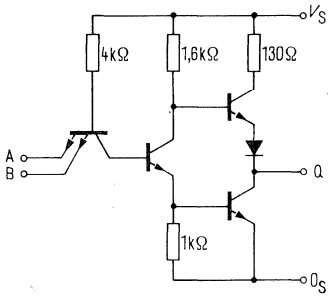
Propagation delay	t_{PHL}	C_1=15 pF, F_Q=10	22		7	15	ns
	t_{PLH}				11	22	ns

Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{AB}$					



Pin configuration
top view



Schematic (each gate)

FLH 111 – 7410
FLH 115 – 8410

order numbers

FLH 111: Q67000–H2
FLH 115: Q67000–H156

Triple 3 Input NAND-Gate

Electrical characteristics
temperature ranges 1 and 5

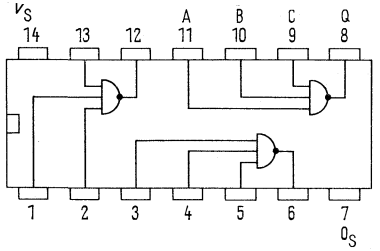
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	2			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V, $-I_{QH}$=400 µA	2	2.4	3.3		V *n*
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA	1		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	3			40	µA
	I_I	V_I=5.5 V | =5.25 V	3			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	4			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	5	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V	6		3	6	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5 V	6		9	16.5	mA

Delay times, V_S=5 V, T_A=25 °C

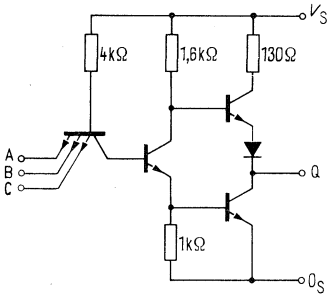
Propagation delay	t_{PHL}	} C_1=15 pF, F_Q=10	22		7	15	ns
	t_{PLH}				11	22	ns

Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{ABC}$					



Pin configuration
top view



Schematic (each gate)

FLH 121 – 7420
FLH 125 – 8420

order numbers

FLH 121: Q67000–H3
FLH 125: Q67000–H157

Dual 4-Input NAND-Gate

Electrical characteristics
temperature ranges 1 and 5

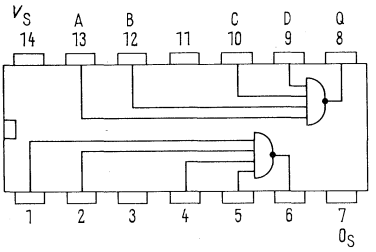
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	2			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=400 µA	2	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA	1		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	3			40	µA
	I_I	V_I=5.5 V | =5.25 V	3			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL} =0.4 V	4			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	5	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V	6		2	4	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5 V	6		6	11	mA

Delay times, V_S=5 V, T_A=25 °C

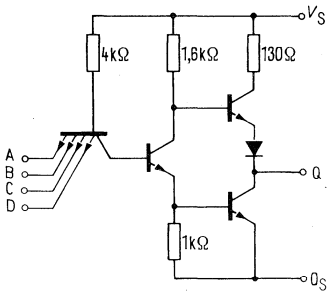
Propagation delay	t_{PHL}	} C_1=15 pF, F_Q=10	22		8	15	ns
	t_{PLH}				12	22	ns

Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{ABCD}$					



Pin configuration
top view



Schematic (each gate)

FLH 131 – 7430
FLH 135 – 8430

order numbers

FLH 131: Q67000–H4
FLH 135: Q67000–H152

8-input NAND-Gate

Electrical characteristics
temperature ranges 1 and 5

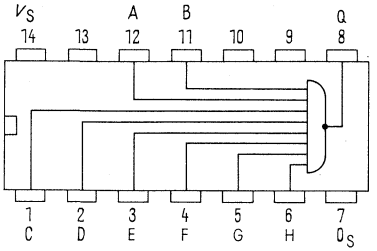
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	2			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IL}=0.8 V, $-I_{QH}$=400 µA	2	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V, V_{QH}=2 V, I_{QL}=16 mA	1		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S=	3			40	µA
	I_I	V_I=5.5 V | 5.25 V	3			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V	4			1.6	mA
Short circuit output current,	I_Q	V_S=5.25 V	5	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V, V_I=0 V	6		1	2	mA
Supply current	I_{SL}	V_S=5.25 V, V_I=5 V	6		3	6	mA

Delay times, V_S=5 V, T_A=25 °C

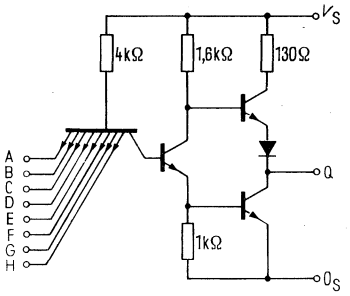
Propagation delay	t_{PHL}	C_l=15 pF, F_Q=10	22		8	15	ns
	t_{PLH}				13	22	ns

Logical Data

Output load factor	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{ABCDEFGH}$					



Pin configuration
top view



Schematic

FLH 141 – 7440
FLH 145 – 8440

order numbers

FLH 141: Q67000–H5
FLH 145: Q67000–H158

Dual 4-input NAND-Powergate

Electrical characteristics
temperature ranges 1 and 5

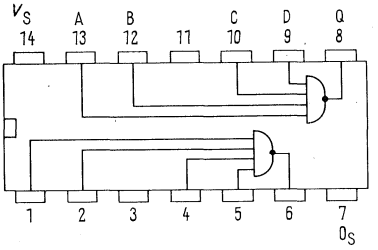
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	2			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=1.2 mA	2	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{QH}=2 V, I_{QL}=48 mA	1		0.28	0.4	V
DC noise margin	V_{nm}			0.4	1		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	3			40	µA
	I_I	V_I=5.5 V | =5.25 V	3			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	4			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	5	18		70	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V	6		2	4	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5 V	6		17	27	mA

Delay times, V_S=5 V, T_A=25 °C

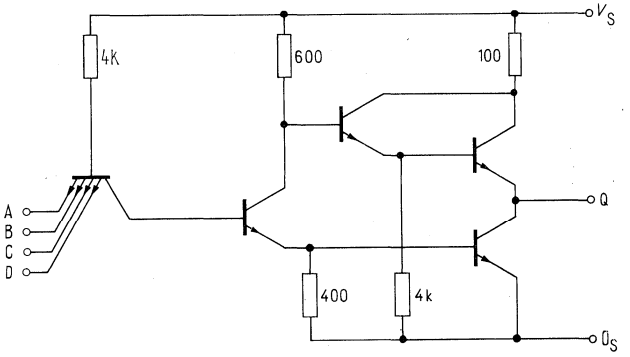
Propagation Delay	t_{PHL}	C_1=15 pF, F_Q=30	22		8	15	ns
	t_{PLH}				13	22	ns

Logical data

Output load factor, each output	F_Q					30	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{ABCD}$					



Pin configuration
top view



Schematic (each gate)

FLH 151 – 7450
FLH 155 – 8450
FLH 161 – 7451
FLH 165 – 8451

order numbers

FLH 151: Q67000–H6
FLH 155: Q67000–H159
FLH 161: Q67000–H7
FLH 165: Q67000–H160

Dual 2+2-input AND/OR-Gate inverting

FLH 151, FLH 155 with expander nodes N_1 and N_2
FLY 101, FLY 105 corresponding expander
FLH 161, FLH 165 without expander nodes (pins 11 and 12 must not be connected)

Electrical characteristics

temperature ranges 1 and 5
pins 11 and 12 open

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	7	2.0			
L-input voltage	V_{IL}	V_S=4.75 V	8			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V, $-I_{QH}$=400 µA	8	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA	7		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	9			40	µA
	I_I	V_I=5.5 V | =5.25 V	9			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	10			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	11	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V	13		4	8	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5 V	12		7.4	14	mA

Delay times, V_S=5 V, T_A=25 °C, pins 11 and 12 open

Propagation delay	t_{PLH} t_{PHL}	} C_1=15 pF, F_Q=10	22		8 13	15 15	ns ns

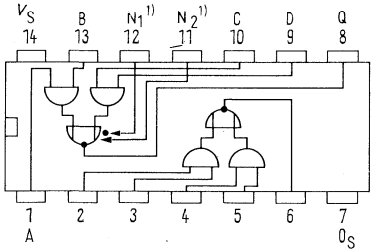
Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{AB+CD+\text{exp.}}$[1]					

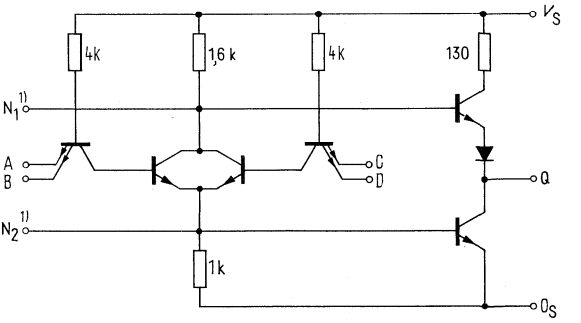
[1]) FLH 151/155 only

Electrical characteristics of the expander nodes N_1 and N_2 at V_S=5 V, T_A=0 °C[1, 2])

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Input current of the expander nodes N_1 and N_2	$I_{N1,N2}$	V_S=4.75 V R=130 Ω I_{QH}=16 mA	15			3.1	mA
Base-emitter-voltage of the lower output transistor	V_{BE}	V_S=4.75 V R=130 Ω I_{QH}=16 mA, I_{N2}=620 µA	15			1	V
H-output voltage	V_{QH}	V_S=4.75 V $-I_{QH}$=400 µA $-I_{N1}$=270 µA I_{N2}=270 µA	16	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V I_{SQ}=16 mA R=130 Ω I_{N2}=0.43 mA	15		0.22	0.4	V



Pin configuration
top view



Schematic
(each gate)

1) FLH 151/155 only
2) Nodes N_1 and N_2 are used simultaneously for expansion.
If N_1 and N_2 are unused, they must not be connected or tied together.
Up to 4 FLY 101 and FLY 105, resp. may be connected to one FLH 151 and FLH 155, resp.

FLH 171 – 7453
FLH 175 – 8453
FLH 181 – 7454
FLH 185 – 8454

order numbers

FLH 171:	Q67000–H8
FLH 175:	Q67000–H161
FLH 181:	Q67000–H9
FLH 185:	Q67000–H162

2+2+2+2-input AND/OR-Gate inverting

FLH 171, FLH 175 with expander nodes N_1 and N_2
FLY 101, FLY 105 corresponding expander
FLH 181, FLH 185 without expander nodes (pins 11 and 12 must not be connected)

Electrical characteristics

temperature ranges 1 and 5
pins 11 and 12 open

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	7	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	8			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IS}=0.8 V, $-I_{QH}$=400 µA	8	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V, V_{QL}=2.0 V, I_{QL}=16 mA	7		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	9			40	µA
	I_I	V_I=5.5 V | =5.25 V	9			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V	10			1.6	mA
Short circuit output current	$-I_Q$	V_S=5.25 V	11	18		55	mA
Supply current	I_{SH}	V_S=5.25 V, V_I=0 V	13		4	8	mA
L-supply current	I_{SL}	V_S=5.25 V, V_I=5 V	12		5.1	9.5	mA

Delay times, V_S=5 V, T_A=25 °C, pins 11 and 12 open

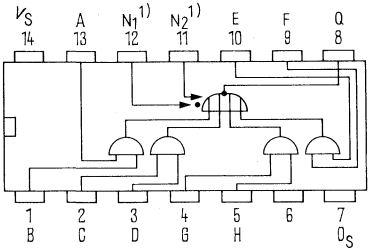
Propagation delay	t_{PHL}	C_1=15 pF, F_Q=10	22		8	15	ns
	t_{PLH}				13	22	ns

Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{AB+CD+GH+EF+\text{exp.}^1)}$					

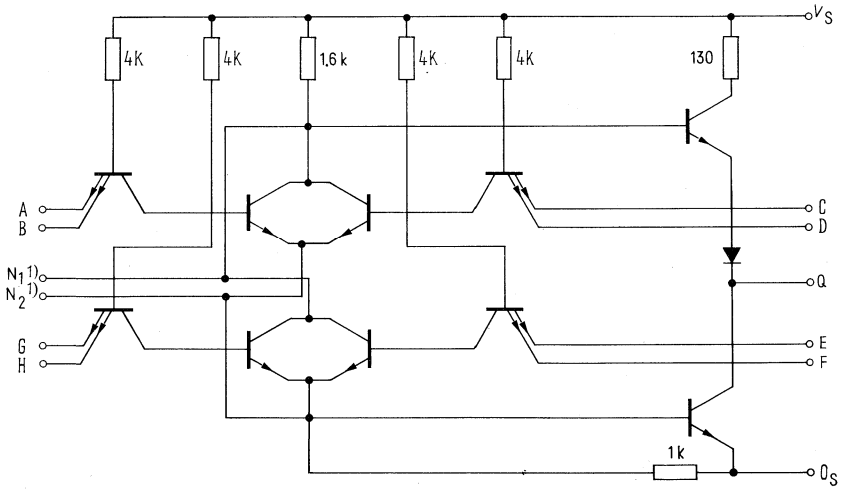
Electrical characteristics of the nodes N_1 and N_2[1,2]
see AND/OR-gate FLH 151/155

1) FLH 171/175 only
2) Nodes N_1 and N_2 are used simultaneously for expansion.
If N_1 and N_2 are unused, they must not be connected or tied together.
Up to 4 FLY and FLY 105 resp. may be connected to one FLH 171 and FLH 175 resp.



Pin configuration
top view

Schematic



1) FLH 171/175 only

FLH 191 – 7402
FLH 191 S – 7402-S1
FLH 195 – 8402

order numbers

FLH 191: Q67000-H10
FLH 191S: Q67000-H428
FLH 195: Q67000-H163

Quadruple 2-input NOR-Gate

Electrical characteristics
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	7	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	8			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=400 µA	8	2.4	3.3		V
L-output voltage		V_S=4.75 V V_{IH}=2 V, I_{QL}=16 mA	7		0.22	0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	9			40	µA
	I_I	V_I=5.54 V | =5.25 V	9			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	10			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25	11	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V	13		8	16	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5 V	12		14	27	mA

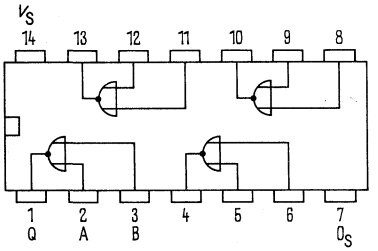
Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	C_1=15 pF, F_Q=10	22		8	15	ns
	t_{PLH}				12	22	ns

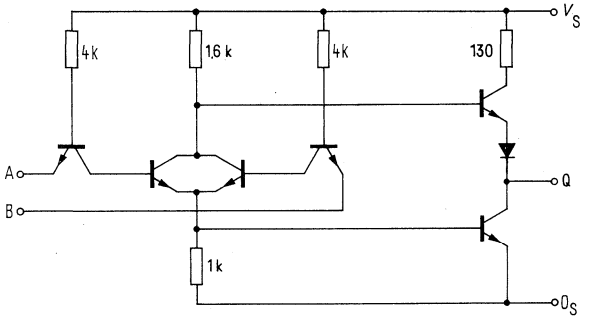
Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{AB}$					

FLH 191S: as FLH 191, however output reverse current I_{QH} < 500 µA at V_Q=6.5 V



Pin configuration
top view



Schematic (each gate)

FLH 201 – 7401
FLH 201 S – 7401 S1
FLH 201 T – 7401 S3
FLH 205 – 8401
FLH 205 S – 8401 S1
FLH 205 T – 8401 S3

order numbers

FLH 201: Q67000–H11
FLH 201S: Q67000–H433
FLH 201T: Q67000–H409
LH 205: Q67000–H1640
FFLH 205S: Q67000–H45
FLH 205T: Q67000–H334

Quadruple 2-input NAND-Gate with Open Collector Output

The gates FLH 201/205 are suited for wired-AND-connections

Electrical characteristics temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	14			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2 V, I_{QH}=16 mA	1			0.4	V
DC noise margin	V_{nm}			0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	3			40	µA
	I_I	V_I=5.5 V | =5.25 V	3			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	4			1.6	mA
H-output current, each output	I_{QH}	V_S=4.75 V V_{QH}=5.5 V, V_{IL}=0.8 V	14			250	µA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V	6		4	8	mA
L-supply current	I_{SL}	V_S=5.25 V V_I=5.0 V	6		12	22	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL}	R_L=400 Ω | C_1=15 pF	22		8	15	ns
	t_{PLH}	R_L=4 kΩ			35	45	ns

Logical data

Output load factor, each output	F_Q					10	
Input load factor, each input	F_I					1	
Logic		$Q=\overline{AB}$					

Calculation of the collector load resistor R_L

The following formulae apply

H-state

$$R_{L\,max} = \frac{V_S - 2.4\ V}{n\ 250\ \mu A + N\ 40\ \mu A}\ M\Omega$$

L-state

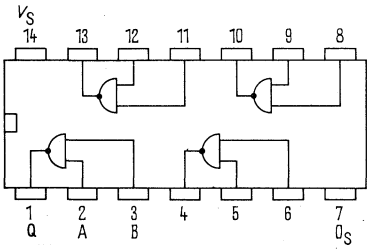
$$R_{Lmin} = \frac{V_S - 0.4\ V}{(10 - N) \cdot 1.6\ mA}\ k\Omega$$

where: V_S = supply voltage
n = number of gates, AND-connected
N = number of inputs connected
} (values see table)

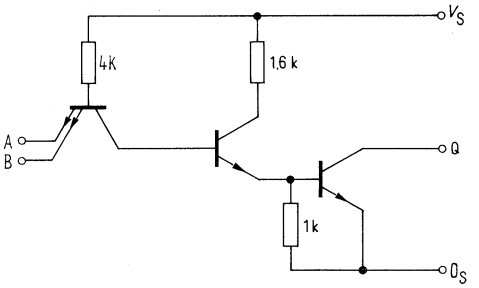
FLH 201/205 S: as FLH 201/205, however output 15 V/150 µA
FLH 201/205 T: as FLH 201/205, however output 5.5 V/50 µA

At V_S=5 V and a corresponding variation of n and N the following maximum and minimum values result for R_L. The resistor used in the circuit must have a value in between R_{Lmax} and R_{Lmin} (see table).

N	n							n
	1	2	3	4	5	6	7	1...7
	$R_{Lmax}\,\Omega$							$R_{Lmin}\,\Omega$
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2419	1969	1656			1437
9	4262	3023						2875
10	4000			not permitted				4000



Pin configuration
top view



Schematic
(each gate)

FLH 211 – 7404
FLH 215 – 8404

order numbers
FLH 211: Q67000–H153
FLH 215: Q67000–H243

Hexinverter

Electrical characteristics
temperature ranges 1 and 5

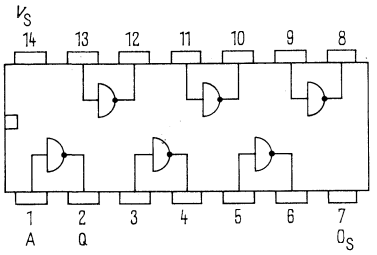
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IH}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V V_{IL}=0.8 V $-I_{QH}$=400 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2.0 V, I_{QL}=16 mA		0.22	0.4	V
DC noise margin	V_{nm}		0.4	1.0		V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S			40	µA
	I_I	V_I=5.5 V | =5.25 V			1.0	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V V_I=0 V		6	12	mA
L-Supply current	I_{SL}	V_S=5.25 V V_I=5.0 V		18	33	mA

Delay times, V_S=5 V, T_A=25 °C

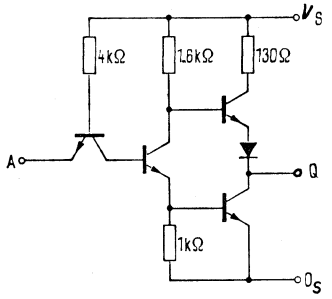
Propagation delay	t_{PHL}	C_1=15 pF R_L=400 Ω		8	15	ns
	t_{PLH}			12	22	ns

Logical data

Output load factor, each output	F_Q				10	
Input load factor, each input	F_I				1	
Logic		$Q=\bar{A}$				



Pin configuration
top view



Schematic (each gate)

FLH 221 – 7480
FLH 225 – 8480

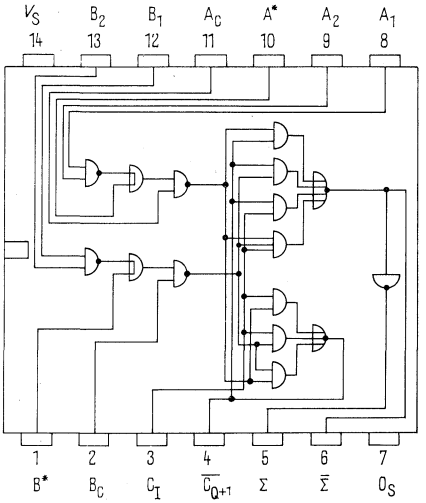
order numbers

FLH 221: Q67000–J26
FLH 225: Q67000–H244

1-bit-Fulladder

The FLH 221/225 are 1-bit-fulladders with complementary inputs and outputs. The carry results at output $\overline{C_Q}$.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	F_Q see table	2.4	3.5		V
L-ouput voltage	V_{QL}			0.22	0.4	V
L-input current at A_1, A_2, B_1, B_2, A_C or B_C	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V			1.6	mA
L-input current at A* or B*	$-I_{IL}$				2.6	mA
L-input current at C_I	$-I_{IL}$				8.0	mA
H-input current at	I_{IQ}	V_{IH}=2.4 V; V_S=			15	µA
A_1, A_2, B_1, B_2, A_C or B_C	I_I	V_I=5.5 V; V_S=			1.0	mA
H-input current at C_I	I_{IH}	V_{IH}= 2.4 V; 5.25 V			200	µA
	I_I	V_I=5.5 V			1.0	mA
Short circuit output current at Σ or $\overline{\Sigma}$, each output	$-I_Q$		18		57	mA
Short circuit output current at $\overline{C_Q}$	$-I_Q$	V_S=5.25 V	18		70	mA
Supply current	I_S			21	35	mA
Delay times, V_S=5 V, T_A=25 °C						
Propagation delay from input C_I to output $\overline{C_Q}$	t_{PHL}	C_1=15 pF, R_L=780 Ω		8	12	ns
from input B_C to output C_Q	t_{PHL}	C_1=15 pF, R_L=780 Ω		38	55	ns
from input A_C to output Σ	t_{PHL}	C_1=15 pF, R_L=400 Ω		62	80	ns
from input B_C to output $\overline{\Sigma}$	t_{PHL}	C_1=15 pF, R_L=400 Ω		56	75	ns
from input A_1 to output A*	t_{PHL}	C_1=15 pF		17	25	ns
from imput B_1 output B*	t_{PHL}	C_1=15 pF		17	25	ns
Propagation delay from input C_I to output $\overline{C_Q}$	t_{PLH}	C_1=15 pF, R_L=780 Ω		13	17	ns
from input B_C to output $\overline{C_Q}$	t_{PLH}	C_1=15 pF, R_L=780 Ω		18	25	ns
from input A_C to output Σ	t_{PLH}	C_1=15 pF, R_L=400 Ω		52	70	ns
from input B_C output $\overline{\Sigma}$	t_{PLH}	C_1=15 pF, R_L=400 Ω		38	55	ns
from input A_1 to output A*	t_{PLH}	C_1=15 pF		48	65	ns
from input B_1 to output B*	t_{PLH}	C_1=15 pF		48	65	ns
Logical data						
Output load factor at $\overline{C_Q}$	F_Q				5	
Output load factor Σ or $\overline{\Sigma}$	F_Q				10	
Output load factor A* or B*	F_Q				3	
Input load factor at A_1, A_2, B_1, B_2, A_C or B_C	F_I				1	
Input load factor at C_I	F_I				5	



Pin configuration
top view

Truth table

inputs			outputs		
C_I	B	A	$\overline{C_Q}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

Notes:

1. $A = \overline{A^* A_C}$, $B = \overline{B^* B_C}$
   where $A^* = \overline{A_1 A_2}$, $B^* = \overline{B_1 B_2}$
2. If A* (B*) is used as input, A_1 and A_2 (B_1 and B_2) must be grounded.
3. If inputs A_1 and A_2 or B_1 and B_2 are used, A* and B* resp. must be left open or wire-AND-connected (see FLH 201 for resistance table).

FLH 231 – 7482
FLH 235 – 8482

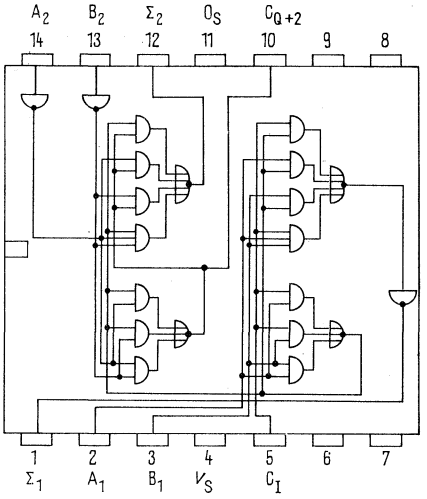
order numbers

FLH 231: Q67000–J28
FLH 235: Q67000–H245

2-bit-Fulladder

The FLH 231/235 are fulladders for 2 x 2 bits. The respective sum results at outputs Σ_1 and Σ_2, the carry is only available for the 2nd bit.

Electrical characteristic temperature ranges 1 and 5		test condition		lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V		2.0			V
L-input voltage	V_{IL}	V_S=4.75 V				0.8	V
H-output voltage	V_{QH}	V_S=4.75 V		2.4	3.5		V
L-output voltage	V_{QL}	F_Q see table			0.22	0.4	V
L-input current at A_1, B_1 or C_I	$-I_{IL}$	V_S=5.25 V				6.4	mA
L-input current at A_2 or B_2	$-I_{IL}$	V_{IL}=0.4 V				1.6	mA
H-input current at A_1, B_1 or C_I	I_{IH}	V_{IH}=2.4 V	V_S=			160	µA
	I_I	V_I=5.5 V	5.25 V			1.0	mA
H-input current at A_2 or B_2	I_{IH}	V_{IH}=2.4 V				40	µA
	I_I	V_I=5.5 V				1.0	mA
Short circuit output current at C_{Q+2}	$-I_Q$			18		70	mA
Short circuit output current at Σ_1 or Σ_2, each output	$-I_Q$	V_S=5.25 V		18		55	mA
Supply current	I_S				36	58	mA
Delay times, V_S=5 V, T_A=25 °C							
Propagation delay from input C_I to output Σ_1	t_{PHL}					40	ns
from input B_2 to output Σ_2	t_{PHL}					35	ns
from input C_I to output Σ_2	t_{PHL}	C_1=15 pF				42	ns
from input C_I to output C_{Q+2}	t_{PHL}	R_L=400 Ω			12	19	ns
Propagation delay from input C_I to output Σ_1	t_{PLH}	R_L=780 Ω at C_{Q+2}				34	ns
from input B_2 to output Σ_1	t_{PLH}					40	ns
from input C_I to output Σ_2	t_{PLH}					38	ns
from input C_I to output C_{Q+2}	t_{PLH}				17	27	ns
Logical data							
Output load factor at C_{Q+2}	F_Q					5	
Output load factor at Σ_1 or Σ_2	F_Q					10	
Output load factor at A_2 or B_2	F_I					1	
Input load factor at A_1, B_1 or C_I	F_I					4	



Pin configuration
top view

Truth table

inputs				outputs					
				C_I = L			C_I = H		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_{Q+2}	Σ_1	Σ_2	C_{Q+2}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

FLH 241 – 7483
FLH 245 – 8483

order numbers

FLH 241: Q67000–J29
FLH 245: Q67000–H248

4-bit-Fulladder

The FLH 241/245 are fulladders for 4 x 2 bits.
The sum outputs are provided for each bit. The resulting carry is available at C_{Q+4} only for the 4th bit.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			8.0	V
H-output voltage	V_{QH}	F_Q see table	2.4	3.5		V
L-output voltage	V_{QL}			0.22	0.4	V
L-input current at A_1, A_3, B_1, B_3 or C_I	$-I_{IL}$	V_S=5.25 V			6.4	mA
L-input current at A_2, A_4, B_2 or B_4	$-I_{IL}$	V_{IL}=0.4 V			1.6	mA
H-input current at A_1, A_3, B_1, B_3 or C_I	I_{IH}	V_{IH}=2.4 V, V_S=			160	µA
	I_I	V_I=5.5 V, 5.25 V			1.0	mA
H-input current at A_2, A_4, B_2 or B_4	I_{HI}	V_H=2.4 V			40	µA
	I_I	V_I=5.5 V			1.0	mA
Short circuit output current at Σ_1, Σ_2, Σ_3 or Σ_4, each output	$-I_Q$		18		55	mA
Short circuit output current at C_{Q+4}	$-I_Q$	V_S=5.25 V	18		70	mA
Supply current	I_S			78	128	mA
Delay times, V_S=5 V, T_A=25 °C						
Propagation delay from input C_I to output Σ_1	t_{PHL}				40	ns
from input C_I to output Σ_2	t_{PHL}				42	ns
from input C_I to output Σ_3	t_{PHL}				60	ns
from input C_I to output Σ_4	t_{PHL}	C_1=15 pF			55	ns
from input C_I to output C_{Q+4}	t_{PHL}	R_L=400 Ω		22	32	ns
from input A_2 or B_2 to output Σ_2	t_{PHL}	R_L=780 Ω at C_{Q+4}			35	ns
from input A_4 or B_4 to output Σ_4	t_{PHL}				35	ns
Propagation delay from input C_I to output Σ_1	t_{PLH}				34	ns
from input C_I to output Σ_2	t_{PLH}				38	ns
from input C_I to output Σ_3	t_{PLH}				50	ns
from input C_I to output Σ_4	t_{PLH}	C_1=15 pF			55	ns
from input C_I to output C_{Q+4}	t_{PLH}	R_L=400 Ω		35	48	ns
from input A_2 or B_2 to output Σ_2	t_{PLH}	R_L=780 Ω at C_{Q+4}			40	ns
from input A_4 or B_4 to output Σ_4	t_{PLH}				40	ns
Logical data						
Output load factor at C_{Q+4}	F_Q				5	
Output load factor at Σ_1, Σ_2, Σ_3 or Σ_4	F_Q				10	
input load factor at A_2, A_4, B_2 or B_4	F_I				1	
input load factor at A_1, A_3, B_1, B_3 or C_I	F_I				4	

order numbers

FLJ 471: Q67000–J308

FLJ 471 – 74167

Programmable Decimal Rate Multiplier

The FLJ 471 performs fixed-rate or variable rate frequency division. The division ratio is selected by means of the inputs A through C as follows:

$f_Q = f_I \times \frac{M}{10}$, where $M = D \times 2^3 + C \times 2^2 + B \times 2^1 + A \times 2^0$ for decimals 0 to 9

The clock frequency is 32 MHz typically. The divider is released by L-signal at the enable input E_I and the reset input R. H-signal at the strobe disables the divider output Q.
Dividers are cascaded by connecting the enable output E_Q of the first stage to the enable input E_I and the strobe input of the second stage. The Q-outputs are crossconnected with the expander inputs N. The desired output frequency results at the outputs Q of each divider stage. H-signal at the set input S_G sets the counter to decimal 9.
Applications: division, analog-digital and digital-analog-conversion.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current at C	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			80	µA
remaining inputs	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current at C	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			3.2	mA
remaining inputs	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		55	mA
H-supply current	I_{SH}	V_S=5.25 V		43		mA
L-supply current	I_{SL}	V_S=5.25 V		65	99	mA

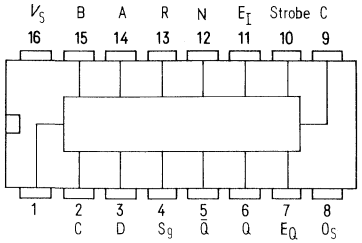
Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Maximum clock frequency	f		25	32		MHz
Clock pulse duration	t_{pC}		10			ns
Setup time	t_S		25			ns
Hold time	t_H		0			ns
Propagation delay from C to Q	t_{PLH}	C_L=15 pF, R_L=400 Ω		26	39	ns
	t_{PHL}	C_L=15 pF, R_L=400 Ω		20	30	ns
from strobe to Q	t_{PLH}	C_L=15 pF, R_L=400 Ω		19	30	ns
	t_{PHL}	C_L=15 pF, R_L=400 Ω		22	33	ns

Logical data

Output load factor	F_Q	10	
Input load factor at C	F_I	2	
remaining input	F_I	1	

FLJ 471



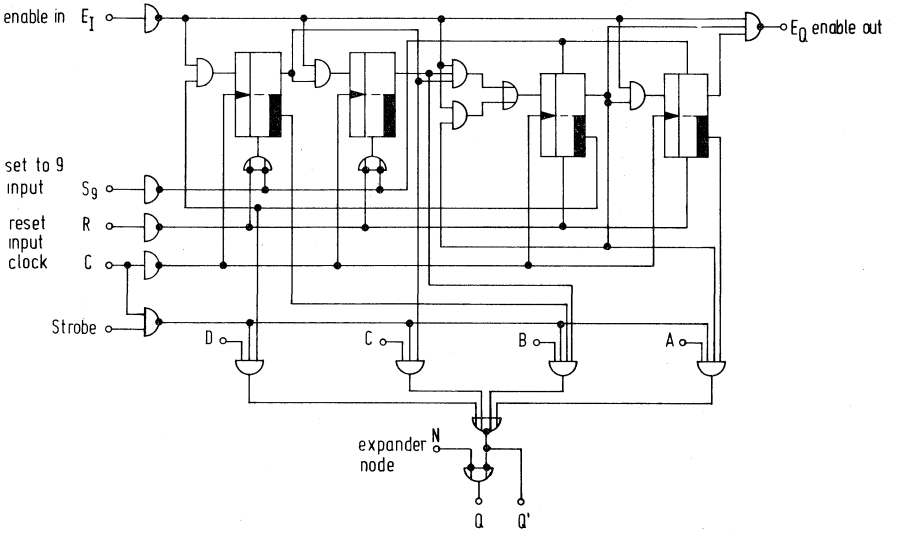
Pin configuration
top view

Truth table

inputs								outputs		
reset input R	enable input E_I	strobe	D	C	B	A	number of clock pulses	expander input N	logic state or number of pulses Q	$\bar{Q}$	FA
H	X	H	X	X	X	X	X	H	L	H	H
L	L	L	L	L	L	L	10	H	L	H	1
L	L	L	L	L	L	H	10	H	1	1	1
L	L	L	L	L	H	L	10	H	2	2	1
L	L	L	L	L	H	H	10	H	3	3	1
L	L	L	L	H	L	L	10	H	4	4	1
L	L	L	L	H	L	H	10	H	5	5	1
L	L	L	L	H	H	L	10	H	6	6	1
L	L	L	L	H	H	H	10	H	7	7	1
L	L	L	H	L	L	L	10	H	8	8	1
L	L	L	H	L	L	H	10	H	9	9	1
L	L	L	H	L	H	L	10	H	8	8	1
L	L	L	H	L	H	H	10	H	9	9	1
L	L	L	H	H	L	L	10	H	8	8	1
L	L	L	H	H	L	H	10	H	9	9	1
L	L	L	H	H	H	L	10	H	8	8	1
L	L	L	H	H	H	H	10	H	9	9	1
L	L	L	H	L	L	H	10	L	H	9	1

Notes:
X=H or L-signal
Inputs A through C can be varied as required.

block diagram



FLK 101 – 74121
FLK 105 – 84121

order numbers

FLK 101: Q67000–K13
FLK 105: Q67000–K10

Monostable Multivibrator

The FLK 101/105 are monostable multivibrators. The following input functions are provided: The A-inputs trigger the multivibrator during the falling edge of the input pulse while the B-input is supplied with an H-level.
The B-input is a Schmitt-Trigger-input which releases the multivibrator at slowly rising input pulses of up to 1 V/s. The B-input triggers the multivibrator during the rising edge of the input pulse while the A-inputs are supplied with an L-level.
Once the multivibrator has been released, the output pulse is a function of the timing components R_T and C_T only. The capacitor C_T is connected between H (positive) and J. The resistor R_T is connected between J and V_S (G open) or G and V_S. An internal timing resistor of nominal 2 kΩ is provided at G. Without external timing components (G and V_S connected, J and H open) an output pulse duration of 30 ns typically results.
The output pulse duration t_Q is nearly independent of supply voltage and temperature variations due to internal compensation. It is limited by the tolerance and the quality of the external components. The output pulse duration is defined by the formula $t_Q = C_T R_T \log e\ 2 \sim 0.7\ C_T R_T$.
The typical noise immunity of the inputs is 1.2 V. Supply voltage noise rejection is typical 1.5 V.

Operating conditions

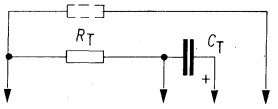
		lower limit B	upper limit A	unit
Transition times at input A_1, A_2	t_{THL}		1	V/µs
at input B	t_{TLH}		1	V/s
Input pulse duration	t_I	50		ns
Timing resistance between pins 11 and 14	R_T	1.4		kΩ
Timing resistance between pins 9 and 14	R_T	0	40	kΩ
Timing capacitance between pins 10 and 11	C_T	0	1000	µF
Output pulse duration	t_Q		40	s
Duty cycle R_T = 2 kΩ			67	%
R_T = 40 kΩ			90	%

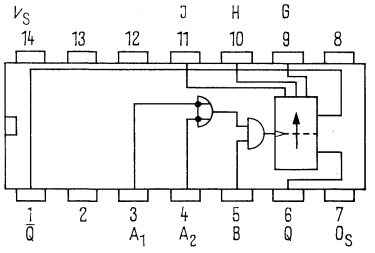
Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
Upper threshold voltage						
at A_1 or A_2	V_{Tu}			1.4	2.0	V
at B	V_{Tu}	V_S=4.75 V		1.55	2.0	V
Lower threshold voltage						
at A_1 or A_2	V_{TI}		0.8	1.4		V
at B	V_{TI}		0.8	1.35		V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=400 µA	2.4	3.3		V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA		0.22	0.4	V
Input current, each input	I_I	V_I=5.5 V, V_S=5.25 V		0.05	1.0	mA
H-input current						
at A_1 or A_2	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V		2.0	40	µA
at B	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V		4.0	80	µA
L-input current						
at A_1 or A_2	$-I_{IL}$	V_S=5.25 V		1.0	1.6	mA
at B	$-I_{IL}$	V_{IL}=0.4 V		2.0	3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18	25	55	mA
Supply current at Q=L	I_{SL}	V_S=5.25 V		13	25	mA
Supply current at Q=H	I_{SH}	V_S=5.25 V		23	40	mA

Delay times, V_S=5 V, T_A=25 °C		test condition	lower limit B	typ.	upper limit A	unit
Propagation delay						
from A_1 or A_2 to $\overline{Q}$	t_{PHL}		30	50	80	ns
from B to $\overline{Q}$	t_{PHL}	C_L=15 pF	20	40	65	ns
Propagation delay		C_T=80 pF				
from A_1 or A_2 to Q	t_{PLH}		25	45	70	ns
from B to Q	t_{PLH}		15	35	55	ns
output pulse duration						
with internal timing resistance (pins 9 and 14 connected)	t_Q	C_L=15 pF, C_T=80 pF R_T=0	70	110	150	ns
without timing capacitance (pins 9 and 14 connected, 10 and 11 open)	t_Q	C_L=15 pF, R_T=0	20	30	50	ns
with external timing resistance 10 kΩ (pin 9 open)	t_Q	C_T=100 pF | C_L=15 pF	600	700	800	ns
	t_Q	C_T=1 µF	6	7	8	ms
minimum input pulse duration	t_I	C_L=15 pF, C_T=80 pF R_T=0 (pins 9 and 14 connected)		30	50	ns

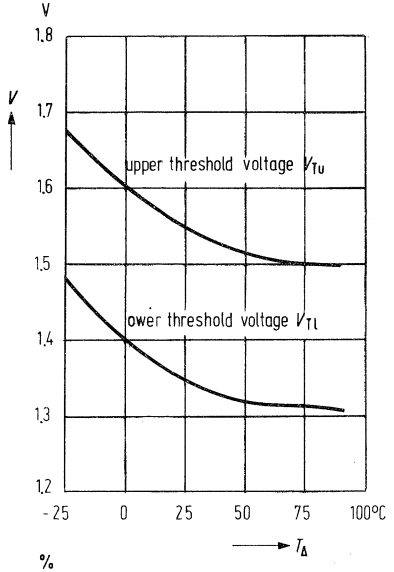
Logical data						
Output load factor, each output	F_Q				10	
Input load factor at A_1 or A_2	F_I				1	
Input load factor at B	F_I				2	



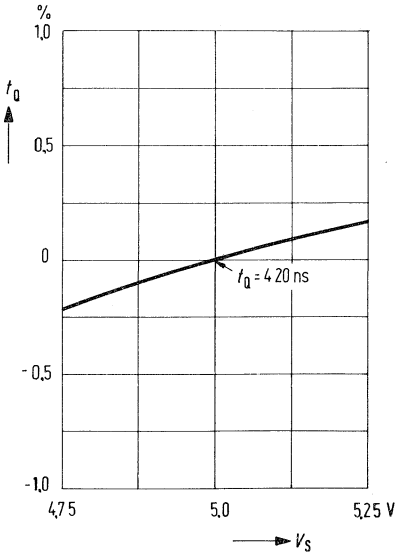


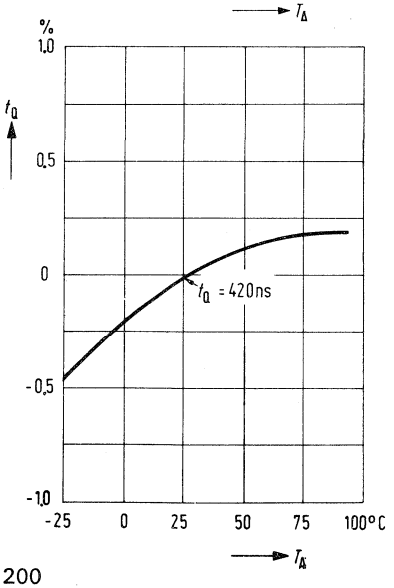
Pin configuration
top view

Treshold voltage at Schmitt-Trigger-input B as a function of the ambient temperature T_A at V_S=5 V



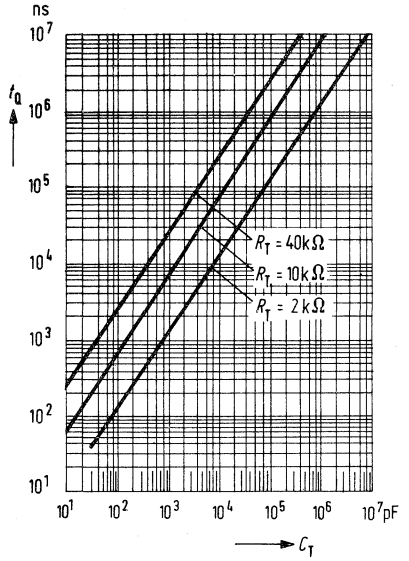
Output pulse duration t_Q as a function of the supply voltage V_S at T_A=25 °C



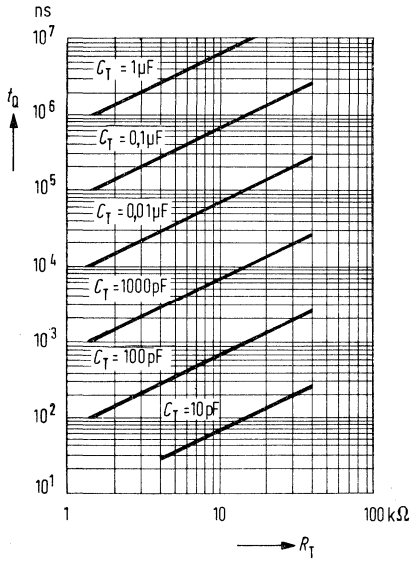


Output pulse duration t_Q as a function of the ambient temperature T_A at V_S=5 V

Output pulse duration t_Q as a function of the external timing capacitance C_T at V_S=5 V, T_A=25 °C



Output pulse duration t_Q as a function of the external timing resistance R_T at V_S=5 V, T_A=25 °C



FLK 111 – 74122
FLK 115 – 84122
FLK 121 – 74123
FLK 125 – 84123

order numbers

FLK 111:	Q67000–K27
FLK 115:	Q67000–K28
FLK 121:	Q67000–K29
FLK 125:	Q67000–K30

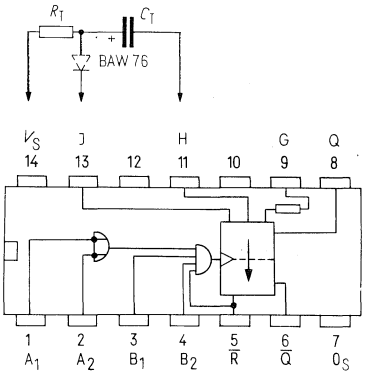
Monostable Multivibrators

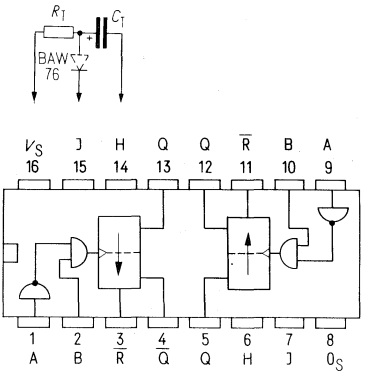
FLK 111/115: Monostable Multivibrator with Reset
FLK 121/125: Dual Monostable Multivibrator with Reset

The A-inputs trigger the multivibrator during the falling edge of the input pulse, while the remaining inputs are supplied with an H-level.
The B-inputs trigger the multivibrator during the rising edge of the input pulse while the A-inputs are supplied with an L-signal and the reset input $\bar{R}$ with an H-signal.
L-signal at $\bar{R}$ resets the multivibrator to Q=L independent of any other input condition. The multivibrator can be retriggered. The output pulse duration is always defined by the last trigger pulse (see pulse diagram).
The output pulse duration is a function of the timing components R_T and C_T. The capacitor C_T is connected between H and J (positive), the resistance R_T between J and V_S.
An internal timing resistor of nominal 10 kΩ is provided at terminal G of the FLK 111/115. The output pulse duration t_Q for $C_T \leqq 1000$ pF is given by a diagram. Values of $C_T > 1000$ pF as well as electrolytic capacitors require a protecting diode BAW 76 at terminal J. The maximum timing resistance in this case is 30 kΩ.
The output pulse duration is defined by the following formula:

$$t_Q = 0.28 \times R_T \times C_T \times \left(1 + \frac{0.7}{R_T}\right)$$

Where R_T in kΩ
C_T in pF
t_Q in ns





Pin configurations, top view

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
Input clamping voltage	$-V_I$	V_S=4.75 V, $-I_I$=12 mA			1.5	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_Q$=800mA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_Q=16 mA		0.22	0.4	V
H-input current at A, B	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1	mA
H-input current at $\bar{R}$	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			80	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1	mA
L-input current at A, B	$-I_{IL}$	V_{IL}=0.4 V, V_S=5.25 V			1.6	mA
L-input current at $\bar{R}$	$-I_{IL}$	V_{IL}=0.4 V, V_S=5.25 V			3.2	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	10		40	mA
Supply current FLK 111/115	I_S	V_S=5.25 V		23	28	mA
Supply current FLK 121/125	I_S	V_S=5.25 V		46	65	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay from A to Q	t_{PLH}			22	33	ns
from B to C	t_{PLH}			19	28	ns
from A to $\bar{Q}$	t_{PHL}	C_T=0; R_T=5 kΩ		30	40	ns
from B to $\bar{Q}$	t_{PHL}	C_L=15 pF; R_L=400 Ω		27	36	ns
from $\bar{R}$ to Q	t_{PHL}			18	27	ns
from $\bar{R}$ to $\bar{Q}$	t_{PLH}			30	40	ns
Minimum output pulse duration	t_Q			45	65	ns
Output pulse duration	t_Q	C_T=1000 pF; R_T=10kΩ C_L=15 pF; R_L=400 Ω	3.08	3.42	3.76	µs
Hold time	t_H		40			ns
Setup time	t_S		40			ns
Reset pulse duration	t_R		40			ns

Timing components

Resistance	R_T		5		50	kΩ
Capacitance	C_T			no restriction		
Internal capacitance at pin J	C_o				50	pF

Logical data

Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor at A, B,	F_I				1	
at $\bar{R}$	F_I				2	

FLK 111
FLK 115
FLK 121
FLK 125

Truth table FLK 111/115

inputs				outputs	
A1	A2	B1	B2	Q	$\bar{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	⌐	H	⌐⌙	⌙⌐
L	X	H	⌐	⌐⌙	⌙⌐
X	L	H	H	L	H
X	L	⌐	H	⌐⌙	⌙⌐
X	L	H	⌐	⌐⌙	⌙⌐
H	⌙	H	H	⌐⌙	⌙⌐
⌙	⌙	H	H	⌐⌙	⌙⌐
⌙	H	H	H	⌐⌙	⌙⌐

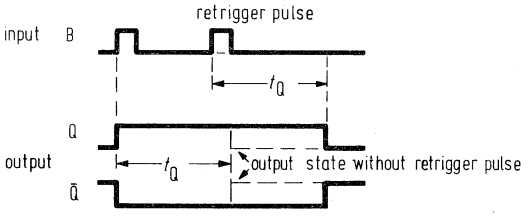
Truth table FLK 121/125

inputs		outputs	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	⌐	⌐⌙	⌙⌐
⌙	H	⌐⌙	⌙⌐

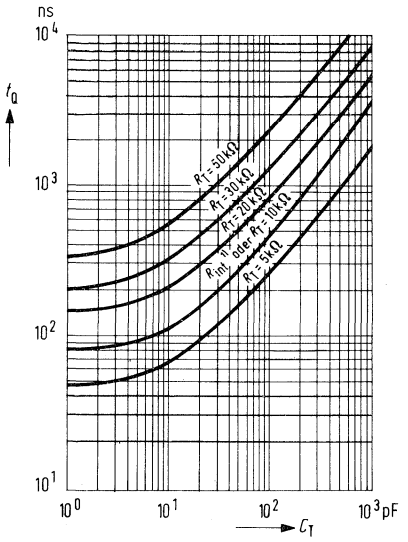
Notes:

= H- or L-signal
= H-pulse
= L-pulse
= transition from L to H
= transition from H to L

Pulse diagram



Output pulse duration t_Q as a function of the external timing capacitance C_T at V_S=5 V, T_A=25 °C



1) FLK 111/115 only

FLL 101 – 74141

order numbers
FLL 101: Q67000–L1

BCD-Decimal Decoder-Driver for indicator tubes

The FLL 101 decodes binary coded decimal numbers. Due to integrated output transistors with high breakdown voltages the direct operation of indicator tubes is possible. The inputs of the FLL 101 can be directly connected to the outputs of the decimal counters FLJ 161, FLJ 201, FLJ 241, FLJ 381, FLJ 401, FLJ 421.
The connections are A with Q_A, B with Q_B, C with Q_C, and D with Q_D.
Binary information between 10 and 15 is suppressed. Thus an automatic zero-blanking can be realized.

In addition the following maximum ratings apply:

Maximum ratings

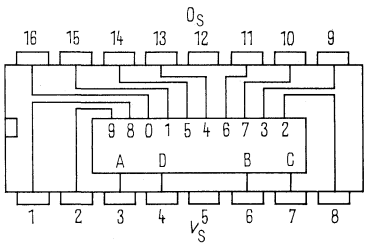
			lower limit B	upper limit A	unit
Output current	I_Q	T_Q blocked	0	2.0	mA
Output voltage	V_Q	T_Q blocked	0	60	V

Electrical characteristics
temperature ranges 1 and 5

		test condition		lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V		2.0			V
L-input voltage	V_{IL}	V_S=4.75 V				0.8	V
L-output voltage	V_{QL}	V_S=4.75 V V_{QL}=7 mA				2.5	V
Output voltage, T_Q blocked, input information 0 to 9	V_Q	V_S=5.25 V I_Q=0.5 mA		60			V
Output current, T_Q blocked	I_Q	V_S=5.25 V V_Q=55 V				50	µA
Output current, T_Q blocked Input information 10 to 15	I_Q	V_S=5.25 V V_Q=30 V				10	µA
H-input current at A	I_{IH}	V_{IH}=2.4 V	V_S=5.5 V			40	µA
	I_I	V_I=5.5 V				1	mA
H-input current, at B, C or D	I_{IH}	V_{IH}=2.4 V				80	µA
	I_I	V_I=5.5 V				1	mA
L-input current, at A	$-I_{IL}$	V_{IL}=0.4 V				1.6	mA
L-input current, at B, C or D	$-I_{IL}$	V_{IL}=0.4 V				3.2	mA
Supply current	I_S	V_S=5.25 V			16	25	mA

Logical data

Input load factor at A	F_I		1
Input load factor at B, C or D	F_I		2



Pin configuration
top view

Truth table

BCD-inputs D	C	B	A	output[1])
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	–
H	L	H	H	–
H	H	L	L	–
H	H	L	H	–
H	H	H	L	–
H	H	H	H	–

[1]) The output indicated is conducting. All other output transistors are blocked.

FLL 111 – 7445
FLL 111 T – 74145
FLL 115 – 88445
FLL 115 T – 84145

order numbers

FLL 111: Q67000–L9
FLL 111T: Q67000–L8
FLL 115: Q67000–L46
FLL 115T: Q67000–L45

BCD-Decimal-Decoder-Driver with Open Collector Outputs

FLL 111/115: BCD-decimal-decoder and driver with open collecter outputs with 30 V/80 mA.
FLL 111 T/115 T: BCD-decimal-decoder and driver with open collector outputs with 15 V/80 mA.
The FLL 111/115, FLL 111 T/115 T decode 4-bit binary coded decimal numbers.
The driver stages have open collector outputs with high breakdown voltages for high load currents.
Wired-AND-connections are possible with the open collector outputs.
Applications: core-memory address-driver, lamp and relais driver, line driver.

In addition the following maximum ratings apply:

Maximum ratings

			lower limit B	upper limit A	unit
Output voltage FLL 111/115	V_Q	T_Q blocked	0	30	V
FLL 111T/115T	V_Q	T_Q blocked	0	15	V
Output current	I_Q	T_Q conducting	0	1	mA
Output current	I_Q	T_Q conducting	0	80	mA

Electrical characteristics
temperature ranges 1 and 5

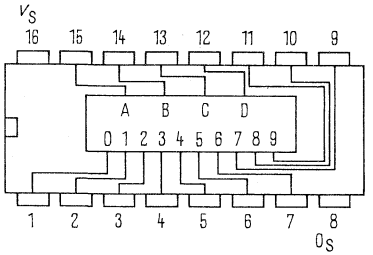
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V=4.75 V	2.0			V
L-input voltage	V_{IL}	V=4.75 V			0.8	V
L-output voltage	V_{QL}	I_{QL}=80 mA, V_S=4.75 V		0.5	0.9	V
		I_{QL}=20 mA, V_S=4.75 V			0.4	V
Output voltage (FLL 111/115)	V_Q	V_S=5.25 V, I_Q=250 µA, T_Q blocked	30			V
Output voltage (FLL 111 T/115 T)	V_Q	V_S=5.25 V, I_Q=250 µA, T_Q blocked	15			V
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1	mA
L-input- current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Supply current	I_S	V_S=5.25 V		43	70	mA

Delay times, V_S=5 V, T_A=25 °C

Propagation delay	t_{PLH}	C_L=15 pF, R_L=100 Ω			50	ns
	t_{PHL}	C_L=15 pF, R_L=100 Ω			50	ns

Logical data

Input load factor	F_I				1	



Pin configuration
top view

Truth table

BCD-inputs				decimal outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

FLL 121 – 7446
FLL 121 T – 7447
FLL 121 U – 7446 A
FLL 121 V – 7447 A

order numbers

FLL 121: Q67000–L10
FLL 121T: Q67000–L11
FLL 121U: Q67000–L51
FLL 121V: Q67000–L63

FLL 121: BCD-7-segment-decoder and driver with open collector output with 30 V/20 mA
FLL 121T: BCD-7-segment-decoder and driver with open collector output with 15 V/20 mA
FLL 121U: BCD-7-segment-decoder and driver with open collector output with 30 V/40 mA
FLL 121V: BCD-7-segment-decoder and driver with open collector output with 15 V/40 mA

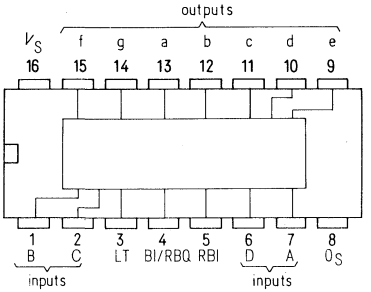
The FLL 121, T, U, V transform BCD-words with 4 bits present at the inputs A, B, C, D into the 7-segment-code. Control functions are provided by means of three auxiliary inputs (BI, RBI, LT). An L-signal at the ripple-blanking-input RBI suppresses the O-signal at the outputs. When the blanking-input BI is supplied with an L-signal, all outputs assume an H-state. The ripple-blanking-output RBQ (internally connected with BI) provides an automatic O-suppression over several decades. An L-signal at the lamp-test-input LT forces all segment outputs into L-state.
In addition the following maximum ratings apply:

Maximum ratings

			lower limit B	typ.	upper limit A	unit
Output voltage at						
outputs a through g (FLL 121, U)	V_Q	T_Q blocked	0		30	V
outputs a through g (FLL 121, T)	V_Q	T_Q blocked	0		15	V
Output current	I_Q	T_Q blocked	0		1	mA
Output current at						
outputs a through g (FLL 121, T)	I_{QL}	T_Q conducting	0		20	mA
outputs a through g (FLL 121, U)	I_{QL}	T_Q conducting	0		40	mA

Electrical characteristics
temperature range 1

		condition test	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage at						
outputs a through g (FLL 121,T)	V_{QL}	I_{QL}=20 mA, V_S=4.75 V		0.27	0.4	V
outputs a through g (FLL 121,U)	V_{QL}	I_{QL}=40 mA, V_S=4.75 V		0.27	0.4	V
L-output voltage at output BI/RBQ	V_{QL}	V_S=4.75 V, I_{QL}=8 mA		0.3	0.4	V
Output voltage at						
outputs a through g (FLL 121,U)	V_Q	I_Q=250 µA, V_S=5.25 V	30			V
outputs a through g (FLL 121,T)	V_Q	I_Q=250 µA, V_S=5.25 V	15			V
H-output voltage at output BI/RBQ	V_{QH}	V_S=4.75 V, $-I_{QH}$=200 µA	2.4	3.7		V
L-input current at						
input BI/RBQ	$-I_{IL}$	V_{IL}=0.4 V, V_S=5.25 V			4.2	mA
remaining inputs	$-I_{IL}$	V_{IL}=0,4 V, V_S=5.25 V			1.6	mA
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			40	µA
except BI/RBQ	I_I	V_I=5.5 V			1	mA
Short circuit output current at BI/RBQ	$-I_Q$	V_S=5.25 V			4	mA
Supply current	I_S	V_S=5.25 V, outputs open		64	103	mA



Pin configuration
top view

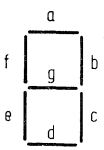
Delay times, V_S=5 V, T_A=25 °C

Propagation delay from A to any output	t_{PLH}	C_L=15 pF, R_L=280 Ω	100	ns
	t_{PHL}		100	ns
from RBI to any output	t_{PLH}		100	ns
	t_{PHL}		100	ns

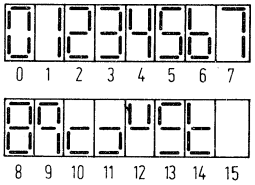
Logical data

Input load factor except BI/RBQ	F_I	1	
Input load factor at BI/RBQ	F_I	2.6	
Output load factor BI/RBQ	F_Q	5	

FLL 121
FLL 121 T
FLL 121 U
FLL 121 V



Segment identification



Output patterns

Truth Table

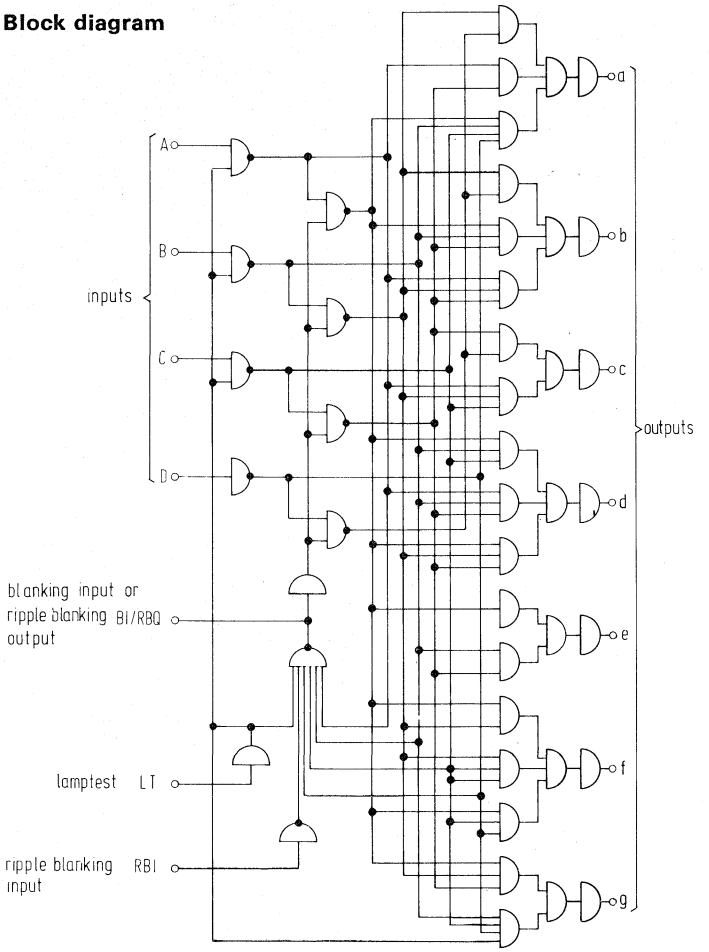
function	LT	RBI	D	C	B	A	BI/RBQ	a	b	c	d	e	f	g
0[1])	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI[2])	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI[3])	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT[4])	L	X	X	X	X	X	H	L	L	L	L	L	L	L

Notes:

X = H or L-signal

1) If O-indication is disired, RBI must be supplied with an H-signal.
2) An L-signal at BI forces all segment outputs into H-state independent of the other input conditions.
3) If an L-signal is supplied to RBI and A, B, C, D, H-signals result at all outputs and L-signal at RBQ (zerocondition).
4) An L-signal at LT switches all outputs to L only if BI/RBQ is supplied with an H-signal regardless of the input condition at A, B, C, D, and RBI.

Block diagram



FLL 131 – 49700
FLL 131 T – 49700–S1
FLL 135 – 49800
FLL 135 T – 49800–S1

order numbers

FLL 131:	Q67000–H236
FLL 131T:	Q67000–H668
FLL 135:	Q67000–H314
FLL 135T:	Q67000–L67

Dual AND-Powerdriver and Dual 2-Input NAND-Gate

The driver stages have open collector outputs with high breakdown voltages for high load currents:
FLL 131/135: 30 V/400 mA
FLL 131T/135T: 65 V/400 mA

Applications: lamp and relais drivers, line drivers.

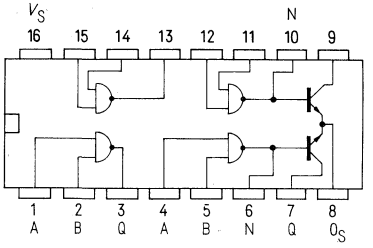
To avoid output spikes, line reflexions, and cross talk, the output transition times can be lengthened by means of a capacitor between the Q-output and the N-input. The N-terminals may not be used as control inputs or outputs.

In addition the following maximum ratings apply:

Maximum ratings

		lower limit B	upper limit A	unit
Output voltage at pins 7 and 10				
FLL 131/135	V_Q	0	30	V
FLL 131T/135T	V_Q	0	65	V
DC-current at pins 7 and 10				
one output (note 1)	I_Q	0	400	mA
both outputs simultaneously	I_Q	0	160	mA
Pulsed current at pins 7 and 10				
one output (note 2)	I_Q	0	400	mA
both outputs simultaneously	I_Q	depends on power consumption per package		
Power consumption per package T_A=70 °C	P		650	mW
T_A=85 °C	P		500	mW
Switching frequency	f		1	MHz

1) V_{QLA}=0.4 V not guaranteed
2) f_{max}=500 kHz, t_{TLH} and t_{THL}=≤ 50 ns, V_{QLA}=0.4 V not guaranteed



Pin configuration
top view

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage at outputs 3 and 13	V_{QH}	V_S=4.75 V, V_{IL}=0.8 V, $-I_{QH}$=400 µA	2.4	3.3		V
L-output voltage at outputs 3 and 13	V_{QL}	V_S=4.75 V, V_{IH}=2.0 V, I_{QL}=16 mA		0.22	0.4	V
L-output voltage at outputs 7 and 9	V_{QL}	I_{QL}=160 mA, V_S=4.75 V			0.4	V
	V_{QL}	I_{QL}=400mA, V_{IL}=0.8 V		0.4	0.8	V
H-output current at outputs 7 and 9	I_{QH}	V_S=4.75 V, V_{IH}=2.0 V, V_{QH}=30 V			500	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			40	µA
	I_I	V_I=5.5 V, V_S=5.25 V			1	mA
H-supply current	I_{SH}	V_S=5.25 V, V_{IH}=5.0 V			24	mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IL}=0 V			85	mA

Logical data

Input load factor	F_I			1	
Output load factor at outputs 3 and 13	F_Q			10	

Logic: outputs 3 and 13 $Q = \overline{AB}$
outputs 7 and 9 $Q = AB$

FLL 141 – 49701
FLL 145 – 49801

Order numbers

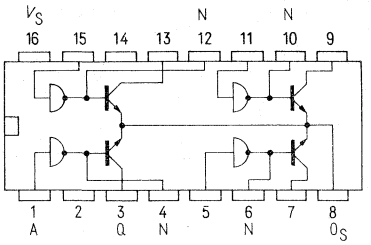
FLL 141: Q67000–H331
FLL 145: Q67000–H415

Quadruple Powerdriver for 30 V/80 mA

The driver stages have open collector outputs with high breakdown voltages for high load currents: 30 V/80 mA.
Applications: lamp and relais drivers, line drivers.
To avoid output spikes, line reflexions, and cross talk, the output transition times can be lengthened by means of a capacitor between the Q-output and the N-input. The N-terminals may not be used as control inputs or outputs.
In order to increase the maximum output current, a resistor $R_B \geqq 2.7\ k\Omega$ can be connected to the N-input and the supply voltage V_S.
In addition the following maximum ratings apply:

Maximum ratings		lower limit B	upper limit A	unit
Output voltage	V_Q		30	V
DC current				
one output at $R_B=\infty$	I_Q	0	130	mA
(note 1) $R_B=2.7\ k\Omega$	I_Q	0	200	mA
all putputs simultaneously	I_Q	0	80	mA
Pulsed current				
one output (note 2)	I_Q	0	130	mA
all outputs simultaneously	I_Q	depends on power consumption per package		
Power consumption per package				
$T_A=70\ °C$	P		650	mW
$T_A=85\ °C$	P		500	mW
Switching frequency	f		1	MHz

1) $V_{QLA}=0.4$ V not guaranteed
2) $f_{max}=500$ kHZ, t_{TLH} and $t_{THL} \leqq 50$ ns, $V_{QLA}=0.4$ V not guaranteed.



Pin configuration
top view

Electical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage at N-node	V_Q	V_S=4.75 V, V_{IH}=2.0 V, I_{QL}=2 mA			0.3	V
L-output voltage at Q-outputs $R_B=\infty$	V_{QL}	I_{QL}=80mA, V_S=4.75 V		0.3	0.4	V
R_B=2.7 kΩ	V_{QL}	I_{QL}=130mA, V_{IL}=0.8V		0.5	0.7	V
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			0.18	mA
H-input current, each input	I_{IH}	V_{IH}=2.4 V, V_S=5.25 V			10	µA
	I_I	V_I=5.5 V, V_S=5.25 V			100	µA
H-output current, each output	I_{QH}	V_S=4.75 V, V_{IH}=2.0 V, V_{QH}=30 V			500	µA
H-supply current	I_{SH}	V_S=5.25 V, V_{IH}=5.0 V			3	mA
L-supply current	I_{SL}	V_S=5.25 V, V_{IL}=0 V			60	mA

Logical data

Input load factor	F_I		0.25
Logic	$Q = A$		

FLQ 101 – 7489

order numbers
FLQ 101: Q67000–Q11

64-Bit RAM (Randum Access Memory)

The FLQ 101 is a fast scratch pad memory with a capacity of 16 4-bit-words.
Write-operation: Information present at the data inputs D_1, D_2, D_3, D_4, is written into the desired word location by means of the address-input A, B, C, D, while the enable inputs E_M and E_W are supplied with an L-level. The state of the read outputs Q_1, Q_2, Q_3, Q_4 will be complementary to the input information.
Read-operation: Read-out is non-destructive if the write enable input E_W is supplied with an H-signal. The word location is selected by means of the address-inputs. The Memory enable input E_M must be at L-level during read-operation.
Access time is 33 ns typically.
Wired-AND-connections of the open collector outputs permit an expansion up to 4096 words of n bits without additional circuit elements.

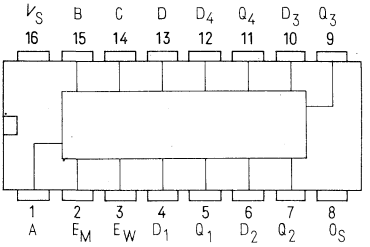
Electrical characteristics
temperature range 1

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.45	V
H-output current, each output	I_{QH}	V_S=4.75 V, V_{QH}=5.5 V			20	µA
Input current, each input	V_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Supply current	I_S	V_S=5.25 V, note 1		75	105	mA
Output capacitance	C_Q	V_S=5 V, V_Q=2.4 V, f=1 MHz		4		pF

Delay times, V_S=5 V, T_A=25 °C

Write enable pulse duration	t_W		40			ns
Setup time at D_1, D_2, D_3, D_4	t_S		40			ns
Hold time at D_1, D_2, D_3, D_4	t_H		5			ns
Setup time at A, B, C, D	t_S		0			ns
Hold time at A, B, C, D	t_H		5			ns
Write recovery time	t_{rH}	(initial state Q=H)		39	70	ns
	t_{rL}	(initial state Q=L)		48	70	ns
Propagation delay from E_M to Q	t_{PLH}	R_{L1}=300 Ω (between Q and V_S)		26	50	ns
	t_{PHL}	R_{L2}=600 Ω (between Q and O_S)		33	50	ns
from A, B, C, D to Q	t_{PLH}	C_L=30 pF		30	60	ns
	t_{PHL}			35	60	ns

[1]) I_S is measured at E_M = L and all other inputs at H.



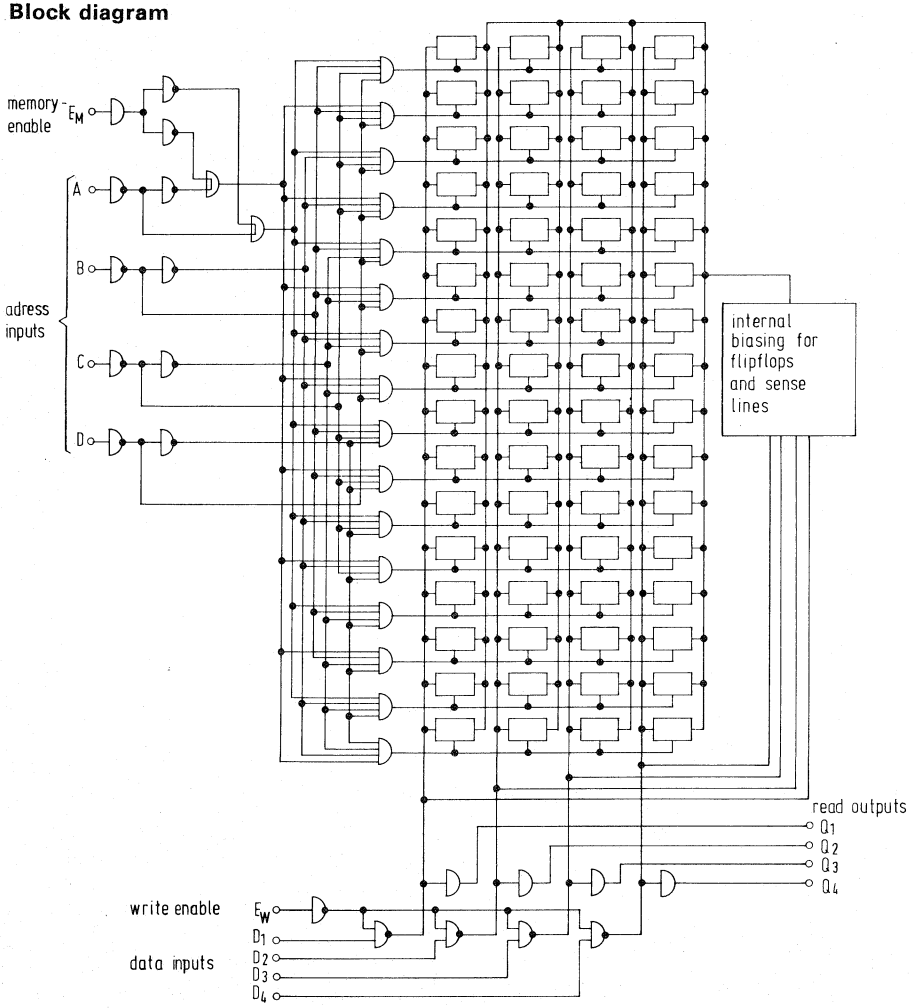
Pin configuration
top view

Truth table

memory enable E_M	write enable E_W	memory operation mode	output state
L	L	write	complement of data inputs
L	H	read	complement of selected word
H	L	inhibit	complement of data inputs
H	H	inhibit	Q = H

FLQ 101

Block diagram



order numbers

FLQ 111: Q67000–J27
FLQ 121: Q67000–J163

FLQ 111 – 7481 A
FLQ 121 – 7484 A

16-Bit RAM (Randum Access Memory)

The FLQ 111 is a fast scratch pad memory with direct access. Read-out is non-destructive. The FLQ 121 has 2 additional write inputs W_{H2} and W_{L2}.

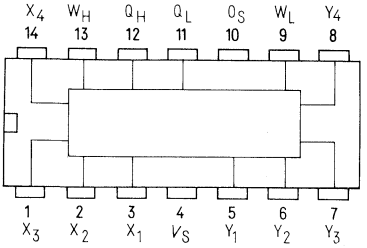
Electrical characteristics temperature range 1		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage at X or Y	V_{IH}	V_S=4.75 V, V_{QL}≦0.4 V I_{QL}=40 mA	2.0			V
H-input voltage at W_H or W_L	V_{IH}	V_S=4.75 V, V_{QL}≦0.4 V I_{QL}=40 mA	2.0			V
L-input voltage at X or Y, write inhibit	V_{IL}	V_S=4.75 V, V_{QL}≦0.4 V I_{QL}=40 mA			0.8	V
L-input voltage at X or Y, read inhibit	V_{IL}	V_S=4.75 V, V_{QH}=5.5 V I_{QH}=250 µA			1.0	V
L-input voltage at W_H or W_L, write inhibit	V_{IL}	V_S=4.75 V, V_{QL}≦0.4 V I_{QL}=40 mA			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V I_{QH}=250 µA	5.5			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=40 mA			0.4	V
L-input current each W_H or W_L	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
L-input current at any X or Y inputs	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			11	mA
H-input current each W_H or W_L input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
		V_S=5.25 V, V_{IH}=5.5 V			1.0	mA
H-input current each X or Y input	I_{IH}	V_S=5.25 V, V_{IH}=4.5 V			400	µA
		V_S=5.25 V, V_{IH}=5.5 V			3.0	mA
Supply current	I_S	V_S=5.25 V		45	65	mA

Delay times, V_S=5 V, T_A=25 °C

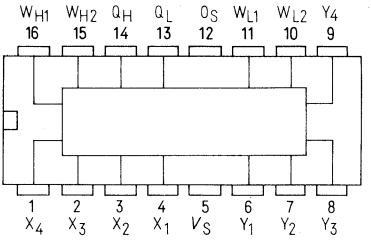
Write-read-recovery time	t_r	C_L=30 pF X_1—Y_1 location adressed			30	ns
Propagation delay from XY to Q_H or Q_L	t_{PHL}	C_L=30 pF X_1—Y_1 location addresssed		12	20	ns
	t_{PLH}	C_L=30 pF X_1—Y_1 location addressed		12	19	ns
	t_{PLH}	C_L=30 pF X_1 through X_4 and Y_1 location addressed		11	19	ns
	t_{PHL}	C_L=30 pF X_1 through X_4 and Y_1 location addressed		13	20	ns

FLQ 111
FLQ 121

FLQ 111

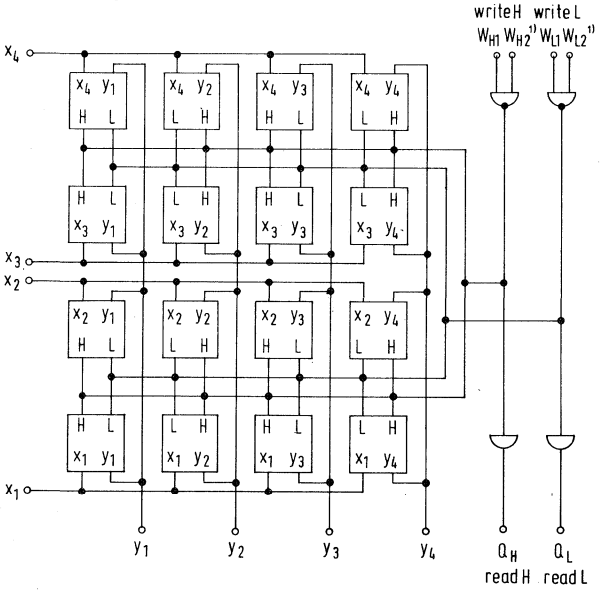


FLQ 121



Pin configurations, top view

Block diagram FLQ 111 and FLQ 121



Note: 1) inputs W_{H2} and W_{L2} FLQ 121 only

order numbers

FLQ 131: Q67000–Q6

FLQ 131 – 74170

16-Bit-RAM, 4 words of 4 bits

The FLQ 131 is a fast scratch pad memory for simultaneous read/write-operation. Recovery times are thus eliminated.
Information present at the data inputs D_1, D_2, D_3, D_4 is writen into the word location by means of the write inputs W_A and W_B while the write enable input E_W is supplied with an L-signal. Write time is 45 ns typically.
The outputs Q_1, Q_2, Q_3, Q_4 supply the desired word information addressed by the read inputs R_A and R_B while the read enable input E_R is supplied with an L-signal. Read-out is non-destructive. Read time is 35 ns typically.
Memory expansion is possible by means of wired-AND-connections of the open collector outputs.

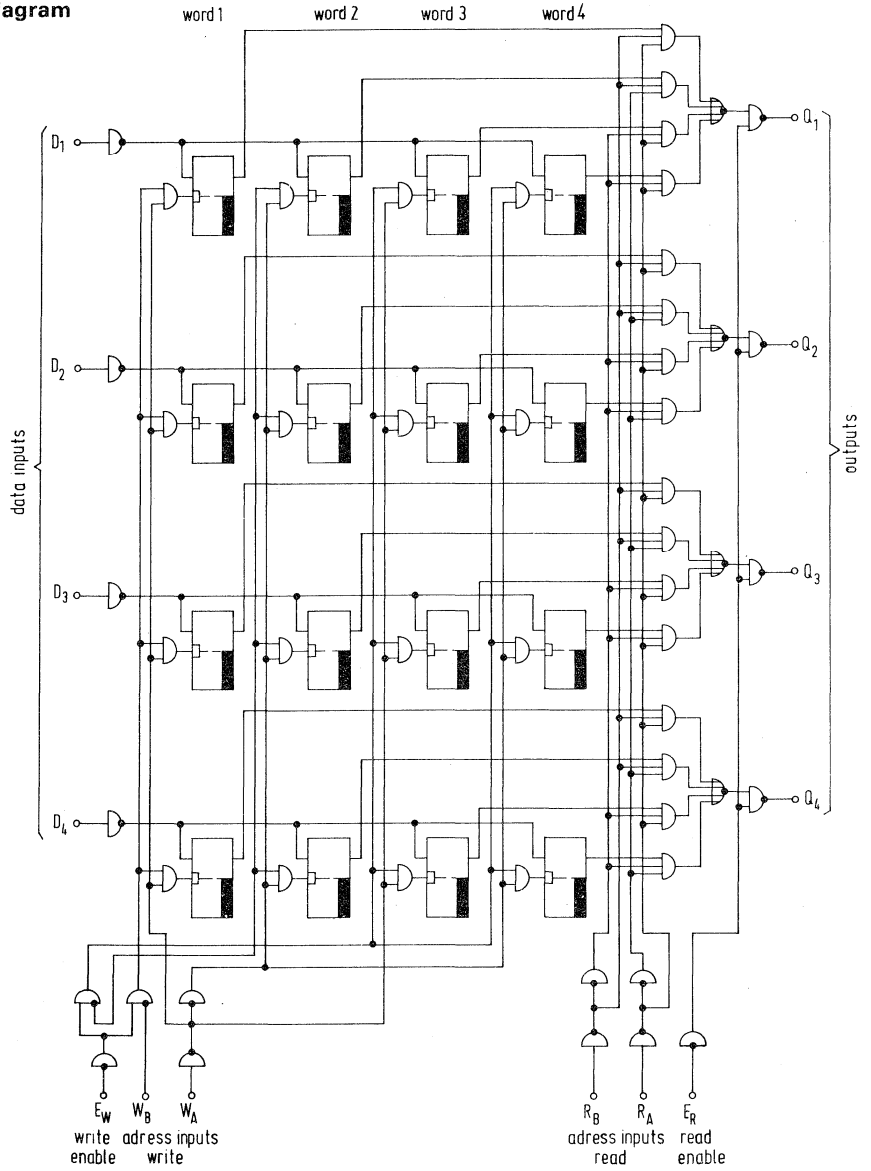
Electrical characteristics temperature range 1		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75		5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
H-output current, each output	I_{QH}	V_S=4.75 V, V_{QH}=5.5 V			30	µA
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Supply current	I_S	V_S=5.25 V duty cycle 1:1		127	140	mA

Delay times, V_S=5 V, T_A=25 °C

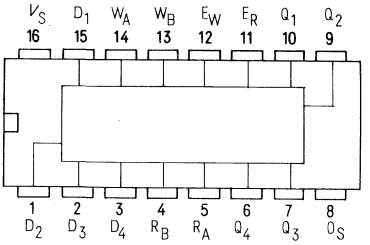
Write and read enable pulse duration	$t_{W,R}$		25			ns
Setup time						
at D_1, D_2, D_3, D_4	t_S		10			ns
at W_A, W_B	t_S		15			ns
at R_A, R_B	t_S		5			ns
Hold time at D_1, D_2, D_3, D_4	t_H		0			ns
at W_A, W_B	t_H		5			ns
at R_A, R_B	t_H		5			ns
Write recovery time	t_r		25			ns
Propagation delay from E_R to Q	t_{PLH}	R_L=400 Ω, C_L=15 pF		20	15	ns
	t_{PHL}			20	30	ns

FLQ 131

Block diagram



FLQ 131



Pin configuration
top view

Truth table

Write function

adress		enable	word			
W_S	W_A	E_W	1	2	3	4
L	L	L	Q=D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q=D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q=D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q=D
X	X	H	Q_n	Q_n	Q_n	Q_n

Read function

adress		enable	data outputs			
R_B	R_A	E_R	Q_1	Q_2	Q_3	Q_4
L	L	L	W1B1	W1B2	W1B3	W1B4
L	H	L	W2B1	W2B2	W2B3	W2B4
H	L	L	W3B1	W3B2	W3B3	W3B4
H	H	L	W4B1	W4B2	W4B3	W4B4
X	X	H	H	H	H	H

X=H or L-signal
Q=D = Information at D is writen into word location
Q_n = Memory content remains unchanged
W1B1 = bit 1 of word 1 is present at Q-output

FLY 101 – 7460
FLY 105 – 8460

order numbers
FLY 101: Q67000–Y1
FLY 105: Q67000–Y18

Dual 4-Input Expander for FLH 151, FLH 171, FLH 511, FLH 155, FLH 175, and FLH 515

Electrical characteristics

temperature ranges 1 and 5, if not indicated otherwise

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	17	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	18			0.8	V
Output voltage T_Q conducting	V_N	V_S=4.75 V V_{IH}=2 V, V_{N2}=1 V R_L=1.1 kΩ, T_A=0 °C	17			0.4	V
H-input current, each input	I_{IH}	V_{IH}=2.4 V | V_S	19			40	µA
	I_I	V_I=5.5 V | =5.25 V	19			1	mA
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	18			1.6	mA
Output current, each gate, T_Q conducting	$-I_N$	V_S=4.75 V V_{IH}=2 V, V_{N2}=1 V	20	0.43			mA
Output current each gate, T_Q blocked	I_N	V_S=4.75 V V_{IL}=0.8 V V_{N1}=4.5V, R_L=1.2 kΩ T_A=0 °C	18			270	µA
Supply current T_Q conducting	I_S	V_S=5.25 V V_I=5 V V_{N2}=0.85 V	21		1.2	2.5	mA
Supply current T_Q blocked	I_S	V_S=5.25 V V_I=0 V, V_{N2}=0.85 V	21		2	4	mA

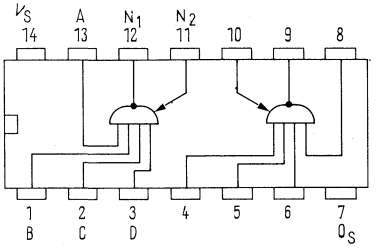
Delay times, in connection with FLH 151, 155, 171, 175, 511, 515, V_S=5 V, T_A=25 °C

Propagation delay	t_{PHL} t_{PLH}	} C_1=15 pF, F_Q=10	23		10 15	20 30	ns ns

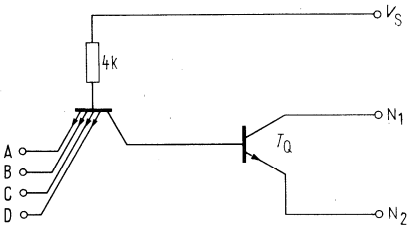
Logical data

Input load factor	F_I					1	
Logic	exp. = ABCD						

Note: Up to 4 expanders FLY 101/105 can be connected to the expander nodes N_1 and N_2 of the gates FLH 151/155, FLH 171/175, and FLH 511/515.



Pin configuration
top view



Schematic
(each gate)

FLY 111 – 74150
FLY 115 – 84150

order numbers

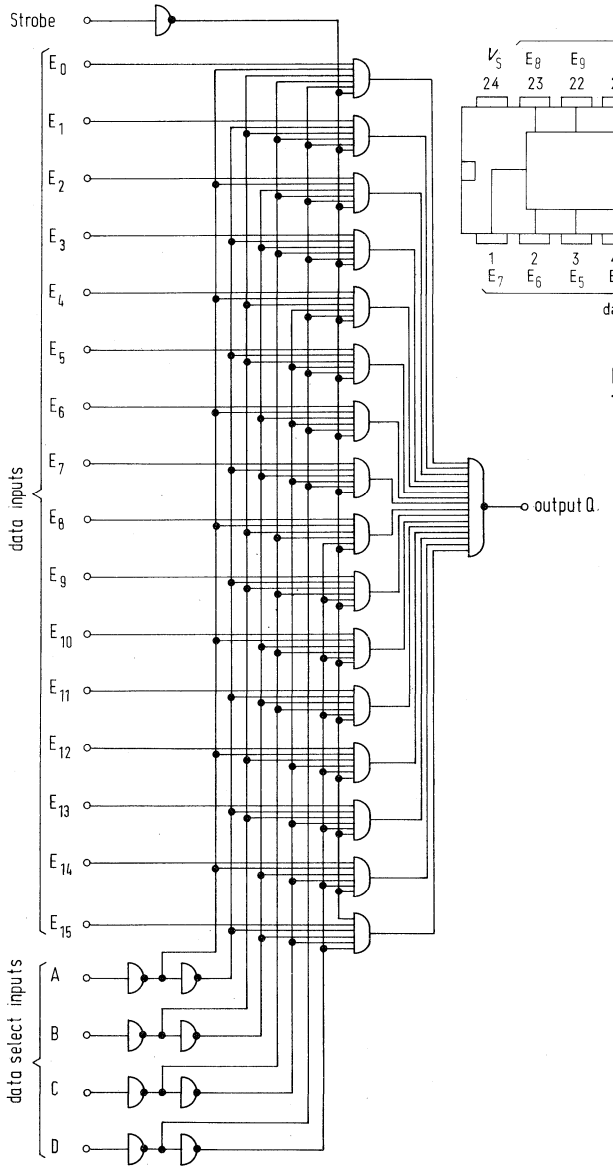
FLY 111: Q67000–Y31
FLY 115: Q67000–Y46

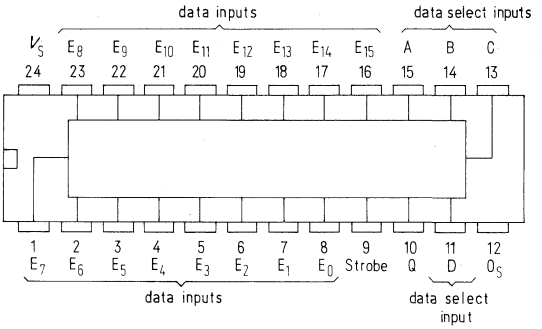
Data Selector/Multiplexer, 4 Bits

The FLY 111/115 have 16 data inputs E_0 through E_{15}. The desired data input is selected by means of the binary data-select-inputs A, B, C, D. The information present at the data input (H- or L-signal) is transferred to the Q-output in complementary form. An H-level at the strobe input switches the output to Q=H independent of any other input condition.
Application: serial data transmissions in connection with the demultiplexers FLY 141/145.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current	$-I_Q$	V_S=5.25 V, V_{QL}=0 V	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=4.5 V		40	68	mA
Delay times, V_S=5 V, T_A=25 °C, F_Q=10						
Propagation delay from A, B, C, D to $\overline{Q}$	t_{PHL}	R_L=400 Ω, C_L=30 pF		20	30	ns
	t_{PLH}			35	52	ns
from A, B, C, D to Q	t_{PHL}			22	33	ns
	t_{PLH}			23	35	ns
from strobe to $\overline{Q}$	t_{PHL}			19	30	ns
	t_{PLH}			35	52	ns
from strobe to Q	t_{PHL}			21	30	ns
	t_{PLH}			15.5	24	ns
from E_0 through E_{15} to Q	t_{PHL}			8.5	14	ns
	t_{PLH}			13	20	ns
Logical data						
Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor, each input	F_I				1	

Block diagram





Pin configuration
top view

FLY 111
FLY 115

Truth table

D	C	B	A	Strobe	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	Q
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

H or L-signal

Order numbers

FLY 121: Q67000–Y30
FLY 125: Q67000–Y29

FLY 121 – 74151
FLY 125 – 84151

Data Selector/Multiplexer, 8 Bits

The FLY 121/125 have 8 data inputs E_0 through E_7. The desired data input is selected by means of the binary data-select-inputs A, B, C. The information present at the data input (H or L-signal) is transferred to the Q-output in complementary form. An H-level at the strobe input switches the output to Q=H independent of any other input condition.
Application: serial data transmissions in connection with the demultiplexers FLY 141/145, FLY 151/155, and FLY 161/165.

Electrical characteristics
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V, V_Q=0 V	18		55	mA
Supply current	I_S	V_S=5.25 V, V_I=4.5 V		29	48	mA

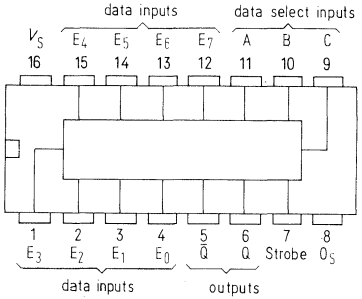
Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Propagation delay from A, B, C to $\overline{Q}$	t_{PHL}	R_L=400 Ω, C_L=30 pF		20	30	ns
	t_{PLH}			35	52	ns
from A, B, C to Q	t_{PHL}			22	33	ns
	t_{PLH}			23	35	ns
from strobe to $\overline{Q}$	t_{PHL}			19	30	ns
	t_{PLH}			35	52	ns
from strobe to Q	t_{PHL}			21	30	ns
	t_{PLH}			15.5	24	ns
from E_0 through E_7 to $\overline{Q}$	t_{PHL}			16	24	ns
	t_{PLH}			19	29	ns
from E_0 through E_7 to Q	t_{PHL}			8.5	14	ns
	t_{PLH}			13	20	ns

Logical data

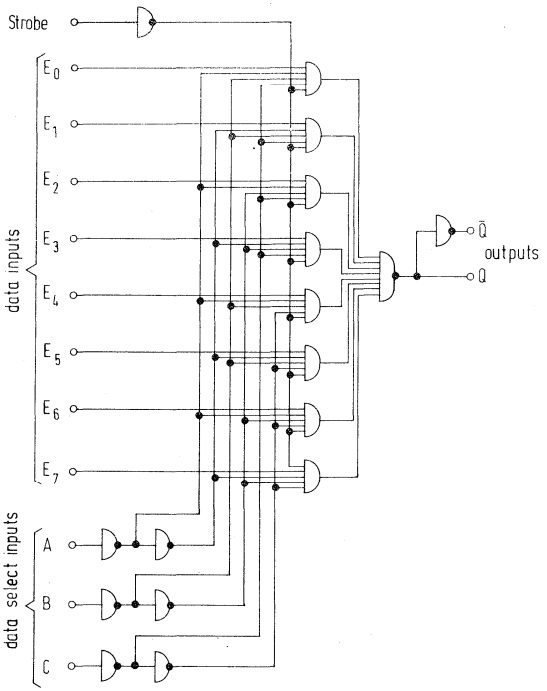
Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor, each input	F_I				1	

FLY 121
FLY 125



Pin configuration
top view

Block diagram



Truth table

C	B	A	Strobe	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	$\bar{Q}$	Q
X	X	X	H	X	X	X	X	X	X	X	X	H	L
L	L	L	K	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	H	L	X	L	X	X	X	X	X	X	H	L
L	L	H	L	X	H	X	X	X	X	X	X	L	H
L	H	L	L	X	X	L	X	X	X	X	X	H	L
L	H	L	L	X	X	H	X	X	X	X	X	L	H
L	H	H	L	X	X	X	L	X	X	X	X	H	L
L	H	H	L	X	X	X	H	X	X	X	X	L	H
H	L	L	L	X	X	X	X	L	X	X	X	H	L
H	L	L	L	X	X	X	X	H	X	X	X	L	H
H	L	H	L	X	X	X	X	X	L	X	X	H	L
H	L	H	L	X	X	X	X	X	H	X	X	L	H
H	H	L	L	X	X	X	X	X	X	L	X	H	L
H	H	L	L	X	X	X	X	X	X	H	X	L	H
H	H	H	L	X	X	X	X	X	X	X	L	H	L
H	H	H	L	X	X	X	X	X	X	X	H	L	H

X = H or L-signal

FLY 131 – 74153
FLY 135 – 84153

order numbers

FLY 131: Q67000–Y54
FLY 135: Q67000–Y58

Dual Data Selector/Multiplexer, 4 Bits

The FLY 131/135 have 4 data inputs each $1C_0$ through $1C_3$ and $2C_0$ through $2C_3$. The desired data inputs are selected by the common data-select-inputs A, B. An H-signal at the strobe inputs switches the outputs 1Q and 2Q to H independent of any other input condition.
Application: serial data transmission in connection with the demultiplexers FLY 151/155 and FLY 161/165.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, $-I_{QH}$=800 µA	2.4	3.1		V
L-output voltage	V_{QL}	V_S=4.75 V, I_{QL}=16 mA		0.2	0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	I_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V, V_I=0 V		36	60	mA

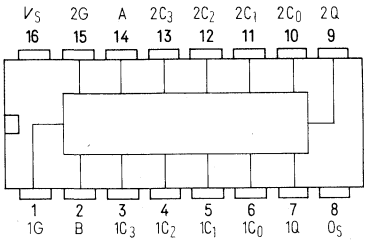
Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Propagation delay from C_0, C_1, C_2, C_3 to Q	t_{PLH}	R_L=400 Ω, C_L=30 pF		12	18	ns
	t_{PHL}			15	23	ns
from A and B to Q	t_{PLH}			22	34	ns
	t_{PHL}			22	34	ns
from G to Q	t_{PLH}			19	30	ns
	t_{PHL}			15	23	ns

Logical data

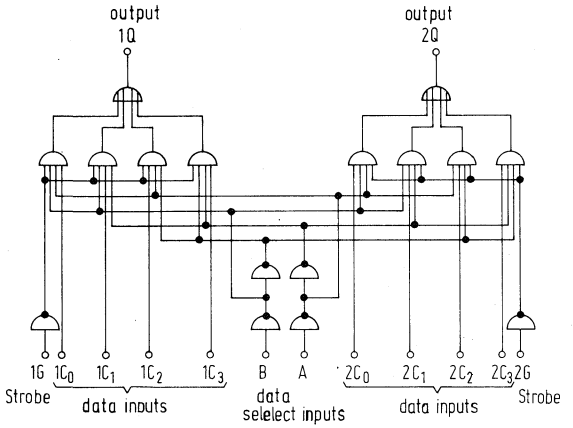
Output load factor	H-signal	F_{QH}			20	
	L-signal	F_{QL}			10	
Input load factor		F_I			1	

FLY 131
FLY 135



Pin configuration
top view

Block diagram



Truth table

data-select inputs		data inputs				strobe	output
B	A	C_0	C_1	C_2	C_3	G	Q
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

X = H or L-signal
A and B are joint inputs.

FLY 141 – 74154
FLY 145 – 84154

order numbers

FLY 141: Q67000–Y45
FLY 145: Q67000–Y51

Binary Decoder/Demultiplexer, 4 Bits

The FLY141/145 decode binary coded 4-bit-words into the decimal numbers 0 to 16. An H-signal at G_1 or G_2 switches all outputs to Q=H independent of any other input condition.
Application: Decoder for the binary counters FLJ 181/185, FLJ 211/215, FLJ 251/255, FLJ 391/395, FLJ 411/415, FLJ 431/435. Serial data transmission in connection with the multiplexer FLY 111/115.

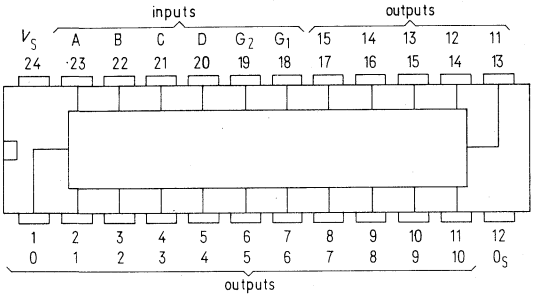
Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75		5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage	V_{QH}	V_S=4.75 V, V_{IH}=2 V, V_{IL}=0.8 V, $-I_{QH}$=800 µA	2.4			V
L-output voltage	V_{QL}	V_S=4.75 V, V_{IH}=2 V, V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 , V_I=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_I=0.4 V			1.6	mA
Short circuit output current, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		34		mA

Delay times, V_S=5 V, T_A=25 °C, F_Q=10

Propagation delay from A, B, C	t_{PLH}	R_L=400 Ω, C_L=15 pF		24	36	ns
or D to the outputs	t_{PHL}			22	33	ns
Propagation delay from G_1	t_{PLH}			20	30	ns
or G_2 to the outputs	t_{PHL}			18	27	ns

Logical data

Output load factor H-signal	F_{QH}				20	
L-signal	F_{QL}				10	
Input load factor, each input	F_I				1	



Pin configuration
top view

Truth table

G_1	G_2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
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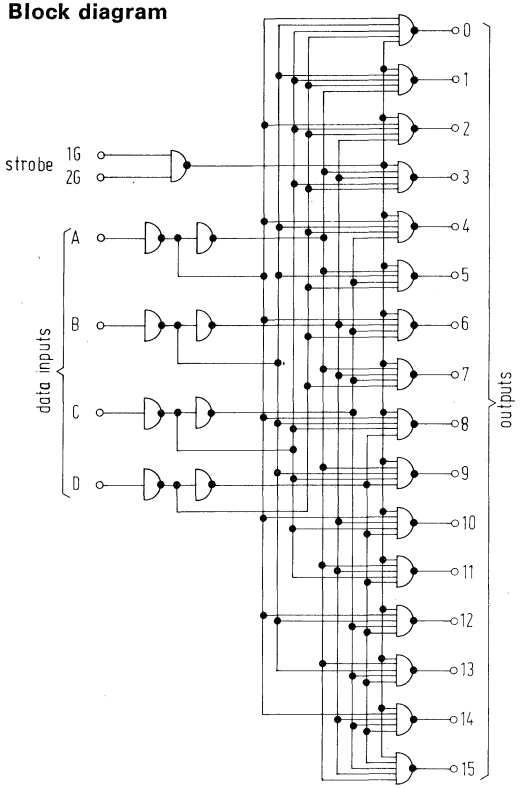
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = H or L-signal

FLY 141
FLY 145

Block diagram



order numbers

FLY 151: Q67000–Y52
FLY 155: Q67000–Y59
FLY 161: Q67000–Y55
FLY 165: Q67000–Y60

FLY 151 – 74155
FLY 155 – 84155
FLY 161 – 74156
FLY 165 – 84156

Dual Binary Decoder/Demultiplexer, 2 Bits

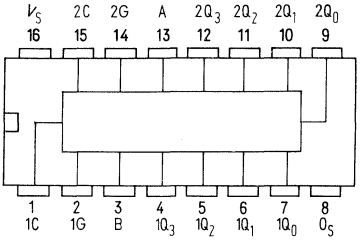
The FLY 151/155 have a push-pull output stage. The FLY 161/165 have open collector outputs.
Applications:
Dual 2 bit binary decoder and 3 bit binary decoder.
Dual 2 bit demultiplexer in connection with the multiplexer FLY 131/135. 3 bit demultiplexer in connection with the multiplexer FLY 121/125.
The functions and the required connections to achieve 3-bit-operation are shown in the truth tables.

Electrical characteristics temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V			0.8	V
H-output voltage of FLY 151/155	V_{QH}	V_S=4.75 V, V_{IH}=2.0 V, $-I_{QH}$=800 µA	2.4			V
H-output current of FLY 161/165, each output	I_{QH}	V_S=4.75 V, V_{IH}=2.0 V, V_{QH}=5.5 V			250	µA
L-output voltage	V_{QL}	V_S=4.75 V, V_{IL}=0.8 V, I_{QL}=16 mA			0.4	V
Input current, each input	I_I	V_S=5.25 V, V_I=5.5 V			1	mA
H-input current, each input	I_{IH}	V_S=5.25 V, V_{IH}=2.4 V			40	µA
L-input current, each input	$-I_{IL}$	V_S=5.25 V, V_{IL}=0.4 V			1.6	mA
Short circuit output current of FLY 151/155, each output	$-I_Q$	V_S=5.25 V	18		57	mA
Supply current	I_S	V_S=5.25 V		25	40	mA

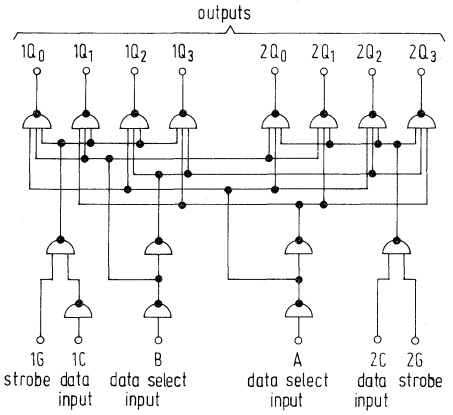
Delay times, V_S=5 V, T_A=25 °C, F_Q=10

FLY 151/155						
Propagation delay						
from A, B, 2C, 1G, 2G to Q	t_{PLH}	R_L=400 Ω, C_L=15 pF		13	20	ns
at 2 logic levels	t_{PHL}			18	27	ns
from A or B to Q	t_{PLH}			21	32	ns
at 3 logic levels	t_{PHL}					
from 1C to Q	t_{PLH}			16	24	ns
	t_{PHL}			20	30	ns
FLY 161/165						
Propagation delay						
from A, B, 2C, 1G, 2G to Q	t_{PLH}	R_L=400 Ω, C_L=15 pF		15	23	ns
at 2 logic levels	t_{PHL}			20	30	ns
from A or B to Q	t_{PLH}			23	34	ns
at 3 logic levels	t_{PHL}			23	34	ns
from C to Q	t_{PLH}			18	27	ns
	t_{PHL}			22	33	ns

FLY 151
FLY 155
FLY 161
FLY 165



Pin configuration
top view



Block diagram

Logical data		upper limit A
Output load factor H-signal at FLY 151/155	F_{QH}	20
Output load factor	F_{QL}	10
Input load factor	F_I	1

Truth table: Dual 2 bit binary decoder/demultiplexer

data select inputs B	A	strobe 1G	data input 1C	outputs $1Q_0$	$1Q_1$	$1Q_2$	$1Q_3$	strobe 2G	data input 2C	outputs $2Q_0$	$2Q_1$	$2Q_2$	$2Q_3$
X	X	H	X	H	H	H	H	H	X	H	H	H	H
L	L	L	H	L	H	H	H	L	L	L	H	H	H
L	H	L	H	H	L	H	H	L	L	H	L	H	H
H	L	L	H	H	H	L	H	L	L	H	H	L	H
H	H	L	H	H	H	H	L	L	L	H	H	H	L
X	X	X	L	H	H	H	H	X	H	H	H	H	H

Truth table: 3-bit binary decoder/demultiplexer

data-select-inputs C[1])	B	A	strobe or data-inputs G[2])	outputs $2Q_0$	$2Q_1$	$2Q_2$	$2Q_3$	$1Q_0$	$1Q_1$	$1Q_2$	$1Q_3$
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

[1]) C=1C and 2C connected
[2]) G=1G and 2G connected

X=H- or L-singnal

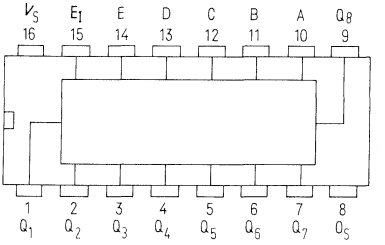
FL 100 - Series

Digital Integrated Circuits

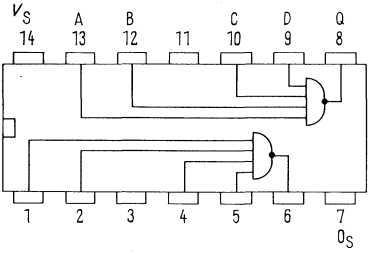
Series FL 100, data sheets on request

Type Order number	Function
FLH 561 74184 Q 67000–H 619	**6-Bit-Binary-BCD-Converter**
FLH 565 84184 Q 67000–H 592	
FLH 571 74185 A Q67000–H605	**6-Bit-Binary-BCD-Converter**
FLH 575 84185 Q 67000–H 622	

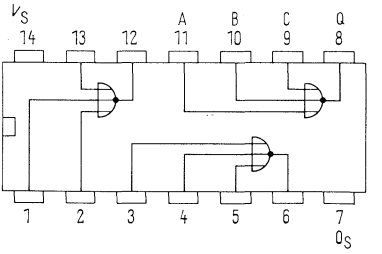
Pin configuration, top view

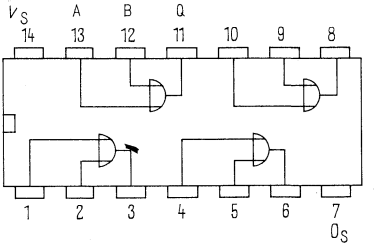
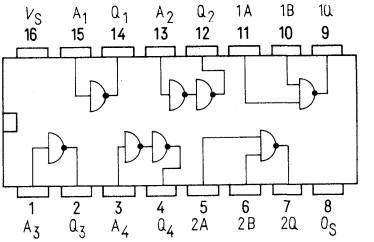
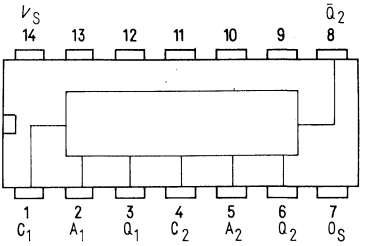


FLH 611 7422 Q 67000–H625	**Dual 4-Input NAND-Gate with Open Collector Output**
FLH 615 8422 Q 67000–H 626	

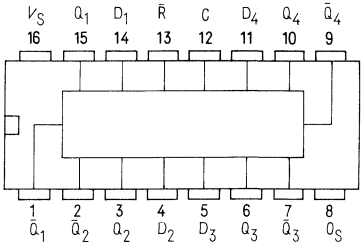


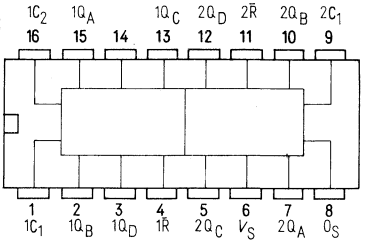
FLH 621 7427 Q 67000–H586	**Triple 3-Input NOR-Gate**
FLH 625 8427 Q 6700–H 589	

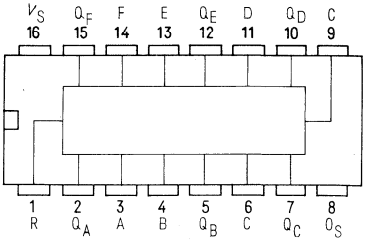


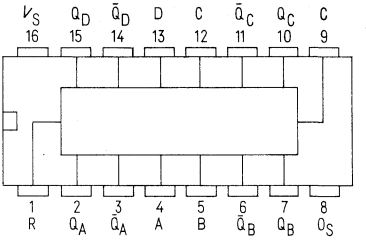
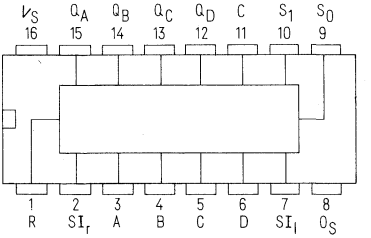
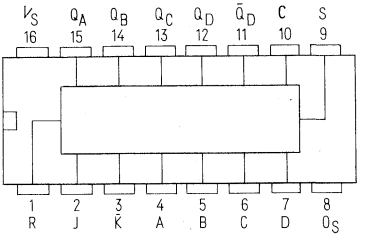
Type order number	Function	Pin configuration, top view
FLH 631 7432 Q67000–H491 **FLH 635** 8432 Q 67000–H 593	**Quadruple 2-Input OR-Gate**	
FLH 641 49703 Q67000–H 604 **FLH 645** 49803 Q 67000–H 632	**Delay Elements**	
FLJ 481 4932 Q 67000–J 72 **FLJ 485** 49832 Q 67000–J 152	**Dual 8-Bit-Shiftregister**	

FL 100 - Series

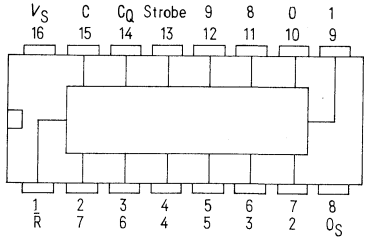
Type order number	Function	Pin configuration, top view
FLJ 491 49702 Q 67000–J 259 **FLJ 495** 49802 Q 67000–J 151	**Quadruple D-Flipflop with Common Reset**	

FLJ 501 49704 Q67000–J 371 **FLJ 505** 49804 Q 67000–J 372	**Dual Binary Counter for 50 MHz**	
FLJ 511 49705 Q67000–J 373 **FLJ 515** 49805 Q 67000–J 374	**Dual Decimal Counter for 50 MHz**	

FLJ 531 74174 Q67000–J349 **FLJ 535** 84174 Q 67000–J 351	**Hex-D-Flipflop with Common Reset**	

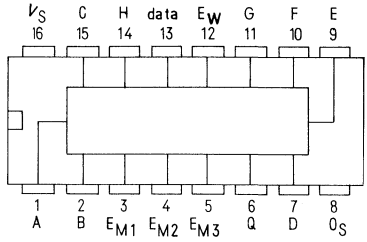
Type Order number	Function	Pin configuration, top view
FLJ 541 74175 Q 67000–J 379 **FLJ 545** 84175 Q 67000–J 352	**Quadruple-D-Flipflop with Common Reset**	
FLJ 551 74194 Q67000–J 350 **FLJ 555** 84194 Q 67000–J 353	**Synchronous 4-Bit-Parallel Shiftregister, Reversible**	
FLJ 561 74195 Q 67000–J 286 **FLJ 565** 84195 Q 67000–J 384	**Synchronous 4-Bit-Parallel Shiftregister with J-$\overline{K}$-Inputs**	

FL 100 - Series

Type order number	Function	Pin configuration, top view
FLQ 141 74200 Q 67000–Q 20	**256-Bit-RAM with Tristate Outputs**	

FLL 151 74142
Q 67000–L57

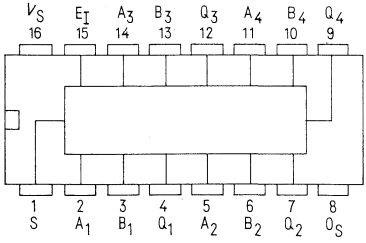
Decimal Counter, Latch, Decoder and Driver for Indicator tubes



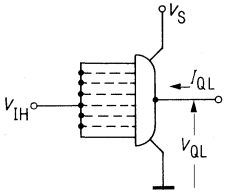
FLY 171 74157
Q 67000–Y75

FLY 175 84157
Q 67000–Y 71

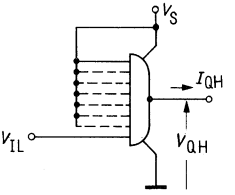
Quadruple Data Selector/Multiplexer, 2 Bits



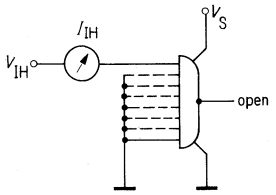
Test circuits (gates)



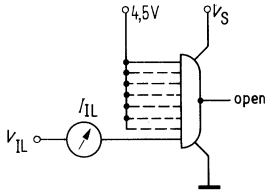
test circuit 1



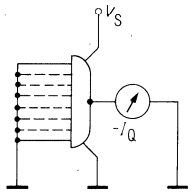
test circuit 2



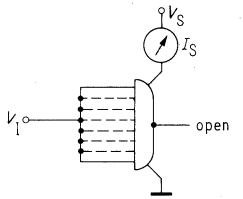
test circuit 3



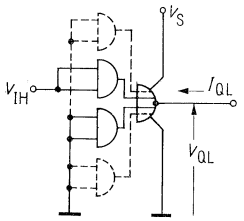
test circuit 4



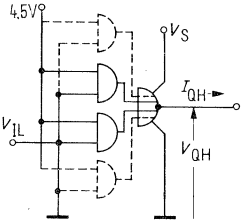
test circuit 5



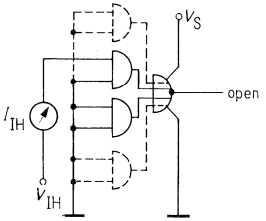
test circuit 6



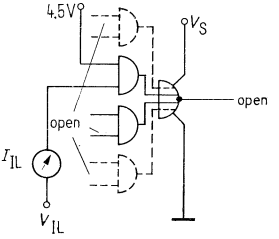
test circuit 7



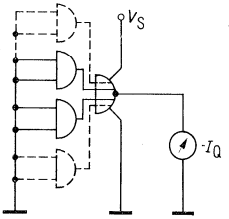
test circuit 8



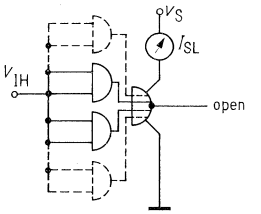
test circuit 9



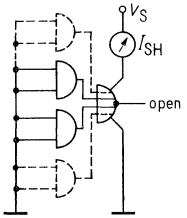
test circuit 10



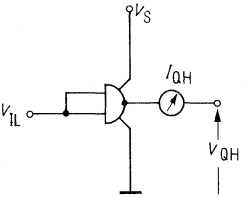
test circuit 11



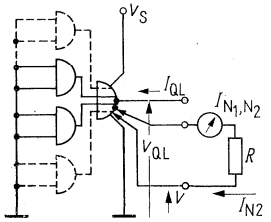
test circuit 12



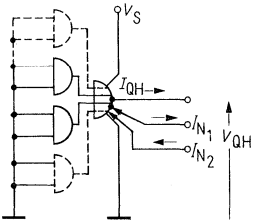
test circuit 13



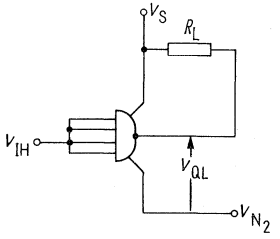
test circuit 14



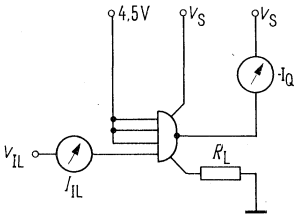
test circuit 15



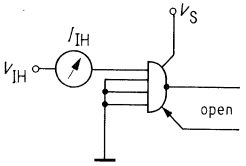
test circuit 16



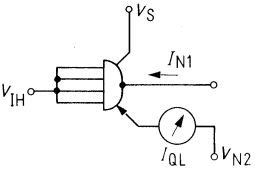
test circuit 17



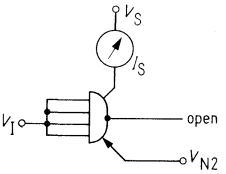
test circuit 18



test circuit 19

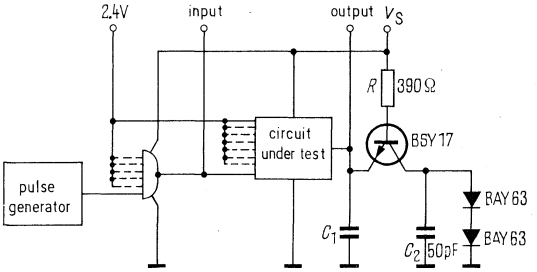


test circuit 20



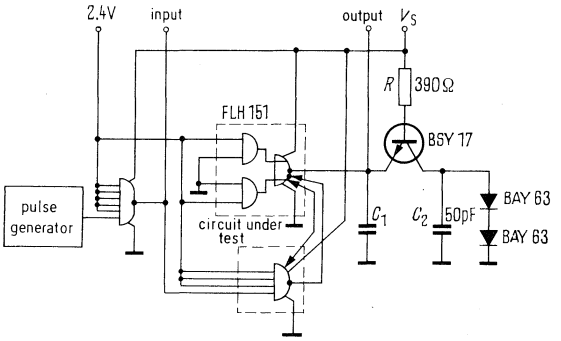
test circuit 21

Test circuit for delay times (gates)

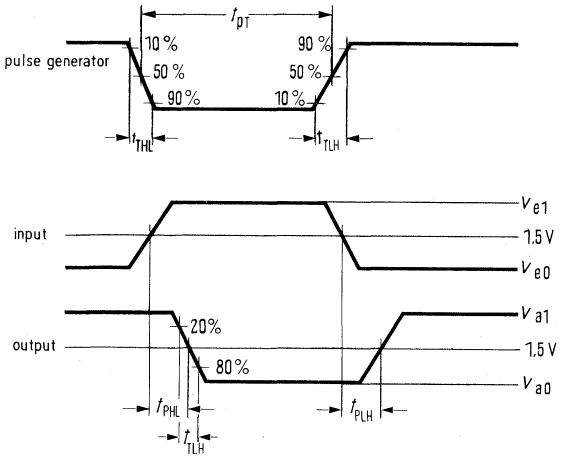


test circuit 22

notes for test circuit 22
for FLH 141: $R = 130\ \Omega$, $C_2 = 150$ pF
with AND/OR gates one input of the AND gate not used is grounded
notes for test circuits 22 and 23
generator: $t = t_r < 5$ ns, $t_p = 0.5\ \mu$s, $f = 1$ MHz
C_1 includes probe and jig capacitance

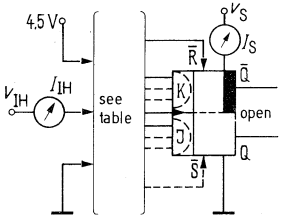


test circuit 23

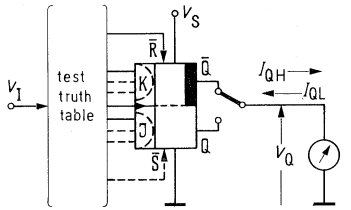


Pulse diagram
for test circuits 22 and 23

Test circuits (Flipflops)



test circuit 24 each output is tested separately



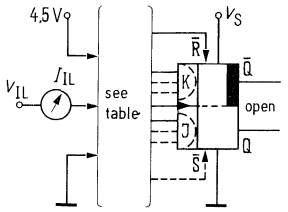
test circuit 25

V_{IH} to	ground	ground momentarily, then apply 4.5 V
J1 or J[1])	C, $\bar{R}$, J2, J3	
J2	C, $\bar{R}$, J1, J3	
J3	C, $\bar{R}$, J1, J2	
K1 or K[1])	C, $\bar{S}$, K2, K3	R[2])
K2	C, $\bar{S}$, K1, K3	
K3	C, $\bar{S}$, K1, K2	
R	C, J1 or J[1]), J2, J	
$\bar{S}$	C, K1, K2, K3	
C	$\bar{S}$, $\bar{R}$, J1 or J[1]), J2 J3, K1 or K[1]), K2, K3	
I_S apply V_{IH} to all inputs		

notes for test circuits 24 to 26

[1]) AND gates (dashed lines) apply for FLJ 111 only; FLJ 121, 131 have direct J- and K-inputs. FLJ 121 has no $\bar{S}$ input.
[2]) applies only for testing FLJ 121.

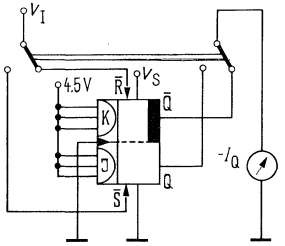
FL 100



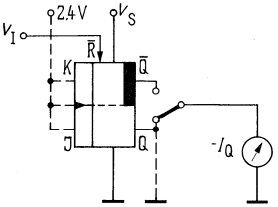
test circuit 26

apply V_{IL} to	ground momentarily then apply 4.5 V to	4.5 V	ground
J1 or J[1])	$\bar{R}$	C, J2, J3	
J2	$\bar{R}$	C, J1, J3	
J3	$\bar{R}$	C, J1, J2	
K1 or K[1])	$\bar{S}$	C, K2, K3	$\bar{Q}$[2])
K2	$\bar{S}$	C, K1, K3	
K3	$\bar{S}$	C, K1, K2	
$\bar{R}$		K2, K3	
$\bar{S}$		K1 or K[1])	
C	$\bar{S}$	J1 or J[1])	
C	$\bar{R}$	J2, J3	

when testing FLJ 121, 131 ground all inputs of unused flip-flop.



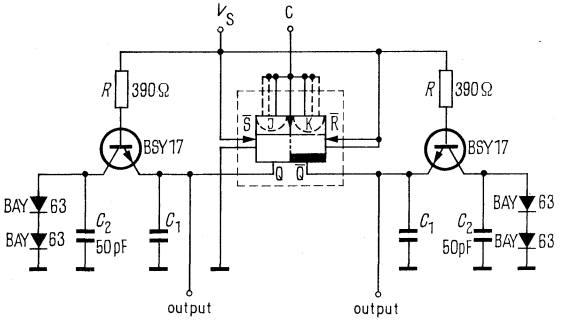
test circuit 27



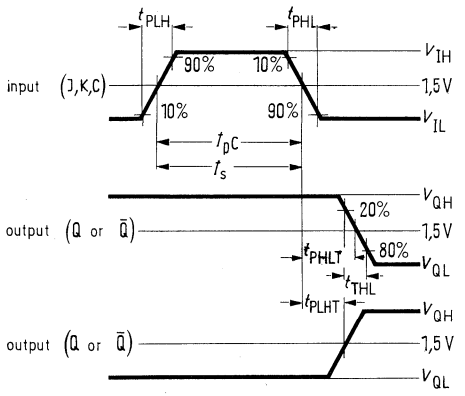
test circuit 28

circuit for testing $\bar{Q}$; when testing Q open all inputs and ground $\bar{Q}$; test duration 100 ms.

Test circuits for delay times (flipflops)

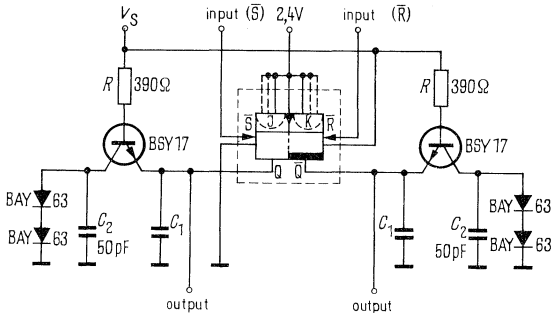


test circuit 29

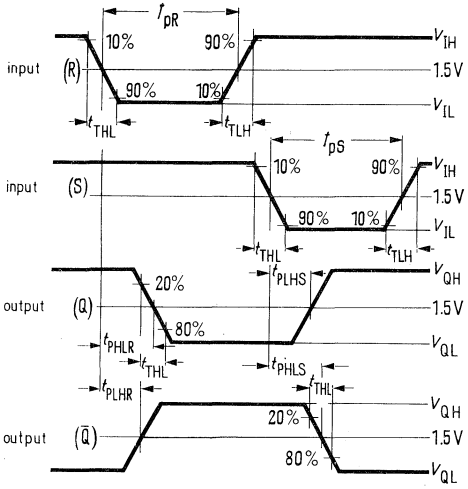


pulse diagram

FL 100



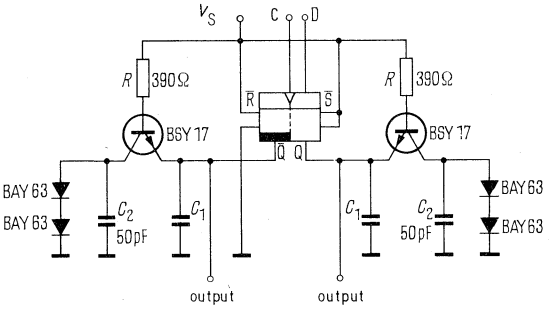
test circuit 30



pulse diagram

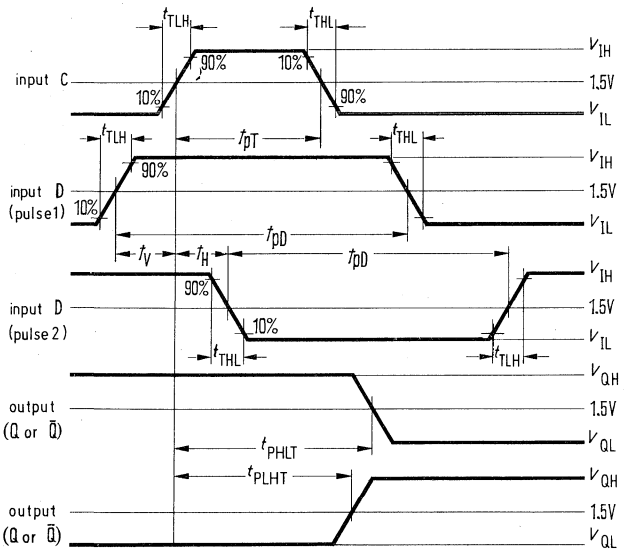
notes for test circuits 29 and 30

1. generator: V_{IL}=0.4 V, V_{IH}=2.4 V, $t_{TLH} \leq 5$ ns, t_{pC}=40 ns, t_{pR}=t_{pS}=25 ns, f=1 MHz. vary f when testing f_C
2. C_1 includes probe and jig capacitance.



test circuit 30

pulse diagram

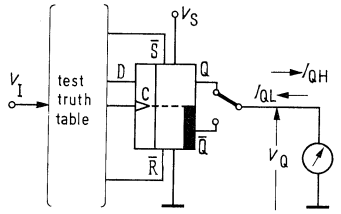


Notes:

1. input pulse: V_{IL}=0.4 V, V_{IH}=2.4 V, t_{TLH}= t_{THL} ≦ 5 ns, t_{pC}= 40 ns, f=1 MHz. Vary f when testing f_C.
2. pulse 1 applies for t_{PLHC} at Q and t_{PHLC} at $\overline{Q}$; pulse 2 applies for t_{PLHC} at $\overline{Q}$ and t_{PHLC} at Q; t_S=20 ns, t_H=5 ns, t_{pD}=60 ns, f=0.5 MHz.
3. C_1 includes probe and jig capacitance.

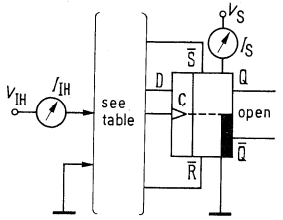
FL 100

Test circuits (flipflops)



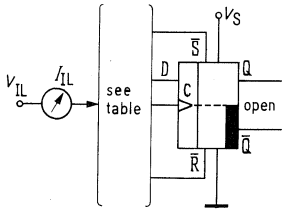
test circuit 31

test truth table
each output is tested separately



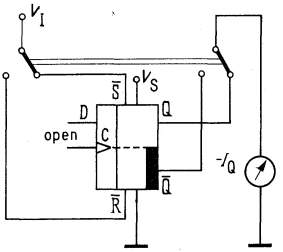
test circuit 32

apply V_{IH} to	4.5 V	ground	ground momentarily, then apply 4.5 V to
D	C	$\overline{R}$	
$\overline{R}$		D, Q, C	
$\overline{S}$	D, $\overline{R}$		C
C		D, C	
I_S		D, C	

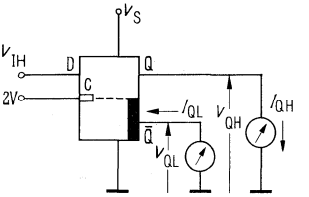


test circuit 33

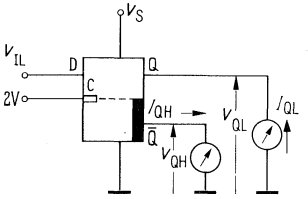
apply in V_{IH} to	4.5 V	ground
D	$\overline{R}$, C	$\overline{S}$
$\overline{S}$	$\overline{R}$, C	D
$\overline{R}$	D, C	
C	$\overline{S}$, $\overline{R}$	D



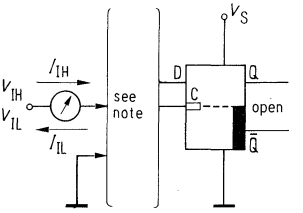
test circuit 34



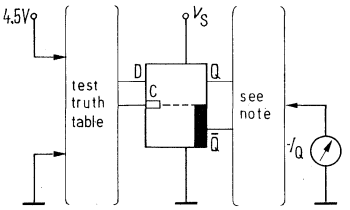
test circuit 36
each output is tested separately



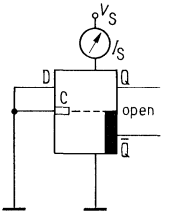
test circuit 37
each output is tested separately



test circuit 38
C must be grounded when testing I_{IH} at D and vice versa.

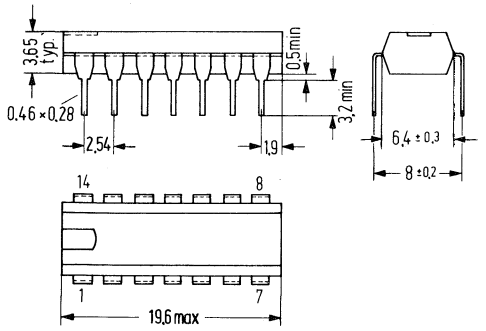


test circuit 39
each flipflop and each output is tested separately

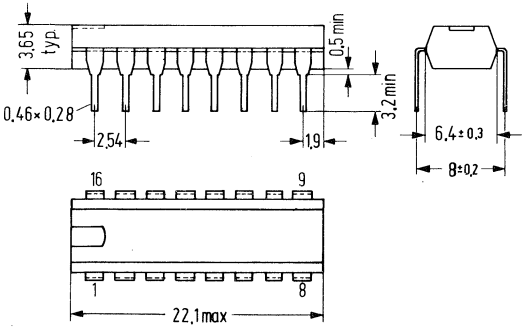


test circuit 40

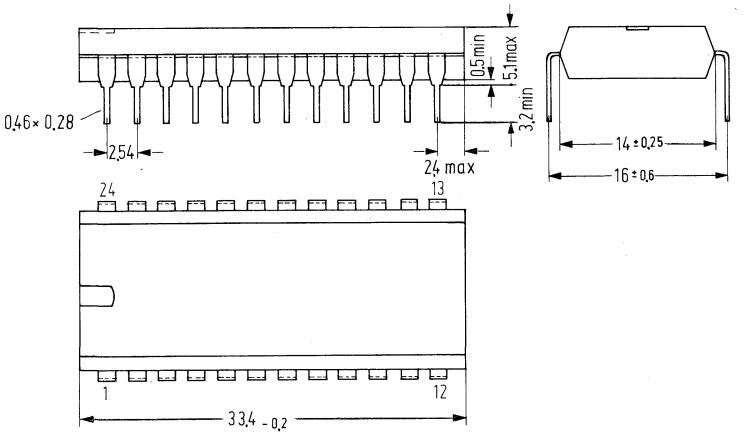
Package outline drawings, dimensions in mm



Plastic dual-in-line package 20A14 DIN 41866
14 pins
weight approx. 1.1 g



Plastic dual-in-line package 20A16 DIN 41866
16 pins
weight approx. 1.2 g



Plastic dual-in-line package 20B24 DIN 41 866
24 pins
weight approx. 3 g

ECL-Series FY 100

2 ECL-Series (Emitter-Coupled-Logic)

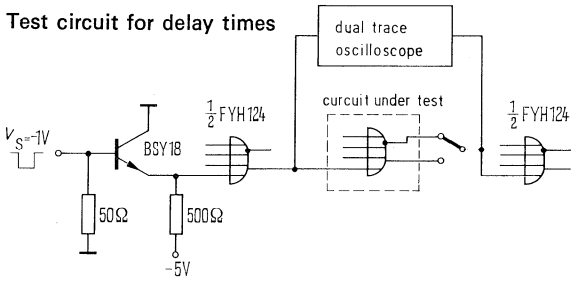
General information about the ECL-series FY 100:

The ECL-series FY 100 comprises three NOR/OR gates. FYH 104, FYH 124 and FYH 134. The ECL-series (emitter-coupled-logic) is a non-satured logic-family intended for the design of digital equipment with very short delay times. The series is encapsulated in a ceramic flat package 21C14 DIN 41865 (TO 87). Qutline drawing below.

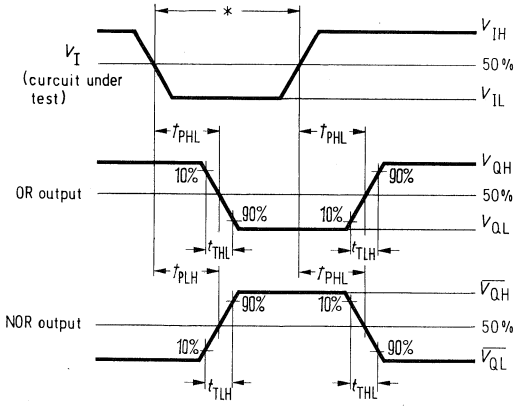
The following maximum ratings apply for all types:

		lower limit B	upper limit A	unit
Supply voltage	V_S	– 7	0	V
Input voltage	V_I	– 5	+2	V
Ambient temperature range	T_A	10	60	°C
Storage temperature range	T_S	–40	150	°C

Test circuit for delay times

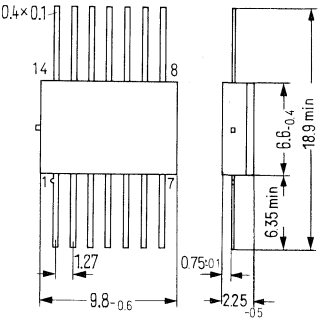


Pulse diagram



*) $t_p \sim 50$ ns, $t_{THL} = t_{TLH} = 5$ ns, $f = 1$ MHz.

ceramic flatpack
21C14 DIN 41865 (TO-87)



weight approx. 0.35 g
dimensions in mm

FYH 104
FYH 124
FYH 134

NOR/OR-Gates

FYH 104: 8-input-NOR/OR-gate
FYH 124: Dual 4-input NOR/OR-gate
FYH 134: Dual 4-input NOR/OR-gate with open emitter output for wired-OR-connections.

Electrical characteristics, $V_S = 5$ V, $T_A = 25$ °C
FYH 104: Connect pin 4 to 5 and 1 to 14
FYH 134: Connect one 500 Ω-resistor each from pins 3 and 4 to 1

		test condition	lower limit B	typ.	upper limit A	unit
H-input voltage	V_{IH}		–1.0			V
L-input voltage	V_{IL}				–1.4	V
H-NOR-output voltage	$\overline{V_{QH}}$	V_{IH}=–1.4 V	–0.85		–0.68	V
L-NOR-output voltage	$\overline{V_{QL}}$	V_{IL}=–1.0 V	–1.75		–1.48	V
H-OR-output voltage	V_{QH}	V_{IL}=–1.0 V	0.82		–0.65	V
L-OR-output voltage	V_{QL}	V_{IH}=–1.4 V	–1.80		–1.53	V
Input current, each input	I_I	V_I=–0.8 V			200	µA
Supply current FYH 104	I_S			25	40	mA
Supply current FYH 124	I_S			45	60	mA
Supply current FYH 134	I_S	pins 1 and 4 open		35	50	mA

Delay times, V_S=5 V, F_Q=F_I=1, T_A=25 °C

NOR-Propagation delay	t_{PLH}				5	ns
	t_{PHL}				5	ns
OR-Propagation delay	t_{PLH}				5	ns
	t_{PHL}				5	ns
Transition time	t_{TLH}				7	ns
Transition time	t_{THL}				5	ns

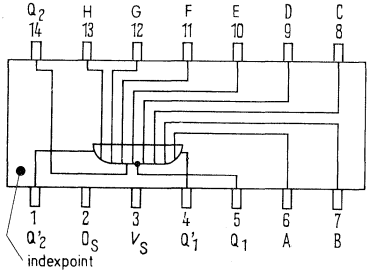
Note:

The lower limit implies a voltage of –V volts or more positive. The upper limit implies a voltage of –V volts or more negative.

FYH 104

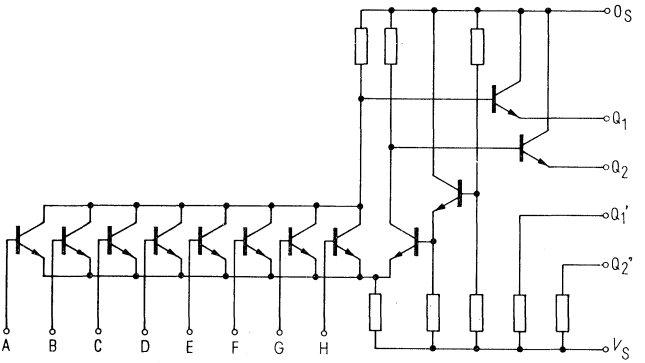
order number
FYH 104: Q67000–H187

8-Input NOR/OR-Gate



Pin configuration
top view

Schematic



Q_1, Q_1 = NOR-output
Q_2, Q_2 = OR-output

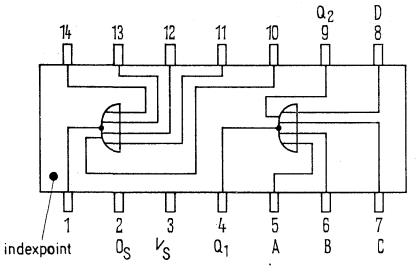
Logical data		upper limit A
Output load factor	F_O	10
Input load factor	F_I	1
Logic	$Q_1 = \bar{Q}_2 = \overline{A + B + C + D + E + F + G + H}$	

Order numbers

FYH 124: Q67000–H188
FYH 134: Q67000–H189

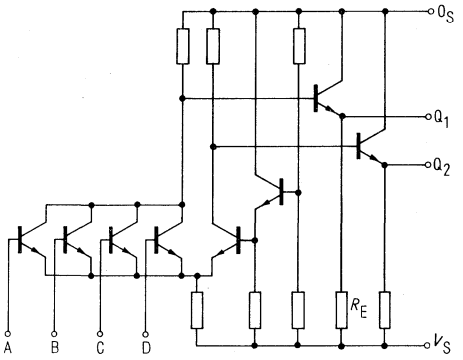
FYH 124
FYH 134

Dual 4-Input NOR/OR-Gates



Pin configuration
top view

Schematic (each gate)



Q_1 = NOR-output
Q_2 = OR-output

Emitter resistors: R_E : FYH 124 only

Logical data		upper limit A
Output load factor	F_O	10
Input load factor	F_I	1
Logic	$Q_1 = \overline{Q}_2 = \overline{A + B + C + D}$	

3 LSL-Series (Low-Speed Noise-Immune Logic)

General Information about the LSL-Series FZ 100

FZ 100 is a low-speed noise-immune logic series of monolithic integrated circuits. A Zener-diode input as well as a relatively large collector capacitance of the input transistor ensure an excellent static and dynamic noise immunity of the integrated circuit. Propagation delay times can be adjusted with capacitors. Thus the dynamic noise immunity can be increased as required. Due to these advantages, the series FZ 100 is in particular suited for applications where strong noise endangers operations, and where the noise immunity is much more important than the switching speed.

1. Description of the Static Characteristics

1.1 Maximum Ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if a single value is exceeded. Maximum ratings are valid at T_A=25 °C unless noted otherwise.

1.2 Electrical Characteristics

Typical characteristics are statistic mean values. In most cases they are supplemented by guaranteed distribution boundaries. Typical characteristics are valid at T_A=25 °C and recommended supply voltages V_S=12 V and 15 V respectively.

1.3 Characteristic Functions

1.3.1 Transfer function

Figure 1 shows the typical transfer function $V_Q=f(V_I)$ of a NAND-gate. The transfer function is almost independent of the output load.
To ensure safe operation, the input voltage must surpass the threshold voltage.The threshold voltage is determined graphically at the intersection of the transfer function with the straight line $V_I=V_Q$.

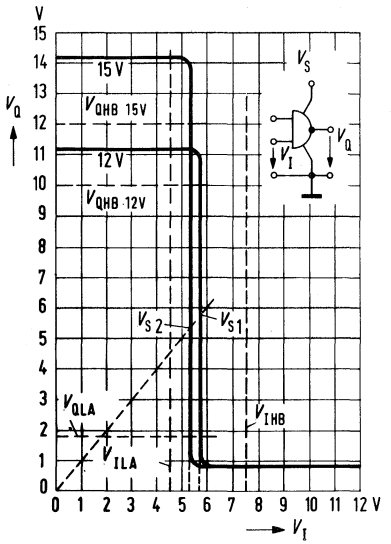


Fig. 1.
Transfer function of a NAND-gate
$V_Q=f(V_I)$ at V_S=12 and 15 V

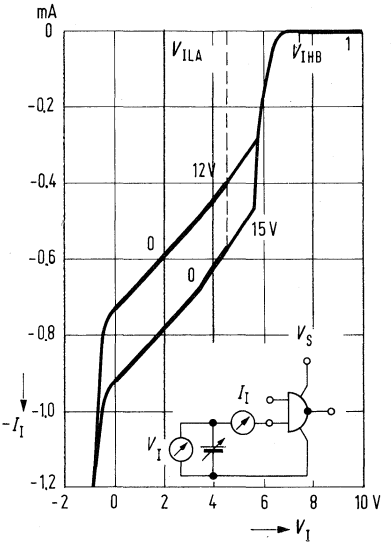


Fig. 2.
Input characteristic of a gate input
$I_I=f(V_I)$ at V_S=12 and 15 V

1.3.2 Input characteristic

Figure 2 shows the typical input characteristic $I_I=f(V_I)$ for supply voltages V_S=12 and 15 V. The input characteristic can be divided into 3 ranges:

1. Only a small reverse current of approximately 1 µA flows into the input if the input is supplied with an H-level. The breakdown voltage of the diodes may not be exceeded.
2. If an L-level is applied to the input, the input current reverses its direction.
3. The substrate diodes start conducting at negative input voltages. The input current increases rapidly. Maximum negative ratings must be observed.

The input characteristic is independent of the load as the gate circuit does not include feedback. The TTL-LSL-level-converter FZH 181 has an input characteristic similar to one given in the TTL-indroduction, figure 2.

1.3.3 Output characteristics

Figure 3 shows the typical output characteristic of the L-state $V_{QL}=f(I_{QL})$. The current I_{QL} is sunk by the gate output. The output characteristic indicates that the output current may exceed the load current of 15 and 18 mA stated in the data sheet for the output voltage V_{QL}=1.7 V. The current limit is given by the total power dissipation per output transistor of 100 mW which must not be exceeded.
Figure 4 shows the typical output characteristic of the H-state $V_{QH}=f(I_{QH})$. Here the output current is supplied by the gate output. Not more than one output may be shortened at the same time.

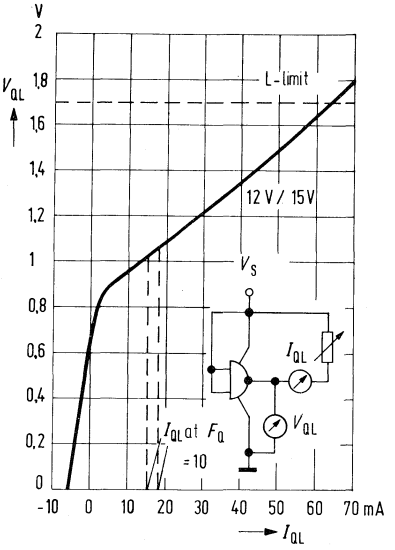


Fig. 3.
Output characteristic of the L-state of a gate output $V_{QL}=f(I_{QL})$ at V_S=12 and 15 V

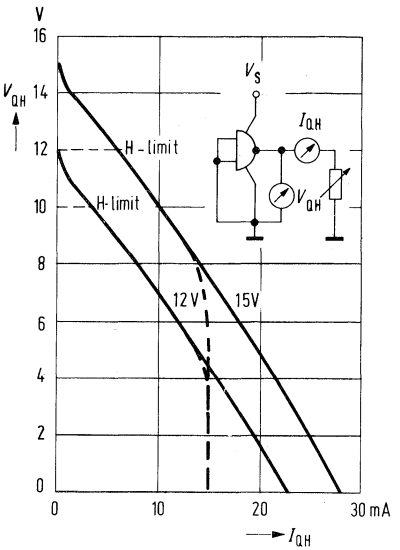


Fig. 4.
Output characteristic of the H-state of a gate output $V_{QH}=f(I_{QH})$ at V_S=12 and 15 V
——— FZH 101 through FZH 171
FZJ 101 and FZJ 111
– – – – FZH 191 through FZH 241
FZJ 121 through FZJ 151

1.4 Static Noise Immunity

The static noise immunity characterizes the behavior of a system disturbed by noise pulses which last longer than the average propagation delay time. The static noise immunity defines the voltage levels which do not influence the logic state. The typical values of the static noise immunity or noise margin are derived from the transfer function (figure 1). For the L-state follows:
at V_S = 12 V: $V_{nmL} = V_{T1} - V_{IL} = 5.9 - 0.9 = 5.0$ V
at V_S = 15 V: $V_{nmL} = V_{T2} - V_{IL} = 5.6 - 0.9 = 4.7$ V.

For the H-state follows:
at V_S = 12 V: $V_{nmH} = V_{QH} - V_{T1} = 11.3 - 5.9 = 5.4$ V
at V_S = 15 V: $V_{nmH} = V_{QH} - V_{T2} = 14.3 - 5.6 = 8.7$ V.

The guaranteed noise immunity under worst-case conditions results as follows:
$V_{nmL} = V_{IL} - V_{QL} = 4.5 - 1.7 = 2.8$ V at V_S = 12 and 15 V
$V_{nmH} = V_{QH} - V_{IH} = 10 - 7.5 = 2.5$ V at V_S = 12 V and
$V_{nmH} = V_{QH} - V_{IH} = 12 - 7.5 = 4.5$ V at V_S = 15 V.

1.5 Logical data

1.5.1 Input load factor

The input load factor defines the currents required by a single input at H-state as well as L-state. The upper limit of the H-input current per input is 1 µA. The upper limit of the L-input current per input is 1.5 mA at V_S = 12 V and 1.8 mA at V_S = 15 V. These values define the normalized load factor F_I = 1. They are valid within the entire temperature range.
F_I = 2 means for example an L-input current of $-I_{IL} = 2 \times 1.5 = 3$ mA at V_S = 12 V and $-I_{IL} = 2 \times 1.8 = 3.6$ mA at V_S = 15 V and an H-input current of $I_{IH} = 2 \times 1 = 2$ µA.

1.5.2. Output load factor

The output load factor defines how many normalized loads F_I=1 can be driven by a single output. The values of the output load factors are stated below:

	L-state	H-state
gates except FZH 151 and open collector circuits	F_{QL} = 10	F_{QH} = 100
FZH 151	F_{QL} = 16	F_{QH} = 100
powergate	F_{QL} = 30	F_{QH} = 100
flipflops and counters	F_{QL} = 10	F_{QH} = 100
level-converters and open collector circuits	F_{QL} = 10	F_{QH} = 20

The H-output load factor is higher than the L-output load factor. In this way it is possible to connect unused inputs of the same gate in parallel without accounting for an additional load.

2. Description of the Dynamic Characteristics

2.1 General

Due to a special geometry of the input transistor the collector capacitance is relatively great. This causes long propagation delay times and a high dynamic noise immunity results. Circuits with an N-node enable the designer to lengthen the propagation delay times with an integrating capacitor. Thus the dynamic noise immunity can be adapted as required. The capacitor is connected between output Q and N-node with gates. The flipflops FZJ 101 and FZJ 105 require two capaciters. One between output Q and node N_Q and another one between output Q and node $N_{\bar{Q}}$. Two additional capacitors may be provided at the nodes N_J, N_J and N_K, N_K of the flipflops FZJ 111 and FZJ 115 to increase the noise immunity of the master. No limit is given for the integrating capacitor. Figure 5 shows the switching parameters as a function of the integrating capacitance C.

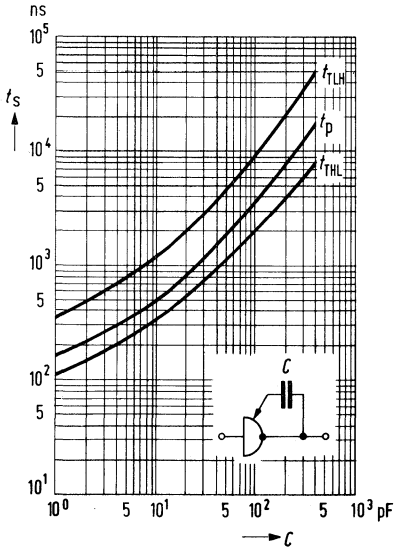


Fig. 5.
Switching parameters t_S as a function of the integrating capacitance C at V_S=12 V

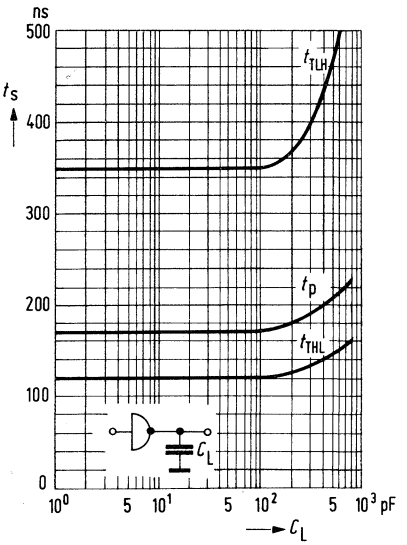


Fig. 6.
Switching parameters t_S as a function of the load capacitance C_L at V_S=12 V

t_{TLH}, t_{THL} transition times
t_P average propagation delay time given by:

$$t_P = \frac{t_{PHL} - t_{PLH}}{2}$$

2.2 Propagation Delay and Transition Time

The propagation delay time t_{PLH} is measured between input and output while the output rises from L to H-level. Whereas t_{PHL} is determined when the output switches from H to L. Reference points for the propagation delay time are the levels 4.5 V.
The transition times t_{THL} and t_{TLH} of the output pulse are measured between the 10% and 90% values.
The pair-delay defines the signal delay which is caused by two NAND-gates connected in series. The output signal is then in phase with the input signal, however delayed by:
$t_{PD} = t_{PHL} - t_{PLH}$
Figure 6 shows that the switching parameters are nearly independent of the load capacitance. This is due to a low output resistance at the L-state as well as the H-state. In this way it is possible to use long connection lines which represent essentially a capacitive load. The switching parameters remain constant over a wide range.
Figures 7 through 11 show the signal propagation delay time as well as the transition time as a function of the supply voltage V_S over the entire operating range of 11.4 to 17 V.

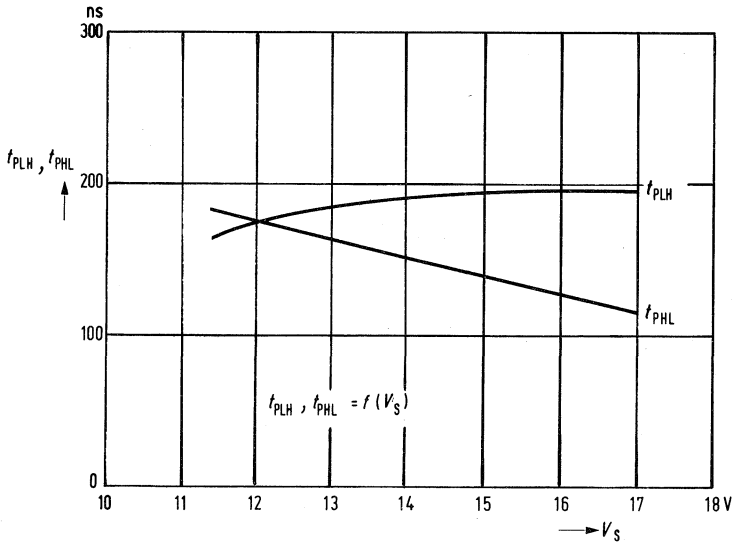


Fig. 7
Propagation delay time of a typical NAND-gate
$t_{PLH} = f(V_S)$
$t_{PHL} = f(V_S)$

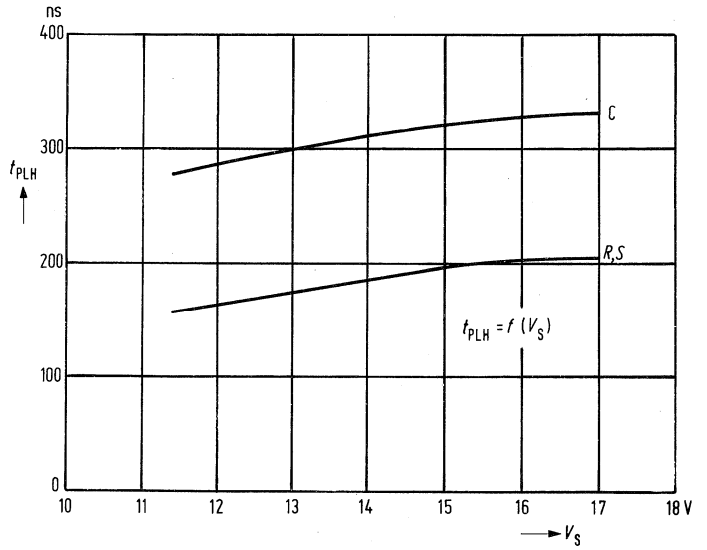


Fig. 8
Propagation delay time of a typical flipflop
$t_{PLH} = f(V_S)$
C = clock input
R, S = reset and set inputs

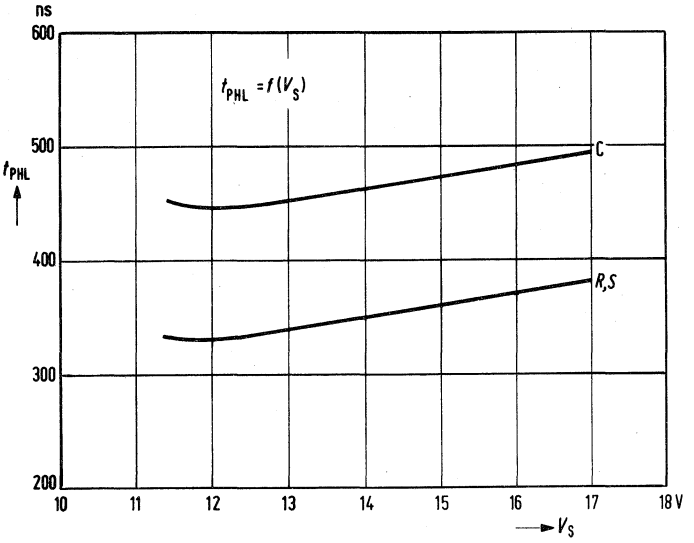


Fig. 9
Propagation delay time of a typical flipflop
$t_{PHL} = f(V_S)$
C = clock input
R, S = reset and set inputs

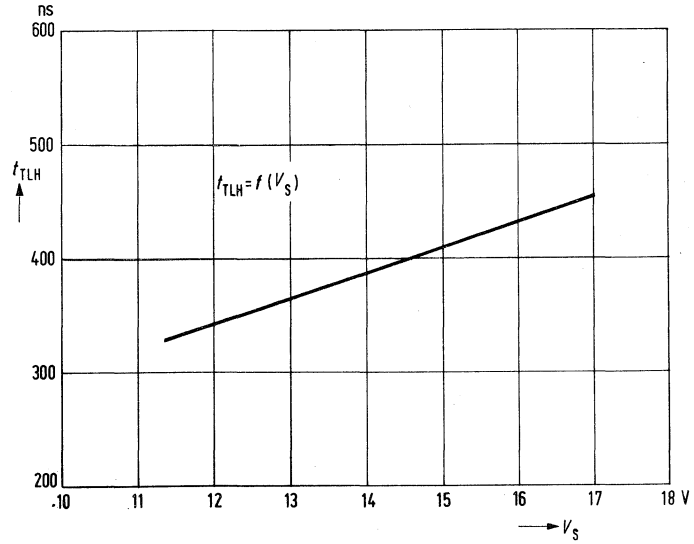


Fig. 10
Transition time of typical NAND-gates and flipflops
$t_{TLH} = f(V_S)$

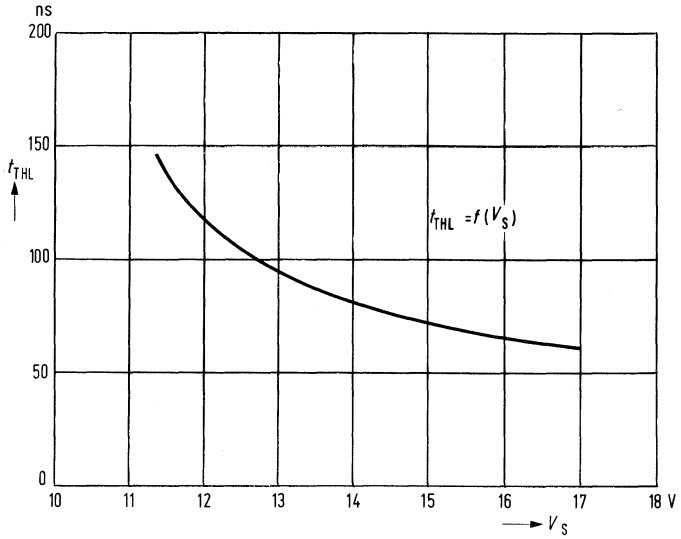


Fig. 11. Transition time of typical NAND-gates and flipflops $t_{THL} = f(V_S)$

2.3 Dynamic Noise Immunity

The dynamic noise immunity characterizes the behavior of a system disturbed by noise pulses of a shorter duration than the signal propagation delay time. In this case the energy of the noise pulse — pulse amplitude and duration — determines whether a change of the logic state will take place.
The practical aspects of the dynamic noise immunity are the input noise immunity and the immunity against capacitively coupled noise. The source of capacitively coupled noise can either be cross talk (system noise) or foreign noise. A couple cpacitance of up to 1.6 nF typically does not yet introduce any cross talk. Due to this value, system noise can in general be regarded as being a minor problem, and foreign noise sources only have to be considered as important.

2.3.1 Input noise immunity

Pulse duration and amplitude of a noise pulse are limited by the propagation delay time t_P of a gate. The noise amplitude may become greater than the static noise immunity if the noise pulse duration $b \leqq {}^1/_2 t_P$. The noise amplitude may not exceed the static noise immunity if $b \geqq t_P$. However, t_P can be adjusted as required by an integrating capacitance C.
Figures 12 and 13 show the input noise immunity of NAND-gates with and without integrating capacitance as well as the AND/OR-gate FZH 151. The noise voltage V_{nm} is shown as a function of the noise pulse duration b. Figure 12 indicates the more critical case where an L-signal at the input is disturbed. This is due to the transition time t_{THL} being shorter than t_{TLH}. Thus the noise pulse duration at L-level is less than at H-level (figure 13).

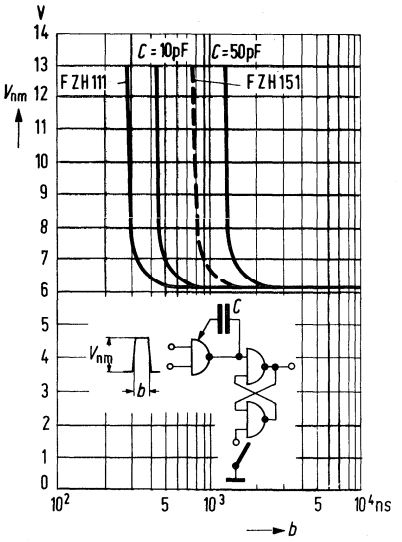


Fig. 12.
Typical boundary characteristic of the dynamic noise immunity of the L-level at the input

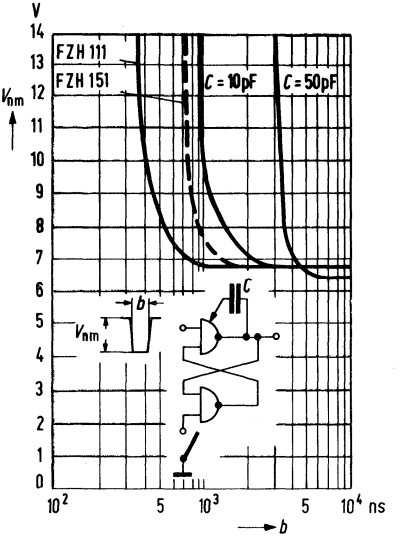


Fig. 13.
Typical boundary characteristic of the dynamic noise immunity of the H-level at the input

2.3.2 Capacitively coupled noise

The push-pull output stage generally used with LSL-circuits has a low output resistance in both logic states ($R_{QL} \sim 20\,\Omega$ and $R_{QH} \sim 400\,\Omega$). The resulting time constants are relatively small, and noise pulses die away rapidly. Figures 14 and 15 show the noise immunity against capacitively coupled noise of NAND-gates with and without integrating capacitance and the AND/OR-gate FZH 151. The noise voltage V_{nm} is shown as a function of the coupling capacitance C_S. The more critical case is given in Figure 15 where an H-state is disturbed. This is due to the H-output resistance being greater than the L-output resistance.
The transition time of the noise source was approximately 1 ns and the source resistance approximately 1 Ω.

The almost vertical part of the boundary curve of figures 12 through 15 indicates the dynamic noise immunity. Noise below this boundary has no influence on the logic state of the circuit. The boundary curves end at the value of the static noise immunity. Noise indicator is a RS-flipflop consisting of two NAND-gates.

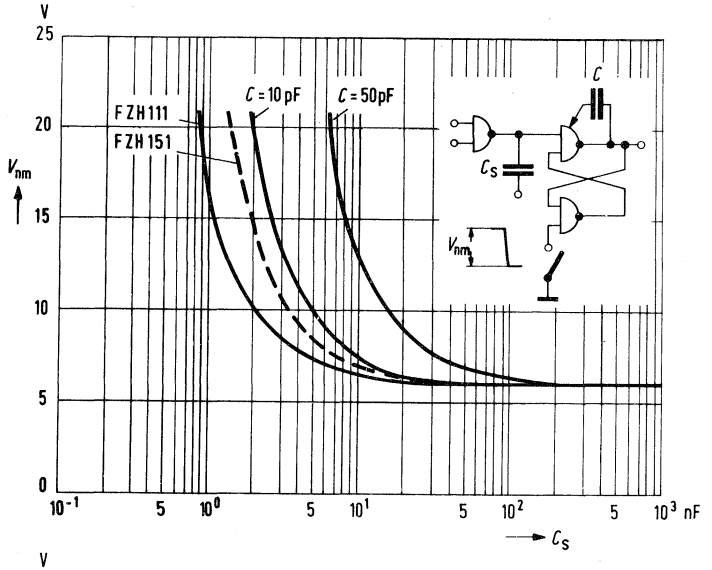


Fig. 14
Typical boundary characteristic of the dynamic noise immunity against capacitively coupled noise during L-state

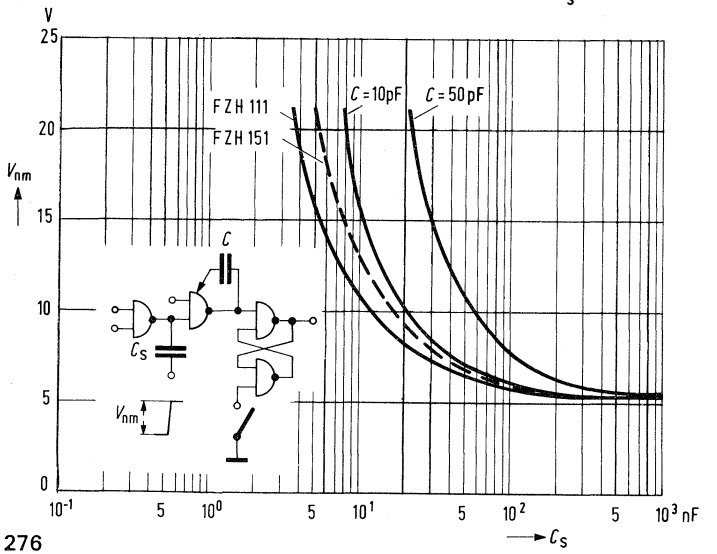


Fig. 15
Typical boundary characteristic of the dynamic noise immunity against capacitively coupled noise during H-state

General Information on the LSL-Series FZ 100

The electrical characteristics are given for two supply voltage ranges. The limits of the 12 V-range are V_{SB} = 11.4 V and V_{SA} = 13.5 V. The limits of the 15 V-range are V_{SB} = 13.5 V and V_{SA} = 17.0 V. Typical values are valid at the corresponding nominal voltages and an ambient temperature T_A = 25 °C.

Maximum Ratings

		lower limit B	upper limit A	unit
Supply voltage except FZH 181/185	V_S	0	18	V
Supply voltage FZH 181/185	V_S	0	7	V
Input voltage except FZH 181/185	V_I	0	18	V
Input voltage FZH 181/185	V_I	0	5.5	V
Voltage at the node N	V_N	–1	0.6	V
Current at the node N	I_N	–10	2	mA
Ambient temperature range 1	T_A	0	70	°C
range 5	T_A	–25	85	°C
Storage temperature	T_S	–65	150	°C

Maximum Negative Ratings at T_A=0 to 70 °C

	V_I V	I_I mA	at V_S V
Any input except N-nodes of FZH 101, 111, 121, 131, 141, 161, 171 FZJ 101, 111 note for FZH 171: no negative voltages at the expander input N_1		–25	17
FZH 151	–0.7		17
FZH 181	–0.5	–25	5

Pins shown unconnected in the pin configuration must be left open.
LSL-Series FZ 100 is available in plastic dual-in-line packages with 14 and 16 pins. (outline drawings at the end of chapter).
The LSL-Series will be expanded progressively.

FZH 101 FZH 121 FZH 171
FZH 105 FZH 125 FZH 175
FZH 111 FZH 131
FZH 115 FZH 135

FZH 101/105 Quadruple 2-Input NAND-Gate
FZH 111/115 Quadruple 2-Input NAND-Gate with N-Input
FZH 121/125 Dual 5-Input NAND-Gate
FZH 131/135 Dual 5-Input NAND-Gate with N-Input
FZH 171/175 Dual 4-Input NAND-Gate with Expander Nodes N_1 and N-Input

Electrical Characteristics

12 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SA}$ and V_{SB}	2			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} V_{IL}=4.5 V, $-I_{QH}$=0.1 mA	2	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ V_{IH}=7.5 V, I_{QL}=15 mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	4		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ V_I=0 V, T_A=25 °C	5	10.0	30.0	50.0	mA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ V_I=0 V	6		0.9	1.6	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		1.7	3.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			16	31	mW

Delay times, V_S=12 V, F_Q=1, T_A=25 °C

Propagation delay	t_{PLH}	C_L=10 pF	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}			200	340	570	ns
	t_{THL}			70	120	210	ns

Electrical characteristics

15 V-range temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	2	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=18$ mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.6	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=0$ V, $T_A=25$ °C	5	15.0	37.0	60.0	mA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	6		2.1	2.1	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		2.3	4.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			27	52	mW

Delay times, $V_S=15$ V, $F_Q=1$, $T_A=25$ °C

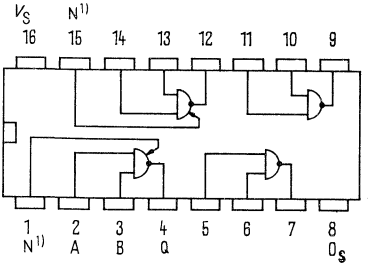
Propagation delay	t_{PLH}	$C_L=10$ pF	26		195		ns
	t_{PHL}				140		ns
Transition time	t_{TLH}				410		ns
	t_{THL}				75		ns

FZH 101
FZH 105
FZH 111
FZH 115

order numbers

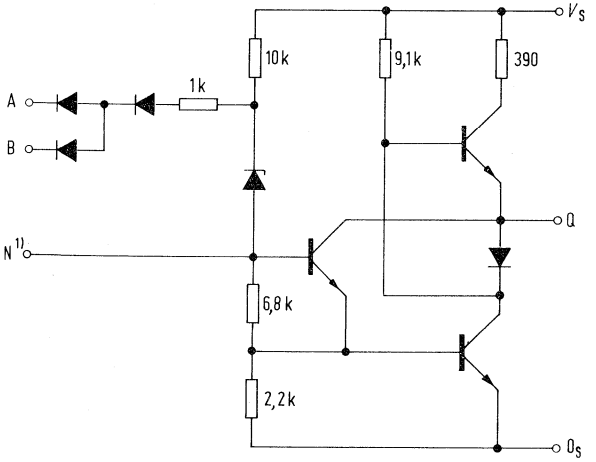
FZH 101:	Q67000–H190
FZH 105:	Q67000–H250
FZH 111:	Q67000–H191
FZH 115:	Q67000–H215

Quadruple 2-Input NAND-Gate



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor, H-signal	F_{QH}	100
L-signal	F_{QL}	10
Input load factor, each input	F_I	1

Logic Q = $\overline{AB}$

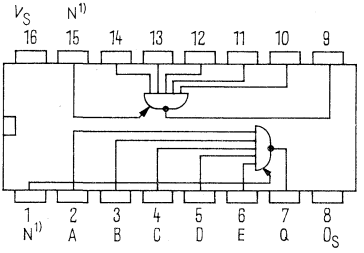
[1]) FZH 111/115 only

order numbers

FZH 121: Q67000–H192
FZH 125: Q67000–H254
FZH 131: Q67000–H193
FZH 135: Q67000–H255

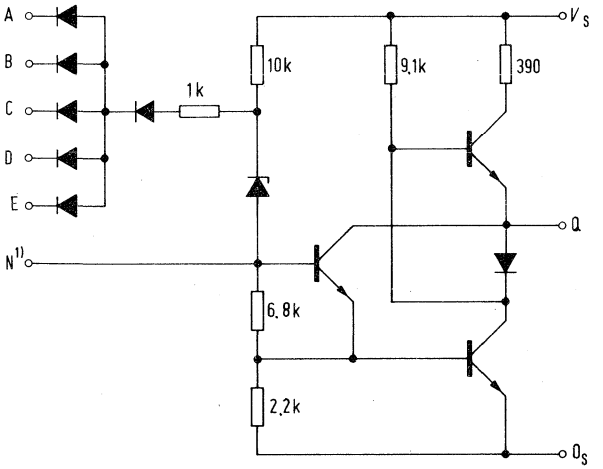
FZH 121
FZH 125
FZH 131
FZH 135

Dual 5-Input NAND-Gate



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor, H-signal	F_{QH}	100
L-signal	F_{QL}	10
Input load factor, each input	F_I	1

Logic Q = $\overline{ABCDE}$

[1]) FZH 131/135 only

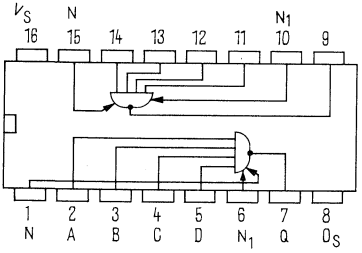
FZH 171
FZH 175

order numbers

FZH 171: Q67000–H328
FZH 175: Q67000–H329

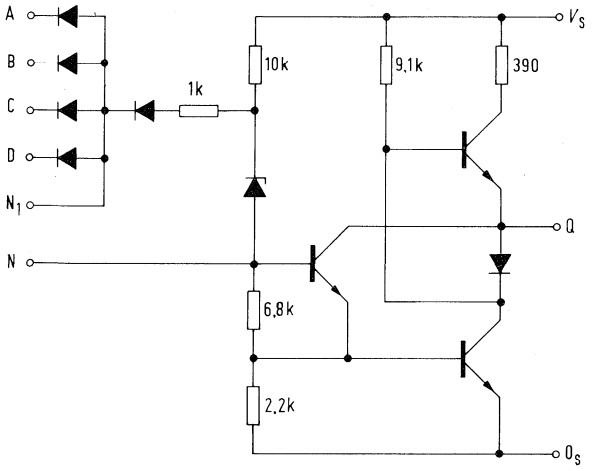
Dual 4-Input NAND-Gate with Expander Nodes N_1 and N-Input

The number of inputs can be expanded as required by means of additional input diodes BAW 76 at the expander input N_1. The anodes of the diodes must be connected in parallel to N_1.



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor, H-signal	F_{QH}	100
L-signal	F_{QL}	10
Input load factor, each input	F_I	1

Logic $Q = \overline{ABCD\ Exp.}$

order numbers

FZH 141: Q67000–H194
FZH 145: Q67000–H256

FZH 141
FZH 145

Dual 5-Input NAND-Powergate with N-Input

The electrical characteristics of the FZH 141/145 are similar to the FZH 131/135 except for the values stated below.

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=45$ mA	1		1.3	1.7	V

Electrical characteristics

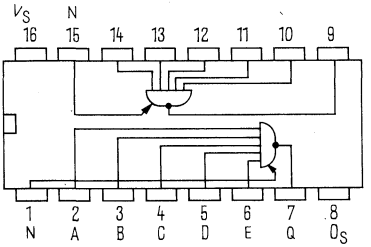
15 V-range
temperature ranges 1 and 5

L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=54$ mA	1		1.4	1.7	V

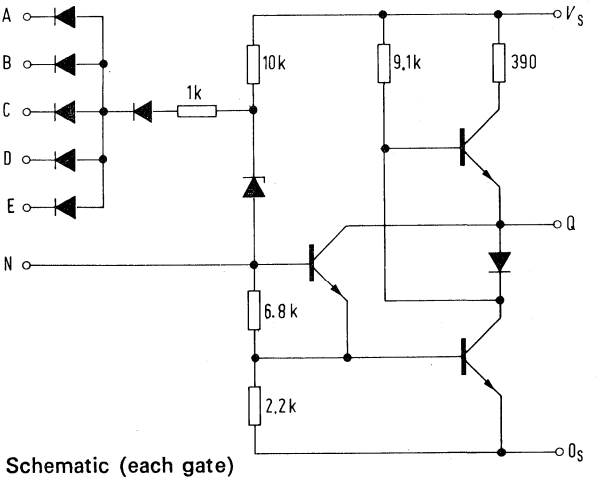
Logical data, each gate

Output load factor, H-signal	F_{QH}		100
L-signal	F_{QL}		30
Input load factor, each input	F_I		1

Logic $Q = \overline{ABCCE}$



Pin configuration
top view



Schematic (each gate)

FZH 151
FZH 155

order numbers
FZH 151: Q67000–H195
FZH 155: Q67000–H260

Dual-AND-OR-Gate with N-Input

The FZH 151/155 are suited for the following applications:
AND/OR-gate, counter, divider, and shiftregister flipflop, adder, delay element. The lower limit of the supply voltage is V_S=10 V.

Electrical characteristics

12 V-range Temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	15	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	16			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ V_{IL}=4.5 V, $-I_{QH}$=0.1 mA	16	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ V_{IH}=7.5 V, I_{QL}=30 mA	15		0.9	1.7	V
DC noise margin							
H-signal	V_{SS}			2.5	5.0		V
L-signal	V_{SS}			2.8	5.0		V
H-input current at R_1, C_1, R_2, C_2	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			2.0	µA
H-input current remaining inputs	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			1.0	µA
L-input current at R_1, C_1, R_2, C_2	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	18		1.0	2.5	mA
L-input current remaining inputs	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	18		0.5	1.25	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ V_I=0 V, T_A=25 °C	19	10.0	30.0	50.0	mA
H-supply current	I_{SH}	$V_S=V_{SA}$ V_I=0 V	20		14.0	22.0	mA
L-supply current	I_{SL}	$V_S=V_{SA}$ $V_I=V_{SA}$	21		8.0	15.0	mA
Power consumption	P	$V_S=V_{SA}$ duty cycle 1 : 1			132	250	mW

Delay times, V_S=12 V, F_Q=1, T_A=25 °C

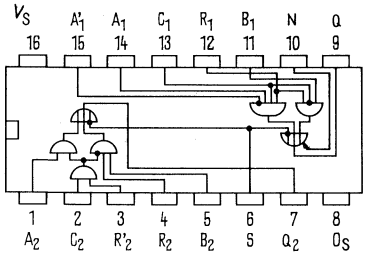
Propagation delay	t_{PLHI}	output signal non-inverted			340		ns
	t_{PLHII}	output signal inverted			340		ns
	t_{PLHIII}	input pin 15			270		ns
Propagation delay	t_{PHLI}	output signal non-inverted			230		ns
	t_{PHLII}	output signal inverted			300		ns
	t_{PHLIII}	input pin 15			400		ns
Transition time	t_{TLH}	C_L=10 pF			330		ns
	t_{THL}	C_L=10 pF			200		ns

Electrical characteristics

15 V-range
temperature range 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	15	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	16			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	16	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=30$ mA	15		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current at R_1, C_1, R_2, C_2	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			2.0	µA
H-input current remaining inputs	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	17			1.0	µA
L-input current at R_1, C_1, R_2, C_2	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	18		1.2	3.0	mA
L-input current remaining inputs	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	18		0.6	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=0$ V, $T_A=25$ °C	19	15.0	37.0	60.0	mA
H-supply current	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	20		18.0	29.0	mA
L-supply current	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	21		12.0	21.0	mA
Power consumption	P	$V_S=V_{SA}$ duty cycle 1:1			225	125	mW

FZH 151
FZH 155



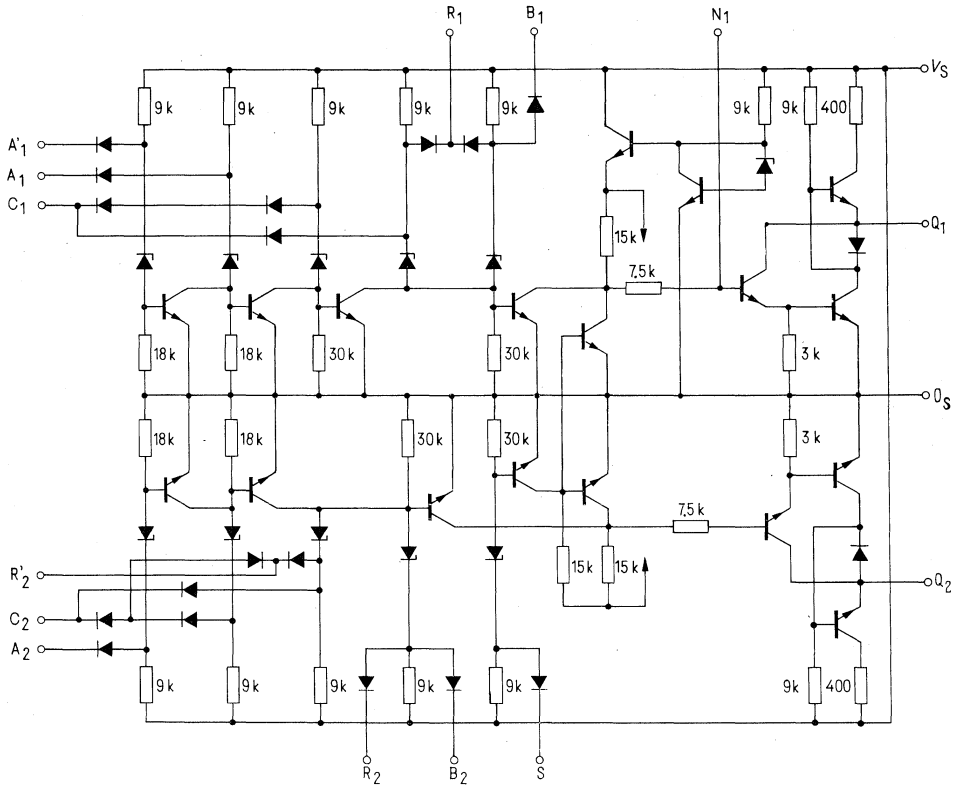
Pin configuration
top view

Logical data, each gate		upper limit A
Output load factor		
H-signal	F_{QH}	100
L-signal (LSL load)	F_{QL}	16
L-signal (FZH 151 as load)	F_{QL}	20
Input load factor at R_1, C_1, R_2, C_2	F_I	2
Input load factor, remaining inputs	F_I	1

Logic $Q_1 = \bar{S} + (A_1 A'_1 R_1 C_1) + (B_1 R_1 \bar{C}_1)$

$Q_2 = \bar{S} + (A_2 C_2 R'_2) + (B_2 R_2 \overline{C_2 R'_2})$

Schematic


R1
B1
N1
VS
A'1
A1
C1
9k
400
15k
7,5k
18k
30k
3k
Q1
QS
Q2
R'2
C2
A2
R2
B2
S

FZH 161
FZH 165

order numbers

FZH 161: Q67000–H288
FZH 165: Q67000–H289

Quadruple LSL-TTL-Level-Converter

The FZH 161/165 may also be used as LSL-wired-AND stages. The collector load resistance is calculated according to the formulaes stated on the following pages. The upper limit of the breakdown voltage at the Q-outputs is 18 V.

Electrical characteristics

15 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	9	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	10			4.5	V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $V_{IH}=7.5$ V, $I_{QL}=20$ mA	9			0.4	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current							
at input pins 2, 5, 11, 14	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	11			1.0	µA
at input pins 1, 15	I_{IH}					2.0	µA
L-input current							
at input pins 2, 5, 11, 14	$-I_{IL}$	$V_S=V_{SA}$, $V_I=1.7$ V	12		0.8	1.5	mA
at input pins 1, 15	$-I_{IL}$				1.6	3.0	mA
H-output current, each output	I_{QH}	$V_S=V_{SA}$, $V_Q=18$ V	10			80	µA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$, $V_I=0$ V	14		2.5	4.5	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$, $V_I=V_{IHA}$	13		4.0	6.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1 : 1			39	70	mW

Delay times, $V_S=12$ V, $F_Q=1$, $T_A=25$ °C

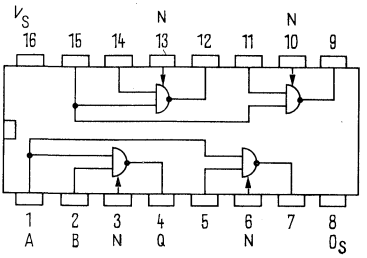
Propagation delay	t_{PLH}	$V_{SC}=12$ V	28		250	500	ns
	t_{PLH}	$V_{SC}=5$ V			230	500	ns
	t_{PHL}	$V_{SC}=12$ V			130	300	ns
	t_{PHL}	$V_{SC}=5$ V			120	300	ns

Electrical characteristics

15 V-range
temperature range 1 and 5

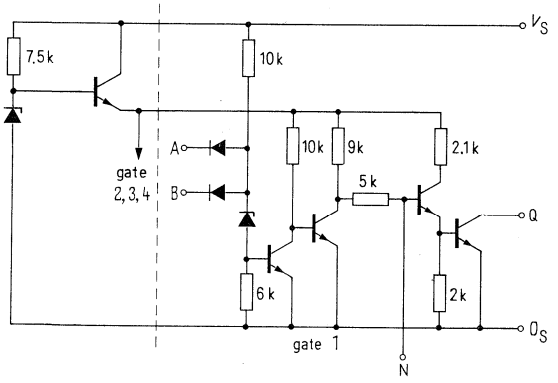
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	9	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$	10			4.5	V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $V_{IH}=7.5$ V, $I_{QL}=20$ mA	9			0.4	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current							
at input pins 2, 5, 11, 14	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	11			1.0	µA
at input pins 1, 15	I_{IH}					2.0	µA
L-input current							
at input pins 2, 5, 11, 14	$-I_{IL}$	$V_S=V_{SA}$, $V_I=1.7$ V	12		1.0	1.8	mA
at input 1, 15	$-I_{IL}$				2.0	3.6	mA
H-output current, each output	I_{QH}	$V_S=V_{SA}$, $V_Q=18$ V	10			80	µA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$, $V_I=0$ V	14		2.8	4.5	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$, $V_I=V_{IHA}$	13		4.5	7.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1 : 1			55	78	mW

FZH 161
FZH 165



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor	F_Q	10
Input load factor, input A	F_I	2
Input load factor, input B	F_I	1
Logic	$Q = \overline{AB}$	

Calculation of the Collector Load Resistance R_C

The collector load resistance is derived from the required output voltage and the input and output currents of the gates as follows:

$$R_{CA} = \frac{V_{SC} - V_{OH}}{nI_{QH} + NI_{IH}} \frac{V}{\mu A} \qquad R_{CB} = \frac{V_{SC} - V_{OL}}{I_{QLA} - NI_{IL}} \frac{V}{\mu A}$$

where: V_{SC} = supply voltage of the load resistor
n = number of AND-connections
N = number of inputs connected.

The actual resistance used in the circuit must have a value between the limits A and B.

Applications as level-converters:

FZH 161/165, LSL-TTL: $R_{CA} = \frac{5 - 2.4}{n\,80 + N\,40} \frac{V}{\mu A}$ $R_{CB} = \frac{5 - 0.4}{20 - N\,1.6} \frac{V}{mA}$

where: $n_A = 2$ for $N_A = 10$

FZH 181/185, TTL-LSL_{12V}: $R_{CA} = \frac{12 - 10}{n\,250 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{12 - 1.0}{50 - N\,1.5} \frac{V}{mA}$

TTL-LSL_{15V}: $R_{CA} = \frac{15 - 12}{n\,250 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{15 - 1.0}{50 - N\,1.8} \frac{V}{mA}$

where: $n_A = 4$ for $N_A = 25$

Applications with wired-AND-connections of the FZH 161/165:

12 V-range: $R_{CA} = \frac{12 - 10}{n\,80 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{12 - 0.4}{20 - N\,1.5} \frac{V}{mA}$

15 V-range: $R_{CA} = \frac{15 - 12}{n\,80 + N\,1} \frac{V}{\mu A}$ $R_{CB} = \frac{12 - 0.4}{20 - N\,1.8} \frac{V}{mA}$

where: $n_A = 9$ for $N_A = 10$.

Applications with TTL-wired-AND-connections of the FZH 181/185: see formulae and resistance table of FLH 201.

FZH 181
FZH 185

order numbers

FZH 181: Q67000–H326
FZH 185: Q67000–H327

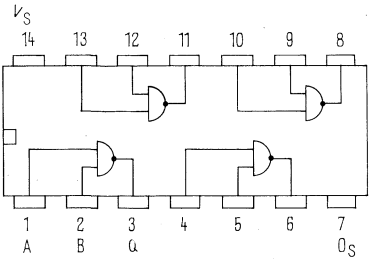
Quadruple TTL-LSL-Level-Converter

The FZH 181/185 may also be used as LSL-wired-AND stages. The collector load resistance is calculated according to the formulaes stated on the preceding page. The upper limit of the breakdown voltage at the Q-outputs is 18 V.

Electrical characteristics temperature ranges 1 and 5		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			4.75	5.0	5.25	V
H-input voltage	V_{IH}	V_S=4.75 V	1	2.0			V
L-input voltage	V_{IL}	V_S=4.75 V	8			0.8	V
L-output voltage	V_{QL}	V_S=4.75 V V_{IH}=2.0 V, I_{QL}=16 mA	1			0.4	V
	V_{QL}	V_S=4.75 V V_{IH}=2.0 V, I_{QL}=50 mA	1			1.0	V
DC noise margin	V_{nm}			0.4	1.0		V
L-input current, each input	$-I_{IL}$	V_S=5.25 V V_{IL}=0.4 V	4			1.6	mA
H-input current, each input	I_{IH}	V_S=5.25 V V_{IH}=2.4 V	3			80	µA
	I_I	V_S=5.25 V V_I=5.5 V	3			1.0	mA
H-output current, each output	I_{QH}	V_S=4.75 V V_{IL}=0.8 V, V_{QH}=18 V	8			250	µA
H-supply current, each gate	I_{SH}	V_S=5 V, V_I=0 V	6		1.0	2.0	mA
L-supply current, each gate	I_{SL}	V_S=5 V, V_I=5 V	7		8.5	12	mA
Power consumption, each gate	P	V_S=V_{SA} duty cycle 1 : 1			24	37	mW

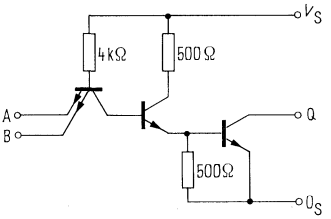
Delay times, V_S=12 V, F_Q=1, T_A=25 °C

Propagation delay	t_{PLH}	V_{SC}=12 V	} 29		130	300	ns
	t_{PHL}	V_{SC}=12 V			20	60	ns



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor	F_Q	10
Input load factor, each input	F_I	1
Logic	$Q = \overline{AB}$	

FZH 191
FZH 195
FZH 201
FZH 205

order numbers

FZH 191:	Q67000–H633
FZH 195:	Q67000–H634
FZH 201:	Q67000–H636
FZH 205:	Q67000–H637

Tentative data

FZH 191/195 Triple 3-Input NAND-Gate with N-Input
FZH 201/205 Hex Inverter with Strobe Inputs

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage				11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA}		10.0	11.3		V
		$V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	2				
Output voltage	V_{QL}	$V_S=V_{SB}$	1		0.9	1.7	V
		$V_{IH}=7.5$V, $I_{QL}=15$mA					
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_Q=0$ V	5	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	6		0.9	1.6	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		1.7	3.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1 : 1			15	31	mW

Delay times, $V_S=12$ V, $F_Q=1$, $T_A=25$ °C

Propagation delay	t_{PHL}	$C_L=10$ pF	26	90	175	310	ns
	t_{PHL}			90	175	310	ns
Transition time	t_{TLH}			200	340	570	ns
	t_{THL}			70	120	210	ns

Electrical characteristics

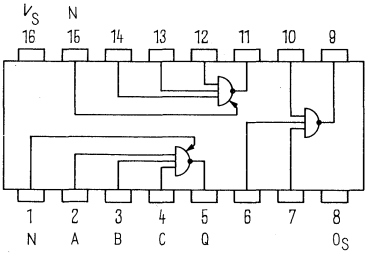
15 V-range temperature range 1		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	2			4.5	V
H-output voltage	V_{IH}	$V_S=V_{SB}$ and V_{SA} V_{IL}=4.5 V, $-I_{QH}$=0.1 mA	2	12.0	14.3		V
L-output voltage	V_{IL}	$V_S=V_{SB}$ V_{IH}=7.5 V, I_{QL}=18 mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current each input	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	4		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ V_Q=0 V	5	9	15	25	mA
H-Supply current, each gate	I_{SH}	$V_S=V_{SA}$ V_I=0 V	6		1.2	2.1	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		2.3	4.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1 : 1			27	46	mW

Delay times, V_S=15 V, F_Q=1, T_A=25 °C

Propagation delay	t_{PLH}	C_L=10 pF	26		410		ns
	t_{PHL}				75		ns
Propagation delay	t_{TLH}				195		ns
	t_{THL}				140		

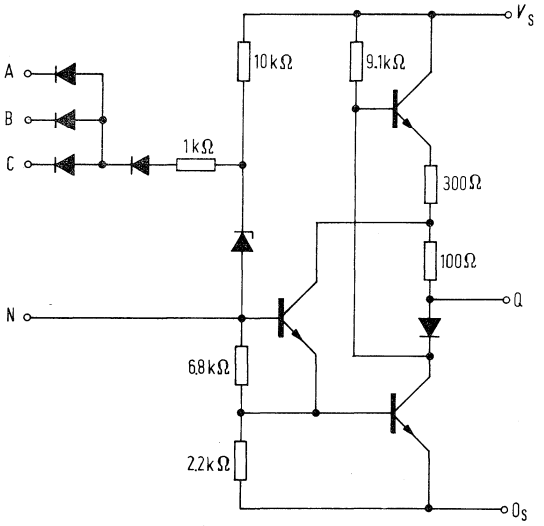
FZH 191
FZH 195

Triple 3-Input NAND-Gate with N-Input



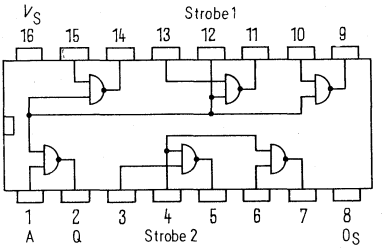
Pin configuration
top view

Schematic (each gate)



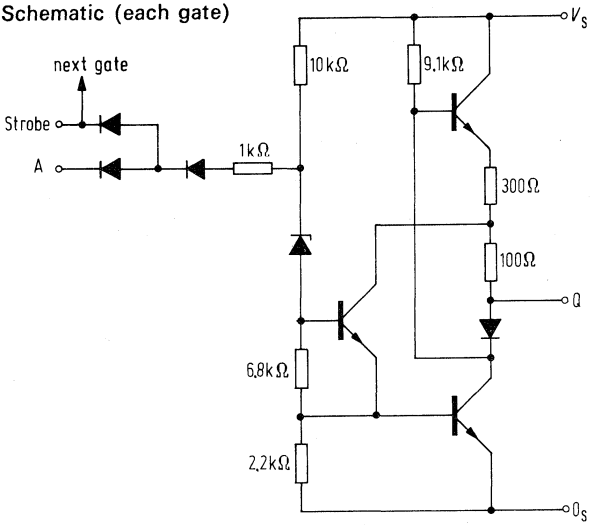
Logical data, each gate		upper limit A
Output load factor H-signal	F_{QH}	100
L-signal	F_{QL}	10
Input load factor, each input	F_I	1
Logic	$Q = \overline{ABC}$	

Hex Inverter with Strobe Inputs



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor H-signal	F_{QH}	100
L-signal	F_{QL}	10
Input load factor A-inputs	F_I	1
strobe 1	F_I	4
strobe 2	F_I	2

Logic $Q = \overline{A \text{ strobe}}$

FZH 211
FZH 215
FZH 231
FZH 235

order numbers

FZH 112:	Q67000–H639
FZH 215:	Q67000–H640
FZH 231:	Q67000–H642
FZH 235:	Q67000–H643

Tentative data

FZH 211/215, Quadruple 2-Input NAND-Gate with Open Collector Output and N-Input
FZH 231/235 Dual 5-Input NAND-Gate with Open Collector Output and N-Input
Calculation of the collector resistance see FZH 161/165

Electrical characteristics
12-V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	8			4.5	V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=15$ mA	1		0.9	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	4		0.8	1.5	mA
H-output current, each output	I_{QH}	$V_S=V_{SB}$ $V_{IL}=4.5$ V, $V_{QH}=18$ V	8			80	µA
H-supply-current, each gate	I_{SH}	$V_S=V_{SA}$ $V_I=0$ V	6		1.0	1.7	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		0.4	1.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			8.5	18	mW

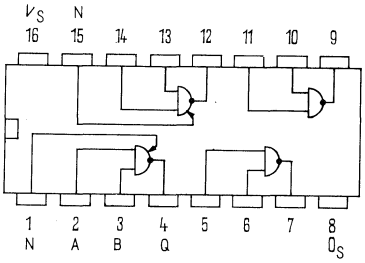
Electrical characteristics

15 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	1	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}	8			4.5	V
L-output voltage	V_{IL}	$V_S=V_{SB}$ V_{IH}=7.5 V, I_{QL}=18 mA	1		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	3			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V	4		1.0	1.8	mA
H-output current, each output	I_{QH}	$V_S=V_{SB}$ V_{IL}=4.5 V, V_{QH}=18 V	8			80	µA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ V_I=0 V	6		1.3	2.1	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$	7		0.7	1.4	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1			15	30	mW

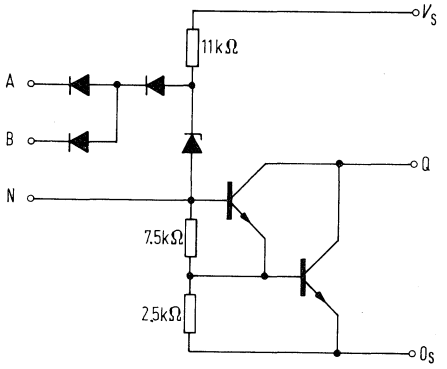
FZH 211
FZH 215

Quadruple 2-Input NAND-Gate with Open Collector Output and N-Input



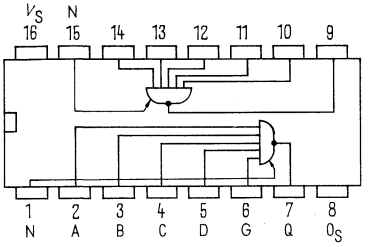
Pin configuration
top view

Schematic (each gate)



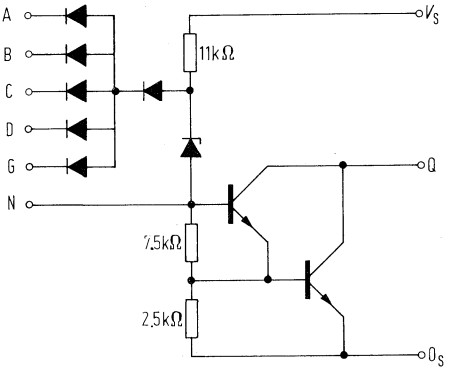
Logical data, each gate		upper limit A
Ouput load factor	F_O	10
Input load factor, each input	F_I	1
Logic	$Q = \overline{AB}$	

Dual 5-Input NAND-Gate with Open Collector Output and N-Input



Pin configuration
top view

Schematic (each gate)



Logical data, each gate		upper limit A
Output load factor	F_O	10
Input load factor, each input	F_I	1
Logic	$Q = \overline{ABCDG}$	

FZH 241
FZH 245

FZH 241: Q67000–H645
FZH 245: Q67000–H646

Dual 5-Input NAND-Schmitt-Trigger with Expander Nodes

Tentative data

The number of inputs can be expanded as required by means of additional input diodes BAW 76 at the expander input N_1. The anodes of the diodes must be connected in parallel to N_1.

Electrical characteristics

12 V-range
temperature ranges 1 and 5

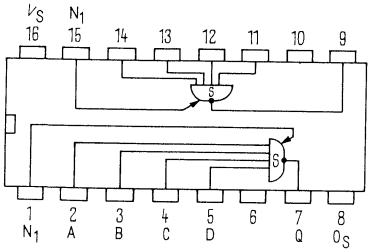
		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
Upper threshold voltage	V_{Su}	V_S=12.0 V		6.5		V
Lower threshold voltage	V_{Sl}	V_S=12.0 V		5.6		V
Hysteresis	V_{Hy}	V_S=12.0 V		0.9		V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} V_{IL}=4.5 V, $-I_{QH}$=0.1 mA	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ V_{IH}=8.0 V, I_{QL}=15 mA		0.9	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V			1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ V_I=0 V, T_A=25 °C	9.0	15.0	25.0	mA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ V_I=0 V		4.0	6.3	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$		4.0	6.3	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1		48		mW

Electrical characteristics

15 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
Upper threshold voltage	V_{Su}	V_S=15.0 V		6.4		V
Lower threshold voltage	V_{Sl}	V_S=15.0 V		5.5		V
Hysteresis	V_{Hy}	V_S=15.0 V		0.9		V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} V_{IL}=4.5 V, $-I_{QH}$=0.1 mA	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ V_{IH}=7.5 V, I_{QL}=18 mA		1.1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$ V_I=1.7 V			1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ V_I=0 V, T_A=25 °C	9	15	25	mA
H-supply current, each gate	I_{SH}	$V_S=V_{SA}$ V_I=0 V		4.5	7.3	mA
L-supply current, each gate	I_{SL}	$V_S=V_{SA}$ $V_I=V_{IHA}$		5.0	8.0	mA
Power consumption, each gate	P	$V_S=V_{SA}$ duty cycle 1:1		72		mW

FZH 241
FZH 245



Pin configuration
top view

Logical data, each gate		upper limit A
Output load factor H-signal	F_{QH}	100
L-signal	F_{QL}	10
Input load factor, each input	F_I	1

Logic $Q = \overline{ABCD}$

FZJ 101
FZJ 105
FZJ 111
FZJ 115

order numbers

FZJ 101:	Q67000–J95
FZJ 105:	Q67000–J124
FZJ 111:	Q67000–J96
FZJ 115:	Q67000–J125

FZJ 101/105 JK-Master-Slave-Flipflop with two J and K-Inputs
FZJ 111/115 JK-Master-Slave Flipflop with N-Inputs

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	22	7.5			V
L-input voltage at any input except C	V_{IL}	$V_S=V_{SB}$ and V_{SA}	22			4.5	V
L-input voltage at C	V_{IL}	$V_S=V_{SB}$ and V_{SA}	22			4.0	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA}, $V_{IL}=4.5$ V, $-V_{QH}=0.1$ mA	22	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $V_{IH}=7.5$ V, $I_{QL}=15$ mA	22		1.0	1.7	V
DC noise margin							
H-signal	V_{nm}			2.5	5.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current at any input except C	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	23			1.0	µA
H-input current at C	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	23			3.0	µA
L-input current at any input except C	$-I_{IL}$	$V_S=V_{SA}$, $V_{IL}=1.7$ V	24		0.8	1.5	mA
L-input current at C	$-I_{IL}$	$V_S=V_{SA}$, $V_{IL}=1.7$ V	24		1.6	3.0	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_I=0$ V, $T_A=25$ °C	25	10.0	30.0	50.0	mA
Supply current	I_S	$V_S=V_{SA}$	23		8.0	14.0	mA

Delay times, $V_S=12$ V, $F_Q=1$, $T_A=25$ °C

Clock pulse duration	t_{pC}	at 50%		0.6			µs
Reset pulse duration	t_{pR}			1.0			µs
Set pulse duration	t_{pS}			1.0			µs
Hold time	t_H			0			ns
Setup time	t_S			0			ns
Maximum clock frequency	f	duty cycle 1:1		0.2	0.5		MHz
Transition time	t_{TLH}	$C_L=10$ pF	31	200	340	570	ns
Transition time	t_{THL}		31	70	120	210	ns
Propagation delay from C to Q	t_{PLH}	$C_L=10$ pF at 4.5 V above ground	31	160	290	520	ns
	t_{PHL}		31	270	450	770	ns
Propagation delay from $\bar{R}$ or $\bar{S}$ to Q	t_{PLH}		30	70	165	330	ns
	t_{PHL}		30	180	330	580	ns

Note: $\bar{R}$ and $\bar{S}$ are approx. 1.5 normalized loads dynamically.

FZJ 101
FZJ 105
FZJ 111
FZJ 115

Electrical characteristics

15 V-range
temperature ranges 1 and 5

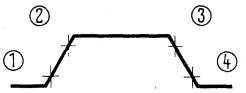
		test condition	test cct.	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S			13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	22	7.5			V
L-input voltage at any input except C	V_{IL}	$V_S=V_{SB}$ and V_{SA}	22			4.5	V
L-input voltage at C	V_{IL}	$V_S=V_{SB}$ and V_{SA}	22			4.0	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	22	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=18$ mA	22		1.1	1.7	V
DC noise margin							
H-signal	V_{nm}			4.5	8.0		V
L-signal	V_{nm}			2.8	5.0		V
H-input current at any input except C	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$	23			1.0	µA
H-input current at C	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$	23			3.0	µA
L-input current at any input except C	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	24		1.0	1.8	mA
L-input current at C	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V	24		2.0	3.6	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=0$ V, $T_A=25$ °C	25	15.0	37.0	60.0	mA
Supply current	I_S	$V_S=V_{SA}$	23		11.0	20.0	mA

Delay times, $V_S=15$ V, $F_Q=1$, $T_A=25$ °C

Clock pulse duration	t_{pC}	at 50%		0.6			µs
Reset pulse duration	t_{pR}	at 50%		1.0			µs
Set pulse duration	t_{pS}	at 50%		1.0			µs
Hold time	t_H	at 50%		0			ns
Setup time	t_S	at 50%		0			ns
Maximum clock frequency	f	duty cycle 1:1			0.5		MHz
Transition time	t_{TLH}	$C_L=10$ pF	31		410		ns
Transition time	t_{THL}	$C_L=10$ pF	31		75		ns
Propagation delay from C to Q	t_{PLH}	$C_L=10$ pF at 4.5 V above ground	31		330		ns
Propagation delay from C to Q	t_{PHL}	$C_L=10$ pF at 4.5 V above ground	31		470		ns
Propagation delay from $\overline{R}$ or $\overline{S}$ to Q	t_{PLH}	$C_L=10$ pF at 4.5 V above ground	30		195		ns
Propagation delay from $\overline{R}$ or $\overline{S}$ to Q	t_{PHL}	$C_L=10$ pF at 4.5 V above ground	30		340		ns

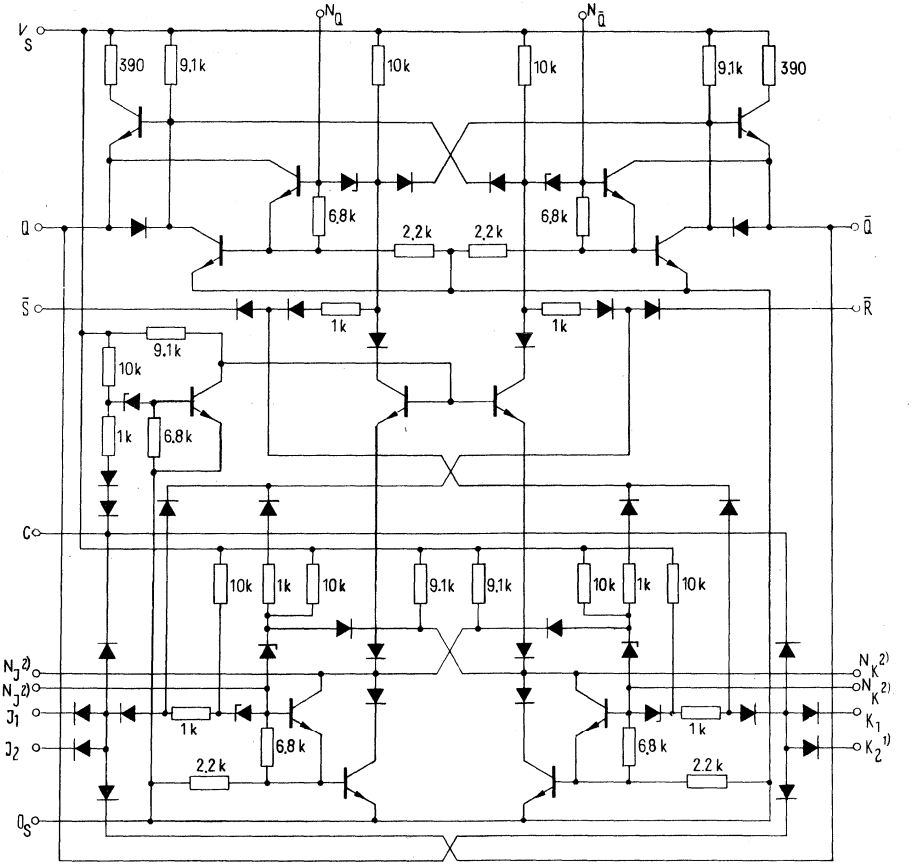
Note: R and S are approx. 1.5 normalized loads dynamically.

Clock pulse



1 isolate slave from master
2 enter signal from J and K into master
3 disable inputs J and K
4 transfer information from master to slave

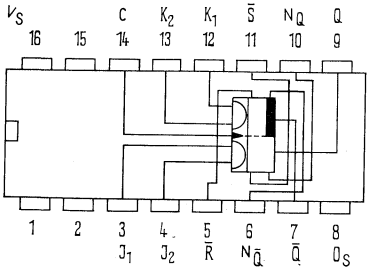
Schematic



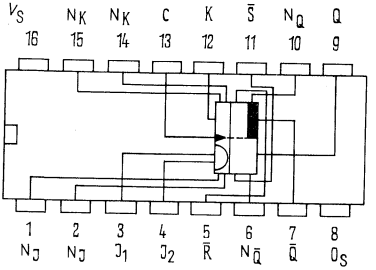
$\bar{R}$ = reset input, $\bar{S}$ = set input, C = clock input

[1]) FZJ 101/105 only [2]) FZJ 111/115 only

FZJ 101
FZJ 105
FZJ 111
FZJ 115



FZJ 101/105
Pin configuration
top view



FZJ 111/115
Pin configuration
top view

Logical data			upper limit A
Output load factor, each output	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor at C	H-signal	F_{IH}	3
	L-signal	F_{IL}	2
Input load factor remaining inputs		F_I	1

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

$J = J_1J_2$
$K = K_1K_2$ FZJ 101/115 only
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

L-level at $\bar{R}$ sets Q to L
L-level at $\bar{S}$ sets Q to H
$\bar{R}$ and $\bar{S}$ operate independent of C.

order numbers

FZJ 121: Q67000–J385
FZJ 125: Q67000–J386

FZJ 121
FZJ 125

Dual JK-Master-Slave Flipflop with Set and Reset

Tentative data

Electrical characteristics

12 V-range
temperature range 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage at C	V_{IH}	$V_S=V_{SB}$	6.5			V
L-input voltage at C	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.0	V
H-input voltage at J and K	V_{IH}	$V_S=V_{SB}$	8.0			V
L-input voltage at J and K	V_{IL}	$V_S=V_{SB}$ and V_{SA}			5.5	V
H-input voltage at $\bar{R}$ and $\bar{S}$	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage at $\bar{R}$ and $\bar{S}$	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V[1], $-I_{QL}=0.1$ mA	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V[1], $I_{QL}=15$ mA		1.0	1.7	V
DC noise margin						
H-signal	V_{nm}		2.0	5.0		V
L-signal	V_{nm}		2.3	5.0		V
H-input current at C	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$			3.0	µA
H-input current at J, K, $\bar{R}$ and $\bar{S}$	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$			1.0	µA
L-input current at C, $\bar{R}$ and $\bar{S}$	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V		1.6	3.0	mA
L-input current at J, K	$-I_{IL}$	$V_S=V_{SA}$ $V_{IL}=1.7$ V		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ $V_I=0$ V	9.0	15.0	25.0	mA
Supply current	I_S	$V_S=V_{SA}$		15.0	24.0	mA

[1]) V_I applied to $\bar{R}$ and $\bar{S}$ resp.

FZJ 121
FZJ 125

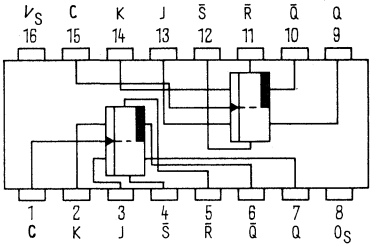
Electrical characteristics

15 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15.0	17.0	V
H-input voltage at C	V_{IH}	$V_S=V_{SB}$	6.5			V
L-input voltage at C	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.0	V
H-input voltage at J and K	V_{IH}	$V_S=V_{SB}$	8.0			V
L-input voltage at J and K	V_{IL}	$V_S=V_{SB}$ and V_{SA}			5.5	V
H-input voltage at $\bar{R}$ and $\bar{S}$	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage at $\bar{R}$ and $\bar{S}$	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} V_{IL}=4.5 V[1]) I_{QH}=–0.1 mA	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ V_{IH}=7.5[1]), I_{QL}=18 mA		1.1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.0	8.0		V
L-signal	V_{nm}		2.3	5.0		V
H-input current at	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$			3.0	µA
H-input current at J, K, $\bar{R}$ and $\bar{S}$	I_{IH}	$V_S=V_{SA}$ $V_I=V_{IHA}$			1.0	µA
L-input current at C, $\bar{R}$ and $\bar{S}$	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V		2.0	3.6	mA
L-input current at J, K	$-I_{IL}$	$V_S=V_{SA}$ V_{IL}=1.7 V		1.0	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$ V_I=0 V	9.0	15.0	25.0	mA
Supply current	I_S	$V_S=V_{SA}$		20.0	32.0	mA

[1]) V_I applied to $\bar{R}$ and $\bar{S}$ resp.

FZJ 121
FZJ 125



Pin configuration
top view

Truth table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
L-level at $\bar{R}$ sets Q to L.
L-level at $\bar{S}$ sets Q to H.
$\bar{R}$ and $\bar{S}$ operate independent of C.

Logical data, each flipflop			upper limit A
Output load factor	H-signal	F_{QH}	100
each output	L-signal	F_{QL}	10
Input load factor			
at C	H-signal	F_{IH}	3
at $\bar{R}$ and $\bar{S}$	H-signal	F_{IH}	1
at C, $\bar{R}$ and $\bar{S}$	L-signal	F_{IL}	2
remaining inputs		F_I	1

FZJ 131
FZJ 135

order numbers:

FZJ 131: Q67000-J388
FZJ 135: Q67000-J389

Quadruple D-Flipflop (Tentative Data)

The FZJ 131/135 contain four D-flipflops. Information present at the D-input is transferred to the Q-output while the clock input C is at H. The D-input is disabled at C = L.
Application: 4 bit scratch pad memory

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$, $-I_Q=0.1$ mA $V_{IH}=7.5$ V	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $I_Q=15$ mA $V_{ID}=4.5$ V, $V_{IC}=7.5$ V		0.9	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_I	$V_I=V_S=V_{SA}$			1	μA
L-input current at D	$-I_I$	$V_S=V_{SB}$, $V_I=1.7$ V			3	mA
L-input current at C	$-I_I$	$V_S=V_{SA}$, $V_I=1.7$ V			6	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_I=V_Q=0$ V	9	15	25	mA
Supply current	I_S	$V_S=V_{SA}$, $V_I=0$ V		22	32	mA
Power consumption	P	$V_S=V_{SA}$, $V_I=0$ V		264	432	mW

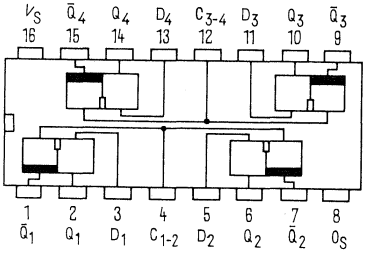
Electrical characteristics

15 V-range temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15	17	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-input voltage	V_{QH}	$V_S=V_{SB}$, $-I_Q=0.1$ mA $V_{IH}=7.5$ V	12.0	14.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$, $I_Q=18$ mA $V_{ID}=4.5$ V, $V_{IC}=7.5$ V		1.0	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8		V
L-signal	V_{nm}		2.8	5		V
H-input current, each input	I_I	$V_I=V_S=V_{SA}$			1	μA
L-input current at D	$-I_I$	$V_S=V_{SA}$, $V_I=1.7$ V			3.6	mA
L-input current at C	$-I_I$	$V_S=V_{SA}$, $V_I=1.7$ V			7.2	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_I=V_Q=0$ V	9	15	25	mA
Supply current	I_S	$V_S=V_{SA}$, $V_I=0$ V		28	42	mA
Power consumption	P	$V=V$, $V_I=0$ V		420	720	mW

Logical data, each flipflop

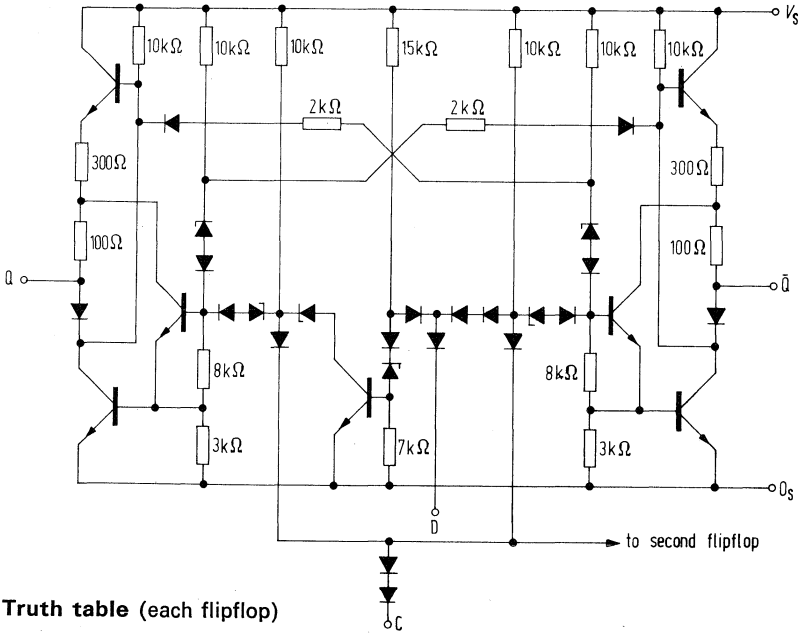
Output load factor	F_{QH}		100
each output	F_{QL}		10
Input load factor at D	F_I		2
Input load factor at C	F_I	for 2 flipflops	4

FZJ 131
FZJ 135



Pin configuration
top view

Schematic (each flipflop)



Truth table (each flipflop)

inputs C	inputs D_n	output Q_{n+1}
L	L	Q_n
L	H	Q_n
H	L	L
H	H	H

n: bit time before clock pulse
n+1: bit time after clock pulse

order numbers:

FZJ 141: Q67000–J391
FZJ 145: Q67000–J392
FZJ 151: Q67000–J394
FZJ 155: Q67000–J395

FZJ 141
FZJ 145
FZJ 151
FZJ 155

Synchronous Counters (Tentative data)

FZJ 141/145 Synchronous Decimal Counter
FZJ 151/155 Synchronous 4-Bit-Binary Counter

The FZJ 141/145 and FZJ 151/155 are synchronous counters with set inputs for each bit, a common reset input, clock and carry gating. The information is stored in JK-flipflops. It is available at the outputs Q. The information is transferred to the Q-outputs at the trailing edge of the clock pulse.

Electrical characteristics

12 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$, $-I_Q=0.1$ mA	10.0	11.3		V
L-output voltage	V_{QH}	$V_S=V_{SB}$, $I_Q=15$ mA		0.9	1.7	V
DC noise margin, H-signal	V_{nmH}		2.5	5		V
L-signal	V_{nmL}		2.8	5		V
H-input current, each input	I_{IH}	$V_S=V_I=V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, $V_I=1.7$ V		0.8	1.5	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_Q=0$ V	9	15	25	mA
H-supply current	I_{SH}	$V_S=V_{SA}$, $V_I=V_{SA}$		12		mA
L-supply current	I_{SL}	$V_S=V_{SA}$		20		mA
		input $\overline{R}$: $V_I=0$ V remaining inputs: $V_I=V_{SA}$				

FZJ 141
FZJ 145
FZJ 151
FZJ 155

Electrical characteristics

15 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$, $-I_Q=0.1$ mA	12	14.3		V
L-output voltage	V_{QH}	$V_S=V_{SB}$, $I_Q=18$ mA		1	1.7	V
DC noise margin, H-signal	V_{nmH}		4.5	8		V
L-signal	V_{nmL}		2.8	5		V
H-input current, each input	I_{IH}	$V_S=V_I=V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, $V_I=1.7$ V		1	1.8	mA
Short circuit output current, each output	$-I_Q$	$V_S=V_{SA}$, $V_Q=0$ V	9	15	25	mA
H-supply current	I_{SH}	$V_S=V_{SA}$, $V_I=V_{SA}$		15		mA
L-supply current	I_{SL}	$V_S=V_{SA}$ input $\overline{R}$: $V_I=0$ V remaining inputs: $V_I=V_{SA}$		23		mA

Logical data

Output load factor, each output	F_{QH}				100	
	F_{QL}				10	
Input load factor, each input	F_I				1	

Truth table: Decimal counter FZJ 141/145

count condition: $\overline{A}=\overline{B}=\overline{C}=\overline{D}=E=E_C=\overline{R}=H$

sequence	outputs C_Q	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	H	H	L	L	H

Truth table: Binary counter FZJ 151/155

count condition: $\overline{A}=\overline{B}=\overline{C}=\overline{D}=E=E_C=\overline{R}=H$

sequence	outputs C_Q	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	H	H	H	H	H

Set and reset conditions

Set and reset inputs operate independent of the clock input C and the enable input E. If these inputs are not used, they must be connected to V_S. To store the information properly first $\overline{R}$ must return to H-level before the inputs $\overline{A}$ through $\overline{D}$.

inputs $\overline{R}$	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	outputs Q_A	Q_B	Q_C	Q_D
L	H	H	H	H	L	L	L	L
L	L	X	X	X	H	X	X	X
L	X	L	X	X	X	H	X	X
L	X	X	L	X	X	X	H	X
L	X	X	X	L	X	X	X	H

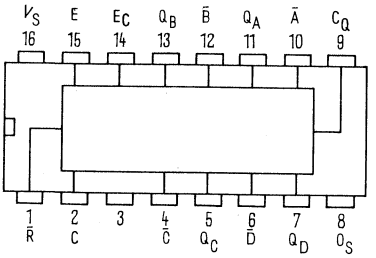
X = L or H-signal

Enable conditions

enable E	operating mode
L	inhibit
H	count

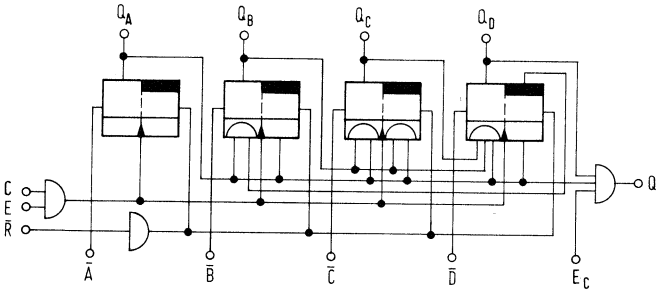
enable E_C	Carry output C_Q
L	L
H	L or H

FZJ 141
FZJ 145
FZJ 151
FZJ 155

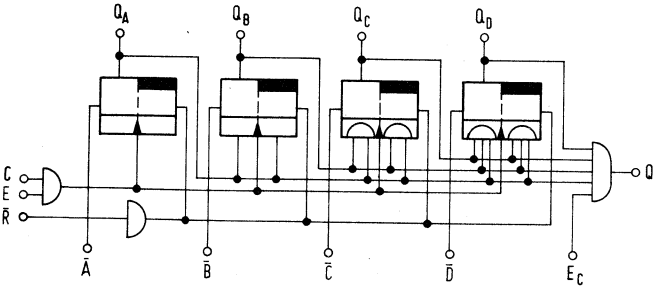


Pin configuration, top view

Block diagram of FZJ 141/145



Block diagram of FZJ 151/155



order numbers:

FZK 101: Q67000–K6
FZK 105: Q67000–K7

FZK 101
FZK 105

Timing Circuit with N-Input (Tentative data)

The FZK 101/105 feature the following operating modes:
1. Monostable multivibrator. L, J, and M connected.
2. Pulse delay. L and K connected.
3. Pulse reduction. J and M connected.
4. Delay switch, L-K and M-O_S connected.
5. Pulse delay is retriggerable if the retrigger pulse returns before the recovery time is elapsed.
6. An electrolytic capacitor can be used as timing component C_t.
7. When the supply voltage V_S is switched on, Q remains at L only if $\bar{R}$ is supplied with an L-level.
8. No voltages and currents may be applied to the function inputs J, K, L, M. The required connection between J, K, L, M may not exceed 5 mm.
9. Inputs A or B must be supplied with an L-level, if C and D are used as trigger inputs.

Electrical characteristics 12 V-range temperature ranges 1 and 5		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{QH}	$V_S=V_{SB}$ and V_{SA} $V_{IL}=4.5$ V, $-I_{QH}=0.1$ mA	10.0	11.3		V
L-output voltage	V_{QL}	$V_S=V_{SB}$ $V_{IH}=7.5$ V, $I_{QL}=15$ mA		1.0	1.7	V
DC noise margin						
H-signal	V_{nm}		2.5	5.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, $V_{IL}=1.7$ V		0.8	1.5	mA
Short circuit output current	$-I_Q$	$V_S=V_{SA}$, $T_A=25$ °C	10.0	30.0	50.0	mA
L-supply current	I_{SL}			13.:	18.5	mA
H-supply current	I_{SH}			12.0	17.0	mA

FZK 101
FZK 105

Electrical characteristics
15 V-range
temperature ranges 1 and 5

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	7.5			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ and V_{SA}			4.5	V
H-output voltage	V_{IH}	$V_S=V_{SB}$ and V_{SA} V_{IL}=4.5 V, $-I_{QH}$=0.1 mA	12.0	14.3		V
L-output voltage	V_{IL}	$V_S=V_{SB}$ V_{IH}=7.5 V, I_{QL}=18 mA		1.1	1.7	V
DC noise margin						
H-signal	V_{nm}		4.5	8.0		V
L-signal	V_{nm}		2.8	5.0		V
H-input current, each input	I_{IH}	$V_S=V_{SA}$, $V_I=V_{IHA}$			1.0	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, V_{IL}=1.7 V		1.0	1.8	mA
Short circuit output current	$-I_Q$	$V_S=V_{SA}$, T_A=25 °C	15.0	37.0	50.0	mA
H-supply current	I_{SH}			14.0	20.0	mA
L-supply current	I_{SL}			15.0	21.5	mA

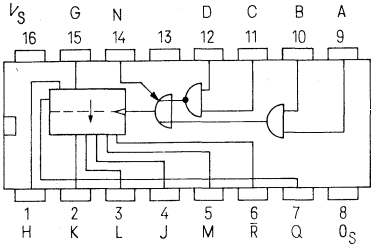
Delay times, 12 and 15 V-ranges

Propagation delay	t_{PLH}			270		ns
Propagation delay at pulse reduction, and reset mode at pulse delay and delay switch	t_{PHL}			$0.1 \cdot t_t$		ns
Propagation delay at remaining operating modes	t_{PHL}			180		ns
Input pulse duration	t_I		500			ns
Output pulse duration	t_Q		400			ns
Transition time of trigger pulse at A, B, C, D	t_T		1			V/µs
Recovery time	t_t			(C_0+C_t) 10^3		s, F
Reset pulse duration	t_R		500			ns

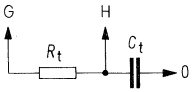
Timing components

Resistance	R_t		5		500	kΩ
Recommended resistance range for high accuracy	R_t		40		200	kΩ
Capacitance	C_t			no limitation		µF
Capacitance	C_N		0		500	pF
Internal capacitance between H and O_S	C_0			10		pF

FZK 101
FZK 105

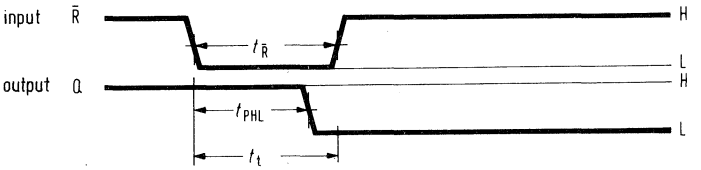


Pin configuration
top view

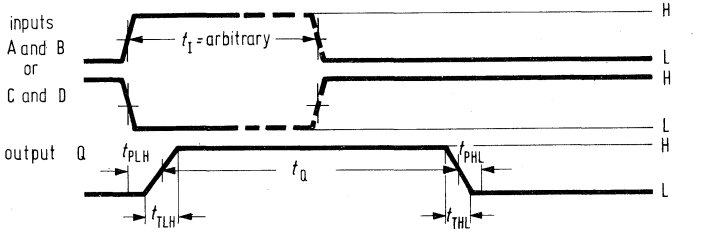


Logical data			upper limit A
Output load factor	H-signal	F_{QH}	100
	L-signal	F_{QL}	10
Input load factor, each input		F_I	1
Logic		Q = (AB) + ($\overline{CD}$) see pulse diagram	

Pulse diagrams for:



reset mode (applies for every operating mode)

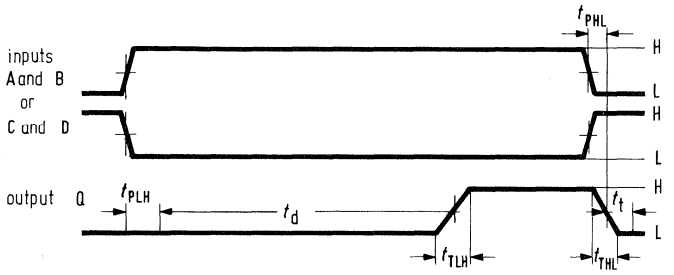


monostable multivibrator (L, J, and M connected)

$t_Q = 0.7 \cdot R_t \cdot (C_0 + C_1)$

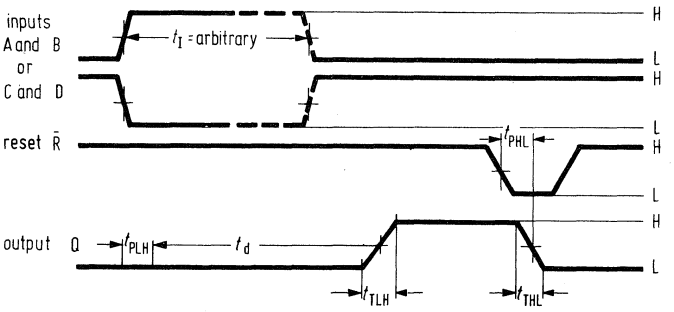
FZK 101
FZK 105

Pulse diagrams for:



Pulse delay
(L and K connected)

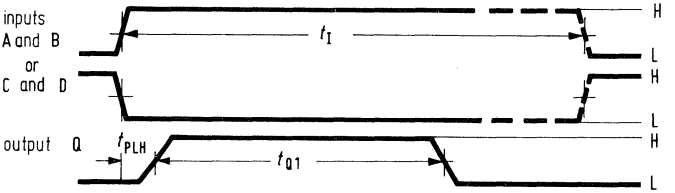
$t_d = 0.7 \cdot R_t \cdot (C_0 + C_t)$



Delay switch
(L-K and M-S_S connected)

Reset to Q=L by means of R=L only

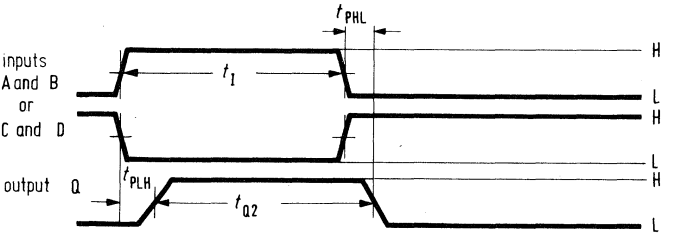
$t_d = 0.7 \cdot R_t \cdot (C_0 + C_t)$



Pulse reduction
(J and M connected)

a) $t_I > 0.7 \cdot R_t \cdot (C_0 + C_t)$

$t_{Q1} = 0.7 \cdot R_t \cdot (C_0 + C_t)$



b) $t_I \leqq 0.7 \cdot R_t \cdot (C_0 + C_t)$

$t_{Q2} = t_I$

Order number:
FZL: Q67000–L68

FZL 101

BCD-Decimal-Decoder-Driver for Indicator Tubes (Tentative Date)

The FZL 101 decodes binary coded decimal numbers. Direct control of indicator tubes is possible by means of output transistors with high breakdown voltages. The FZJ 141 is the corresponding decimal counter. The following conections have to be made from the Q-outputs of the FZJ 141 to the inputs of the FZL 101: Q_A to A, Q_B to B, Q_C to C, and Q_D to D.
Binary input information of the decimal numbers 10 through 15 are suppressed.
In addition the following maximum ratings apply:

In addition the following maximum ratings apply:		lower limit B	upper limit A	unit
Output voltage (output transistor blocked)	V_Q	0	80	V
Output current (output transistor blocked)	I_Q	0	2	mA
each output[1])				
Output current (output transistor conducting)	I_Q	0	20	mA
each output				

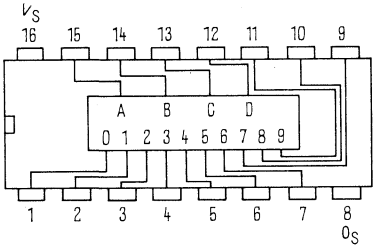
Electrical characteristics 12 V-range temperature range 1		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S		11.4	12.0	13.5	V
H-input voltage	V_{IH}	$V_S=V_{SB}$	8.0			V
L-input voltage	V_{IL}	$V_S=V_{SB}$ und V_{SA}			5.0	V
H-output voltage	V_{QH}	$V_S=V_{SA}$, I_Q=1 mA	80			V
L-output voltage	V_{QL}	$V_S=V_{SB}$, I_Q=9 mA			2.5	V
DC noise margin, H-signal	V_{nmH}		2.0	4.5		V
L-signal	V_{nmL}		3.3	5.5		V
H-output current, each output	I_{QH}	$V_S=V_{SA}$, V_Q=70 V			50	µA
(input combinations	I_{QH}	$V_S=V_{SA}$, V_Q=80 V			1	mA
0 through 9)						
H-output current, each output (input combinations 10 through 15)	I_{QH}	$V_S=V_{SA}$, V_Q=60 V			5	µA
H-input current, each input	I_{IH}	$V_S=V_I=V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, V_I=0 V		0.8	1.5	mA
Supply current	I_S	$V_S=V_{SA}$ input A, C, D: V_I=0 V		17	25	mA
Power consumption	P	input B: $V_I=V_{SA}$		205	340	mW

[1]) only for one output at the some time

FZL 101

Electrical characteristics
15 V-range
temperature range 1

		test condition	lower limit B	typ.	upper limit A	unit
Supply voltage	V_S	$V_S=V_{SB}$	13.5	15.0	17.0	V
H-input voltage	V_{IH}	$V_S=V_{SB}$ and V_{SA}	8.0			V
L-input voltage	V_{IL}	$V_S=V_{SA}$, $I_Q=1$ mA			5.0	V
H-output voltage	V_{QH}	$V_S=V_{SB}$, $I_Q=9$ mA	80			V
L-output voltage	V_{QL}				2.5	V
DC noise margin, H-signal	V_{nmH}		4.0	7.5		V
L-signal	V_{nmL}		3.3	5.5		V
H-output current, each output	I_{QH}	$V_S=V_{SA}$, $V_Q=70$ V			50	µA
(input combinations 0 through 9)	I_{QH}	$V_S=V_{SA}$, $V_Q=80$ V			1	mA
H-output current, each output (input combinations 10 through 15)	I_{QH}	$V_S=V_{SA}$, $V_Q=60$ V			5	µA
H-input current, each input	I_{IH}	$V_S=V_I=V_{SA}$			1	µA
L-input current, each input	$-I_{IL}$	$V_S=V_{SA}$, $V_I=0$ V		1	1.8	mA
Supply current	I_S	$V_S=V_{SA}$ input A, C, D: $V_I=0$ V		18	27	mA
Power consumption	P	input B: $V_I=V_{SA}$		270	460	mW

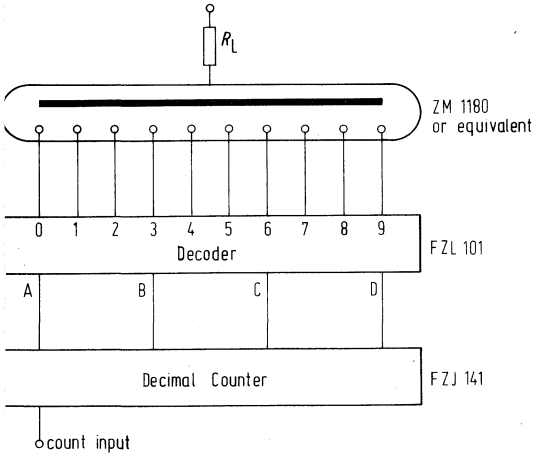


Pin configuration, top view

Truth table

BCD-inputs				decimal outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

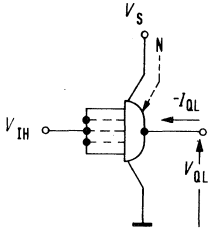
Application with indicator tube



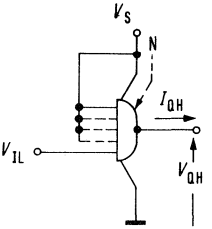
Notes:
Recommended supply voltage for the indicator tube V_S=200 V
Resistance R_L depends on the lighting voltage V_B and the lighting current I_B of the indicator tube.
as follows:

$$R_L = \frac{V_S - V_B}{I_B}\ \Omega$$

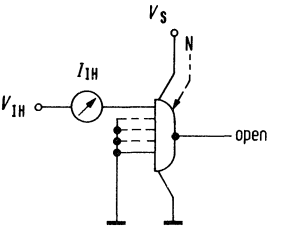
Test circuits



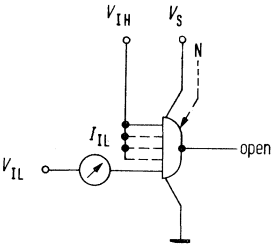
test circuit 1



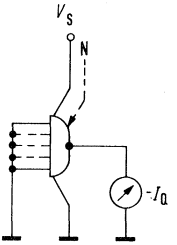
test circuit 2



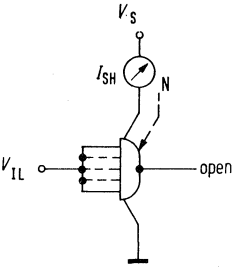
test circuit 3



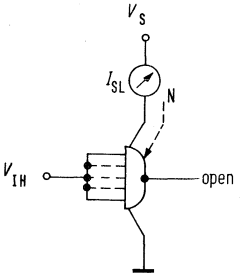
test circuit 4



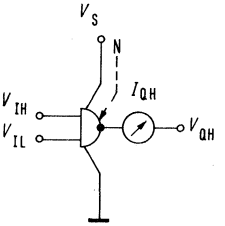
test circuit 5



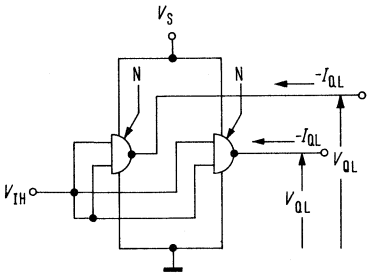
test circuit 6



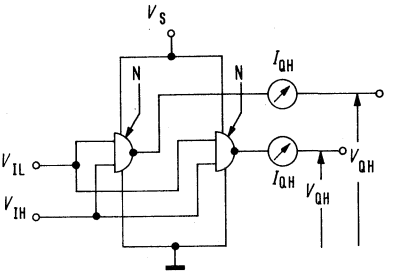
test circuit 7



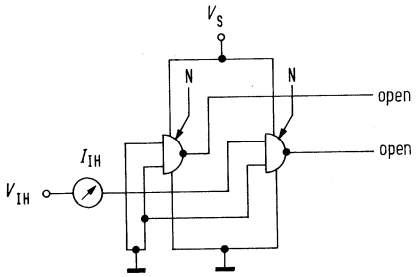
test circuit 8



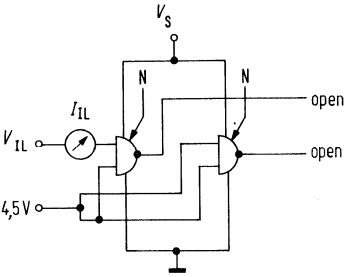
test circuit 9



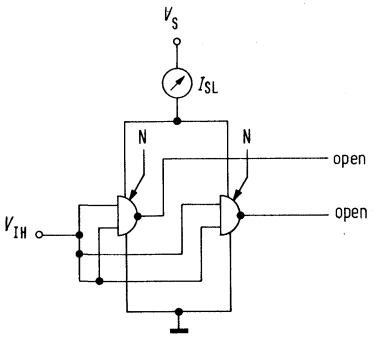
test circuit 10



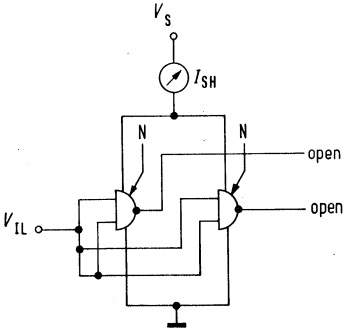
test circuit 11



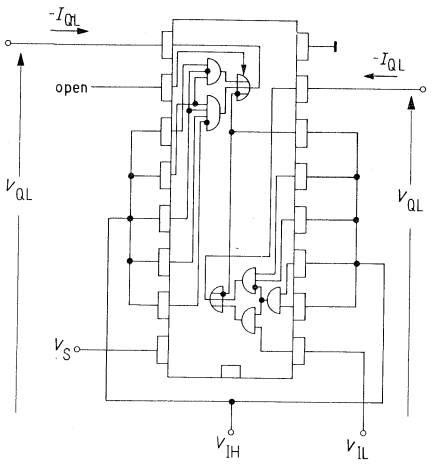
test circuit 12



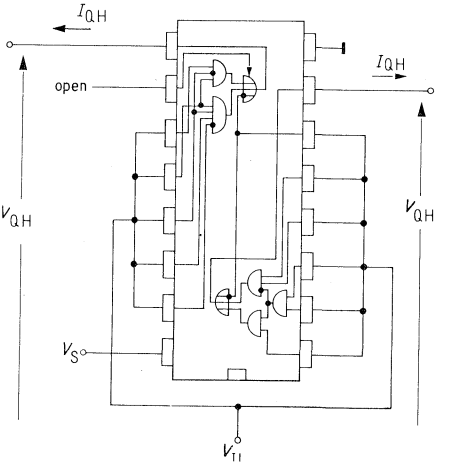
test circuit 13



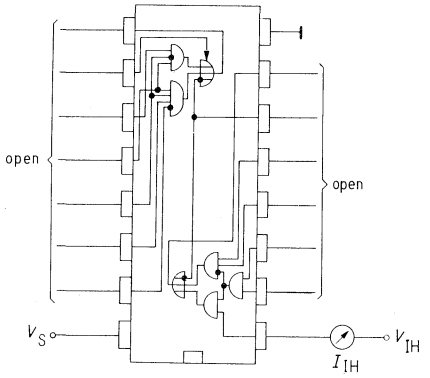
test circuit 14



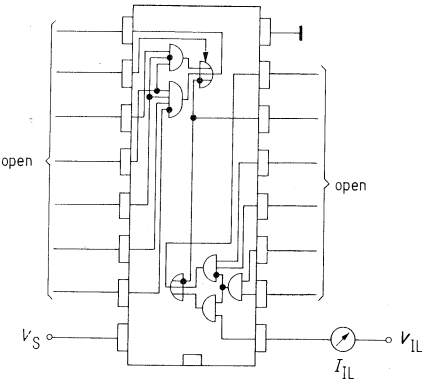
test circuit 15



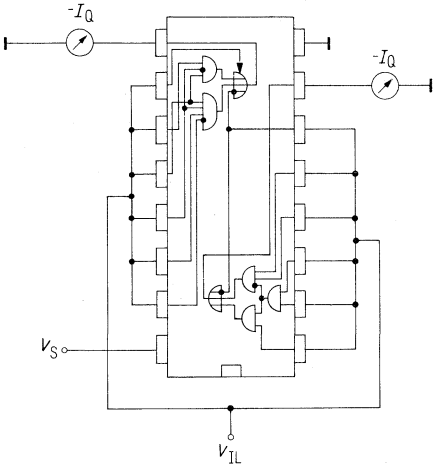
test circuit 16



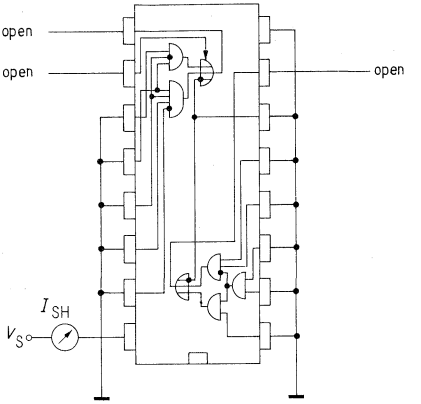
test circuit 17



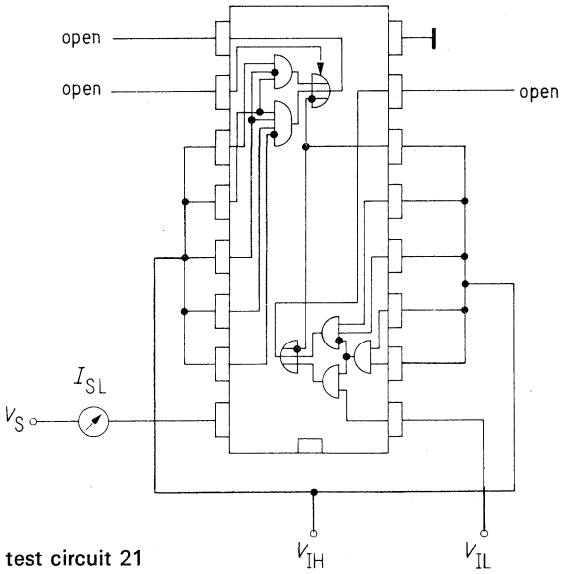
test circuit 18



test circuit 19
each output in tested seperately

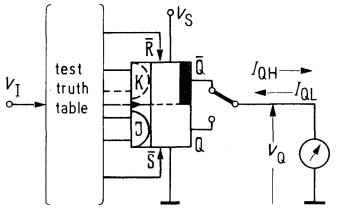


test circuit 20



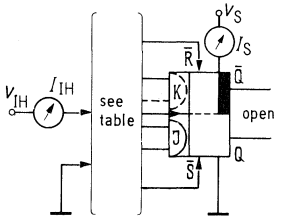
test circuit 21

FZ 100



test circuit 22

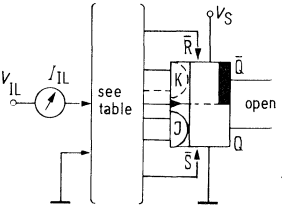
each output is tested seperately



test circuit 23

I_{IH}: each input is tested seperately
I_S: V_{IH} is applied to all inputs

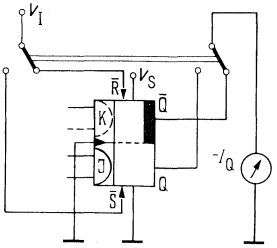
V_{IH} at	ground at
J_1 or J_2	T, $\bar{S}$, J_1, or J_2
K_1 or K_2	T, R, K_1, or K_2
$\bar{R}$	T, J_1, and J_2
$\bar{S}$	T, K_1, and K_2
T	J, J, K, K ,$\bar{R}$, $\bar{S}$



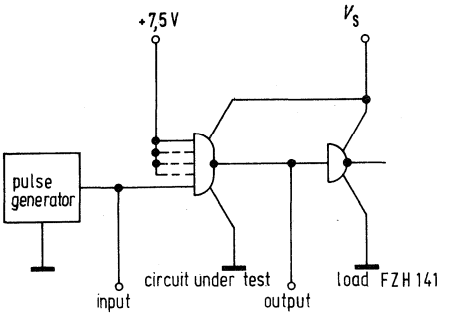
test circuit 24

each input is tested seperately

V_{IL} at	4.5 V at	17 V at
J_1, or J_2	$\bar{R}$	T, J_1, or J_2
K_1, or K_2	$\bar{S}$	T, K_1, or K_2
$\bar{R}$		J_1 and J_2
$\bar{S}$		K_1 and K_2
T		J_1, J_2, K_1, K_2

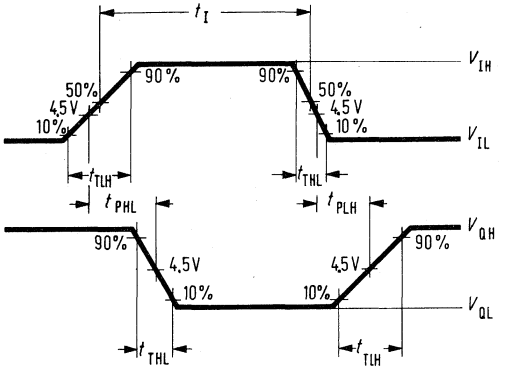


test circuit 25

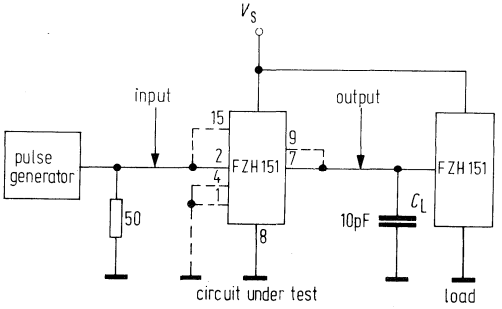


test circuit 26

pulse diagram

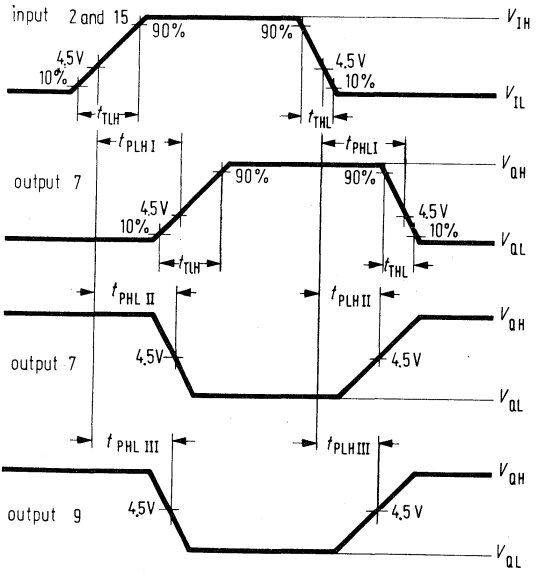


Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 120 ns, t_p = 1 µs, amplitude: +10 V.
The load consits of stray and jig capacitance and one gate FZH 141.

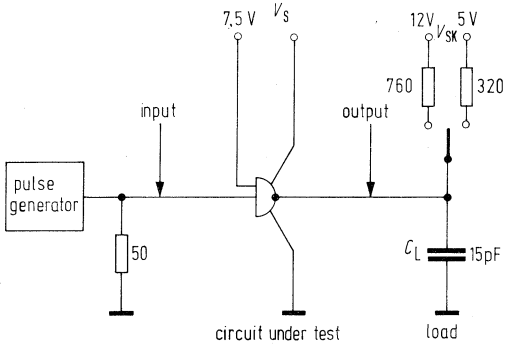


test circuit 27

pulse diagram

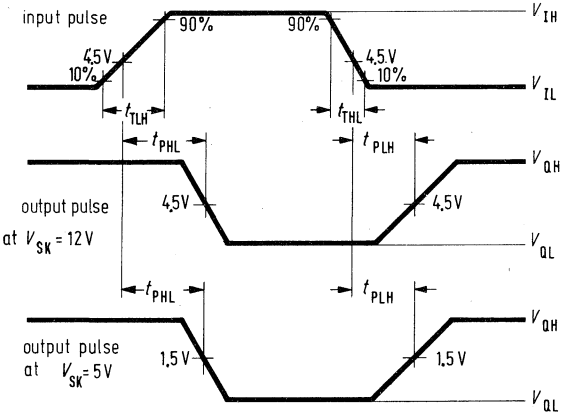


Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 240 ns; amplitude: +10 V.
When measuring t_p between input 2 and output 7, two tests must be made. During the first test input 4 must be grounded. During the second test input 1 must be grounded. When measuring t_p between input 15 and output 9, all inputs must remain open. t_{TLH} and t_{THL} are measured at output 7.

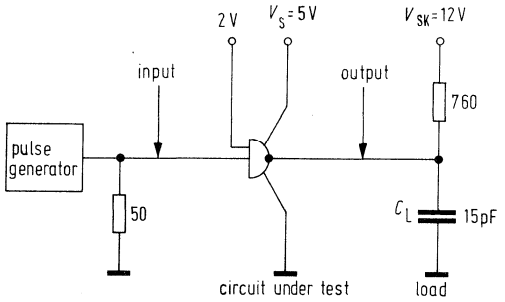


test circuit 28

pulse diagram

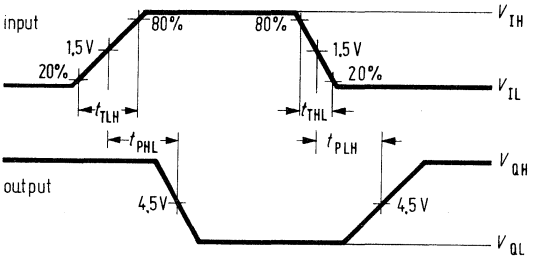


Notes:
generator: t_{TLH} = 350 ns, t_{THL} = 120 ns; amplitude: +10 V.
levels: input pulse 4.5 V above ground, output pulse 1.5 V for V_{SC} = 5 V and 4.5 V for V_{SC} = 12 V above ground.

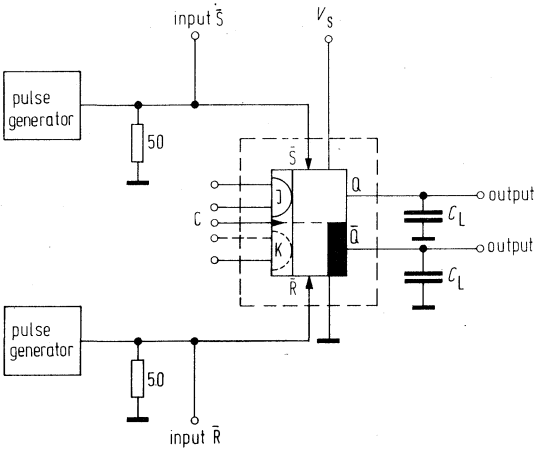


test circuit 29

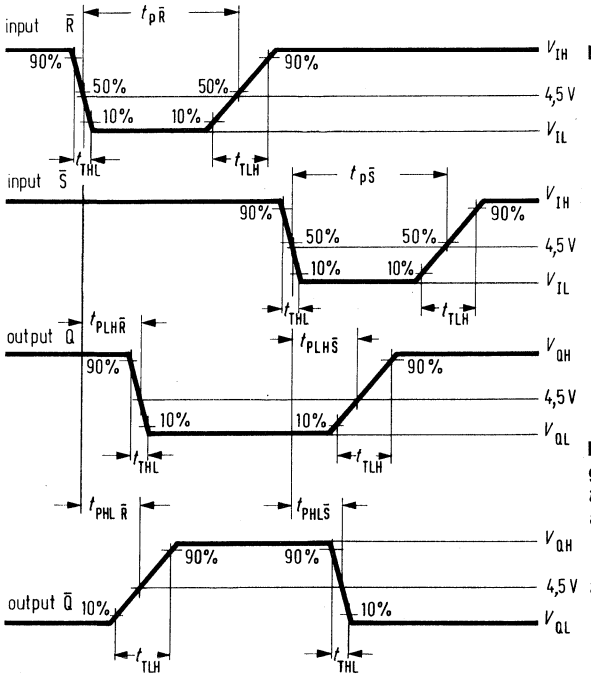
pulse diagram



Notes:
generator: t_{TLH} = 10 ns, t_{THL} = 5 ns; amplitude: +3 V.
levels: input pulse 1.5 V above ground, output pulse 4.5 V above ground.



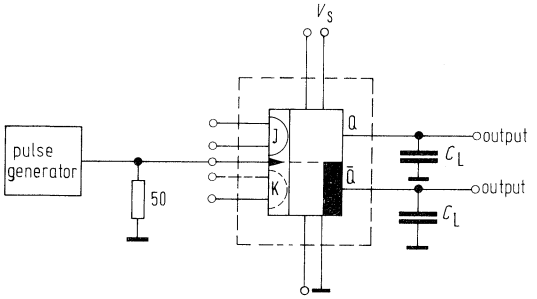
test circuit 30



pulse diagram

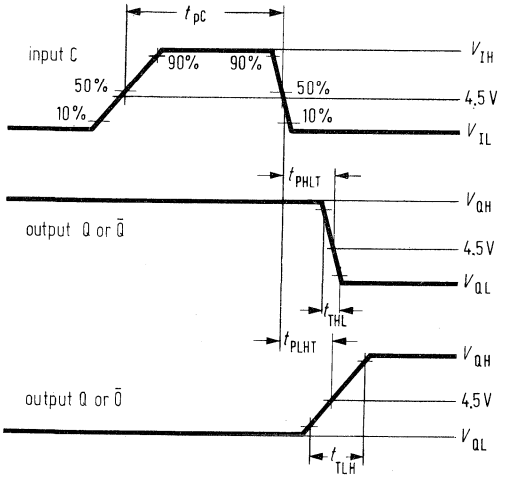
Notes:
generator: t_{THL} = 350 ns, t_{TLH} = 120 ns, $t_{pR} = t_{pS}$ = 700 ns
amplitude: +10 V
unused inputs remain open
C_L includes jig and stray capacitance
$t_{PHL\bar{R}}$ and $t_{PLH\bar{S}}$ are referred to 4.5 V above ground.

FZ 100



test circuit 31

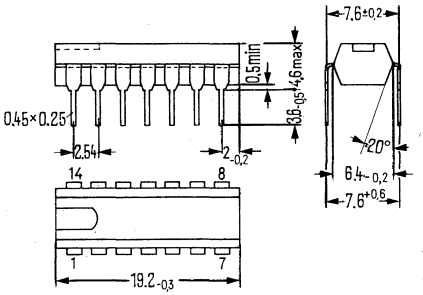
pulse diagram



Notes:
generator: t_{TLH}=350 ns, t_{THL}=120 ns, t_{pT}=400 ns
amplitude = +9 V, +1 V offset
unused inputs remain open
C_L includes jig and stray capacitance.
t_{PHLL} and t_{PLHL} are referred to 4.5 V above ground.

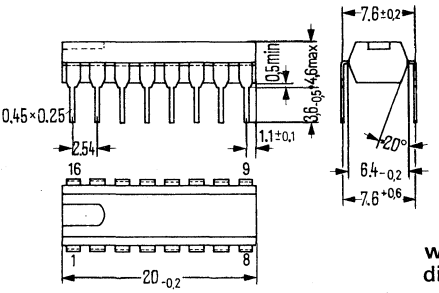
Package outline drawings

Plastic dual-in-linie package 14 pins 20 A 14 DIN 41866 (TO-116)



weight approx. 1.1 g
dimensions in mm

Plastic dual-in-line package 16 pins 20 A 16 DIN 41 866



weight approx. 1.2 g
dimensions in mm

4. MOS-series (Metall-Oxide-Silicon)

MOS-Series

Table of contents

■ Not for new developments

General Information on the MOS (Metal-Oxide-Silicon) circuits

The circuits of series FDN, GD and SAJ are monolithic integrated semiconductor circuits in p-channel MOS-technique. In addition to a high level of integration, these circuits show an outstanding noise rejection, low power requirement and high input resistance. The outputs have been provided with TTL-compatible power stages. All inputs are protected against static over-voltages through protection devices (see "Protective measures for MOS circuits").

Besides the standard circuits listed in this catalog, such as

shift registers
RAMs
ROMs and
frequency-dividers,

Siemens offers the development of MOS custom circuits with special functions and properties a customer needs for a specific application.
Moreover, variations of standard circuits and sub-systems such as

multiplexers
decoders
counters
serial/parallel converters
arithmetic elements
control logic circuits,

and even entire digital systems, can be realized in MOS

Integration levels of 150 to 250 gate-functions per chip can be realized, depending on the structure of logic. The maximum size of a multichip MOS-system is limited only by the reguired system operating frequency; for large systems this will usually have to be below 1 MHz.
For an MOS custom development, a detailed description of system functions, logic diagrams, logic equations or a TTL-logic may be used as a basis for the MOS-design. Siemens offers their customers support in working out an MOS-suited logic, MOS-specifications and an optimal partitioning in case of a multichip-system. The customer may enter into an agreement for MOS-development at various stages of system documentation, extending from a general system concept through logik and MOS-layout to masks. These stages (1 through 6), at which cooperation of a customer with Siemens on an MOS custom-project may start, are shown on the "Working Scheme for MOS Custom Development Projects".

Protection measures for MOS circuits

To guard the sensitive MOS-circuits against destructive static overvoltages and electrical spikes, protection devices have been integrated on the chips at all inputs and outputs. They function as follows:

1. In the case of positive overvoltages a p-n-junction becomes conducting in forward direction, to substrate.
2. Negative overvoltages cause a Zener-type diode conduction with a resistance-limited current into substrate.
3. In addition, all inputs and outputs are connected to thick-oxide protection transistors with a turn-on voltage of –35 V; these devices will short-circuit inputs or outputs subjected to overvoltages.

It should be kept in mind however, that these devices can provide only a limited protection; floors, table tops, chairs, work clothes and carrying trays made of highly insulating material can enable static charges to build up beyond the maximum rating of MOS protection devices and should therefore be avoided in MOS work areas. Operators and equipment getting in contact with MOS-circuits should be electrically grounded through a current-limiting resistor (about 100 k).

Glossary of abbreviations used for MOS-circuits

Voltages

V	Voltage, general
V_{CC}	Supply voltage
V_{SS}	Substrate supply voltage
V_{DD}	Drain supply voltage
V_{GG}	Gate supply voltage
V_{ZZ}	Additional supply voltage for particular cells or stages (for example GDQ 101)
V_{IH}	High level at a signal input
V_{IL}	Low level at a signal input
V_{OH}	High level at an output
V_{OL}	Low level at an output
$V_{\Phi H}$	High level at a clock input
$V_{\Phi L}$	Low level at a clock input
V_I	Voltage at a signal input
V_Φ	Voltage at a clock input
$V_{\Phi 1}$	Voltage at clock 1 input
$V_{\Phi 2}$	Voltage at clock 2 input
$V_{\Phi 3}$	Voltage at clock 3 input
$V_{\Phi 4}$	Voltage at clock 4 input
V_{AH}	High level at an address input
V_{AL}	Low level at an address input
V_A	Voltage at an address input
V_{OS}	Offset-voltage (for example GDR 101)

Currents

I_{I1}	Leakage current at a signal input
$I_{\Phi 1}$	Leakage current at a clock input
I_{DD}	Drain supply current
I_{GG}	Gate supply current
I_Q	Output current, general
I_A	Input current at an address input
I_{ZZ}	Additional supply current for particular cells or stages (for example GDQ 101)

Resistances

R_{OH}	High level output resistance
R_{OL}	Low level output resistance
R_Q	Load resistance at an output
R_I	Input resistance at a signal input
$R_{\Phi 1}$	Input resistance at clock 1 input
$R_{\Phi 2}$	Input resistance at clock 2 input
$R_{\Phi 3}$	Input resistance at clock 3 input
R	Resistance, general
R_A	Input resistance at an address input

Capacitances

C_I	Input capacitance at a signal input
C_Φ	Input capacitance at a clock input

C_Q	Output load capacitance
$C_{\Phi 1}$	Input capacitance at clock 1 input
$C_{\Phi 2}$	Input capacitance at clock 2 input
$C_{\Phi 3}$	Input capacitance at clock 3 input
$C_{\Phi 4}$	Input capacitance at clock 4 input
C	Capacitance, general
C_A	Input capacitance at an address input

Frequencies

f_I	Input frequency
f_Φ	Clock frequency

Power

P	Power dissipation (power consumption)
P_{max}	Maximum power rating
P_T	Total power dissipation

Temperatures

T_A	Ambient Temperature
T_S	Storage Temperature

Timing

t_d	Delay time
t_{pd}	Propagation delay
t_t	Transition time
t_r	Rise time
t_f	Fall time
t_w	Pulse width
t_{wH}	Pulse width at the high level
t_{wL}	Pulse width at the low level
t_{d1HLI}	Overlap of input signal and clock (Φ_1),
t_{d1LHI}	(for example FDN 141 A)
t_{tHLQ}	Transition time HL of the output signal
t_{tLHQ}	Transition time LH of the output signal
t_{dHLQ}	Delay of the HL transition of the output signal
t_{dLHQ}	Delay of the LH transition of the output signal (for example FDN 141 A)
$t_{wH\Phi}$	Pulse width at the H-level of the clock signal
$t_{wL\Phi}$	Pulse width at the L-level of the clock signal
$t_{tHL\Phi}$	HL transition time of the clock signal
$t_{tLH\Phi}$	LH transition time of the clock signal
$t_{dHL\Phi 2}$	Delay of the HL transition of the Φ_2 clock signal
$t_{dLH\Phi 2}$	Delay of the LH transition of the Φ_2 clock signal
$t_{dHL\Phi 3}$	Delay of the HL transition of the Φ_3 clock signal
$t_{dLH\Phi 3}$	Delay of the LH transition of the Φ_3 clock signal
t_{d2HLI}	Delay of the HL transition of the input signal
t_{d2LHI}	Delay of the LH transition of the input signal (for example FDN 141 A)
$t_{wL\Phi}$	Pulse width of the clock signal
$t_{wL\Phi 1}$	Pulse width of the clock 1 signal
$t_{wL\Phi 2}$	Pulse width of the clock 2 signal

$t_{wL\Phi3}$ Pulse width of the clock 3 signal
$t_{wL\Phi4}$ Pulse width of the Clock 4 signal
t_{wCS} Pulse width of the inhibit signal CS
t_{d1A} Advance time of the address signal
t_{d2A} Delay time of address signals
t_{d1S} Address advance time at turn-on of supply voltage
t_{d2S} Address delay time at turn-off of supply voltage
t_{dHL} Advance time of signal R/W
t_{acc} Access time
t_{dLH} Delay time of signal R/W
$t_{wR/W}$ Pulse width of R/W signal
t_{dW} Switching delay R/W to read signal
t_{wW} Pulse width of write signal (for example GDQ 101)
t_{pI} Overlap of write signal relative to R/W (GDQ 101)
t_{wHI} Pulse width of input signal at the H-level
t_{wLI} Pulse width of input signal at the L-level
t_{tHLI} HL transition time of an input signal
t_{tLHI} LH transition time of an input signal
t_{dLH} LH transition delay time
t_{wHQ} Pulse width of an output signal at the H-level

Miscellaneous

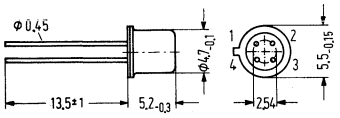
Φ Clock input
Φ_1 Clock 1 input
$\Phi 2$ Clock 2 input
$\Phi 3$ Clock 3 input
$\Phi 4$ Clock 4 input
I Input
$I1$ Input 1
$I2$ Input 2
Q Data output
$\overline{Q}$ Data output inverted
$Q1$ Output 1
$Q2$ Output 2
$Q3$ Output 3
$Q4$ Output 4
$Q5$ Output 5
$Q6$ Output 6
$Q7$ Output 7
$Q8$ Output 8
$Q9$ Output 9
L Low logic level (more negative than H-level)
H High logic level (less negative than L-level)
A1 through A6 Address inputs
B1 through B6 Address inputs
CS Inhibit signal for chip-select
R/W Read/Write signal
M Noise margin

Indices for currents and voltages

Signal input	*I*
Address input	*A, B*
Clock inputs	*Φ*
Output	*Q*
Read/Write signal	*R/W*
Chip-select signal	*CS*
Offset voltage	*OS*
Drain supply	*DD*
Gate supply	*GG*
Substrate supply	*SS*
Cell or stage	*ZZ*

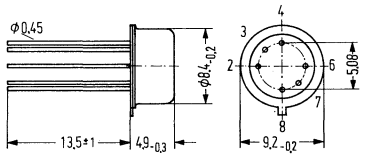
Type 1

Dimensions in mm



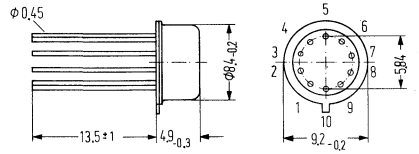
1. 4-pin metal case 18 A 4 DIN 41876 (similar to TO-72).

Type 2



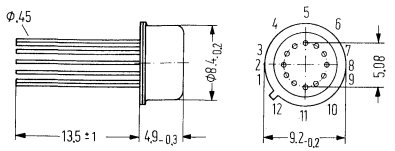
2. 6-pin metal case 5 H 6 DIN 41873 (similar to TO-78).

Type 3



3. 10-pin metal case 5 J 10 DIN 41873 (TO-100).

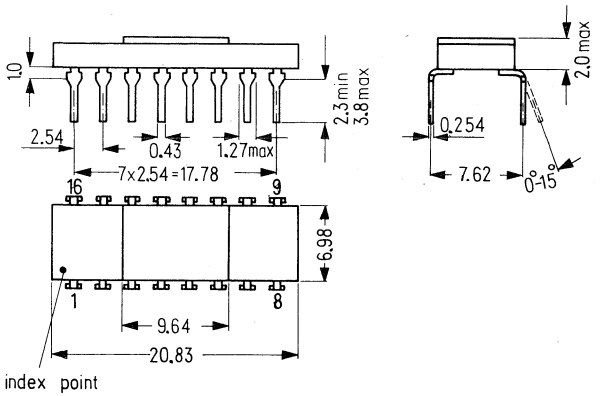
Type 4



Dimensions in mm

4. 12-pin metal case 5 G 12 DIN 41873 (TO-173).

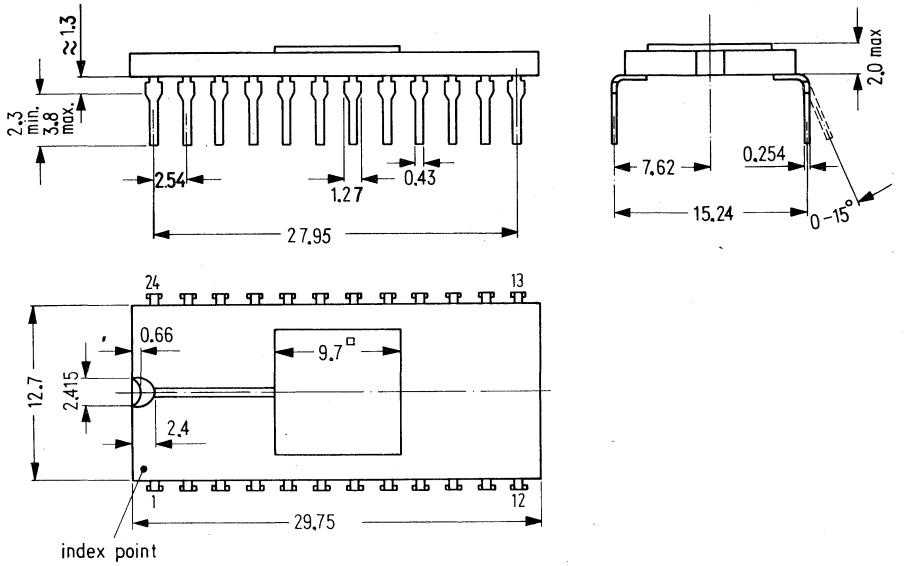
Type 5



5. 16-pin metal-ceramic DIL package (similar to 20 A 16 DIN 41866).

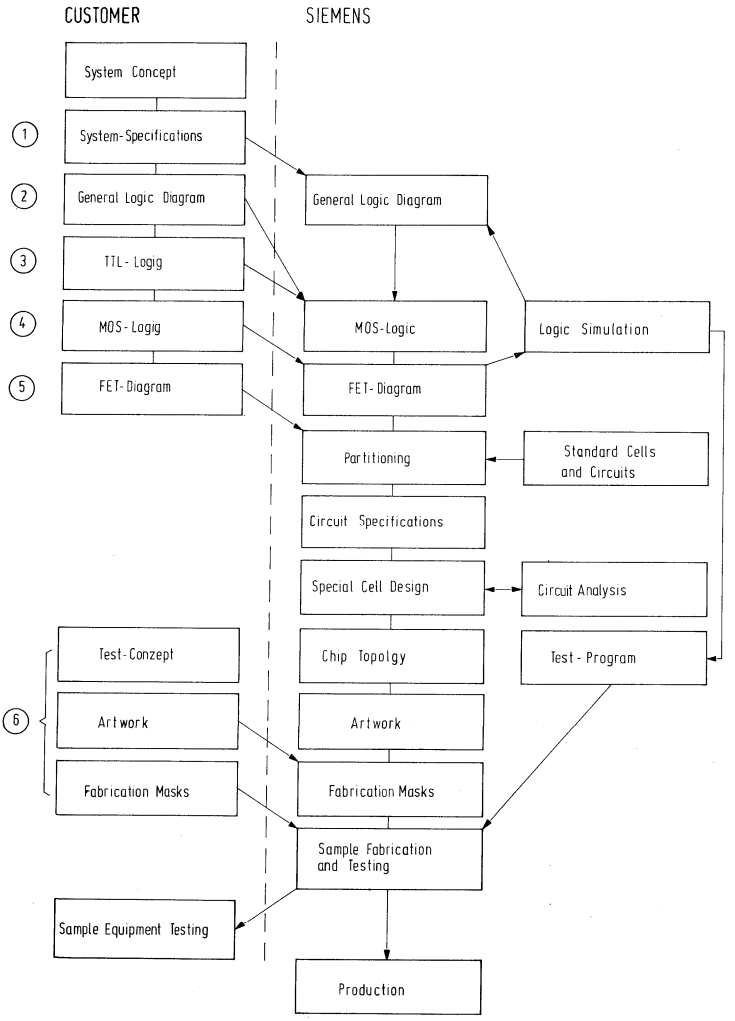
Type 6

Dimensions in mm



6. 24-pin metal-ceramic DIL package (similar to 20 B 24 DIN 41866).

Working Scheme for MOS Custom Development Projects



Ordering Code:
FDN 141A=Q67000–N32

FDN 141 A

Dynamic 256-bit shift register with two clock inputs

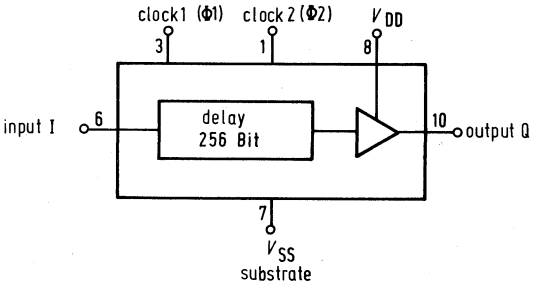
General description

The FDN 141 A is a dynamic 256-bit shift register of the MOS p-channel enhancement type. It is characterized by a high-speed operation capability (up to 3 MHz) and a low power requirement (0.8 mW/bit at 3 MHz).
The low-resistance push-pull output-stage can be used to control MOS-, DTL-, TTL- or other loads directly, with an appropriate voltage supply.
This shift register is also available with guaranteed higher upper frequency ratings.

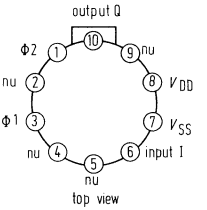
Special features

Bit-length programmable (change of only one mask required)
TTL-compatible
High upper frequency limit (3 MHz)
Low power requirement: Max. 0,03 mW/bit at 10 kHz
max. 0,8 mW/bit at 3 MHz
Variable output voltage, clock-independent NRZ output signal
Protection devices at all inputs and outputs. 256 bit type exchangeable with EA 1204 and pL 5 R256

Block-diagram



Pin-connections



Maximum ratings

		lower limit B	upper limit A	unit
Voltage at all connections (relative to V_{SS}=0 V)	V	–30	+0.3	V
Total power dissipation	P_T		300	mW
Ambient operating temperature	T_A	0	70	°C
Storage temperature	T_S	–55	125	°C

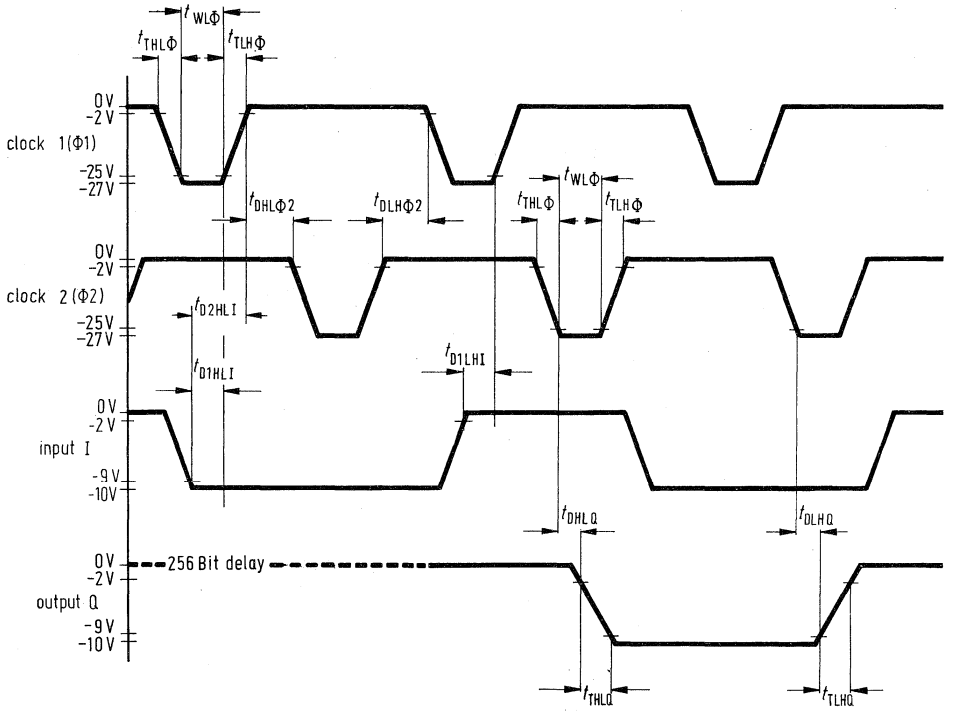
FDN 141 A

Operating characteristics at V_{DD}=–12 V to –14 V, R_Q=1 MΩ, C_Q=20 pf, T_A=0° to 70 °C, unless stated otherwise

		Test conditions	lower limit B	upper limit A	unit
Supply voltage	V_{DD}		–14	–5	V
Power consumption	P_T	f_Φ=2 MHz, V_{DD}=–14 V		170	mW
Signal input					
H-input voltage	V_{IH}		–1.5	+0.3	V
L-input voltage	V_{IL}		–28	–9	V
Input capacitance	C_I	V_I=0 V, f_Φ=1 MHz		3.5	pf
Leakage current	I_{I1}	V_I=–15 V, all other connections 0 V, T_A=25 °C	–1		μA
		V_I=–15 V, all other connections 0 V, T_A=70 °C	–10		μA
Overlap-time	t_{d1HLI}=t_{d1LHI}		10		ns
Noise margin	M		1		V
Signal output					
H-output voltage	V_{OH}		–0,5		V
L-output voltage	V_{OL}		–14	–10	V
H-output resistance	R_{OH}	V_{DD}=–5 V		500	Ω
L-output resistance	R_{OL}	V_{DD}=–5 V		300	Ω
HL-transition time	t_{tHLQ}			100	ns
LH-transition time	t_{tLHQ}			100	ns
Delay time	t_{dHLQ}= t_{dLHQ}			100	ns
Clock-Inputs					
Clock frequency	f_Φ		0.01	3.0	MHz
H-input voltage	$V_{\Phi H}$		–2	+0.3	V
L-input voltage	$V_{\Phi L}$		–28	–26	V
Leakage current	$I_{\Phi I}$	V_Φ=–28 V, all other connections 0 V, T_U=25 °C	–100		μA
Input capacitance					
clock 1 and 2	C_Φ	V_Φ=0 V, f_Φ=1 MHz		85	pf
clock 1 and 2	C_Φ	V_Φ=–26 V, f_Φ=1 MHz		60	pf
Pulse width	$t_{wL\Phi}$		0.125	1.0	μs
HL-transition time	$t_{tHL\Phi}$			100	ns
LH-transition time	$t_{tLH\Phi}$			100	ns
Delay time	$t_{dHL\Phi2}$=$t_{dLH\Phi2}$		0	49	μs
Delay time	t_{d2HLI}=t_{d2HLHI}		t_{d1HLI} +$t_{tLH\Phi}$		ns

The supply current I_{DD} is dependent on the external load; for example, I_{DD}<–1,5 mA for R_Q= 1 MHz, C_Q=50 pf, V_{DD}=–13 V, f_Φ=1 MHz.
The maximum load capacitance is dependent on the maximum power dissipation.

Pulse-diagram



Explanations

$t_{wL\Phi}$ = time interval during which a clock pulse is at the L-level.

$t_{tLH\Phi}$ = time interval during which a clock pulse changes from a –25 V to a –2 V level.

$t_{tHL\Phi}$ = time interval during which a clock pulse changes from a –2 V to a –25 V level.

$t_{dHL\Phi2}=t_{dLH\Phi2}$ = time interval of clock signal measured from the –2 V level of a HL-transition of clock 1 (clock 2, respectively) to the –2 V level of the following LH transition of clock 2 (clock 1, respectively)

$t_{d1HLI}=t_{d1LHI}$ = time interval during which an input signal must be stable before the clock voltage changes from –25 V to –2 V, in order to be transferred into the shift register correctly.

t_{tLHQ} = time interval of the transition of an output signal from –9 V to –2 V.

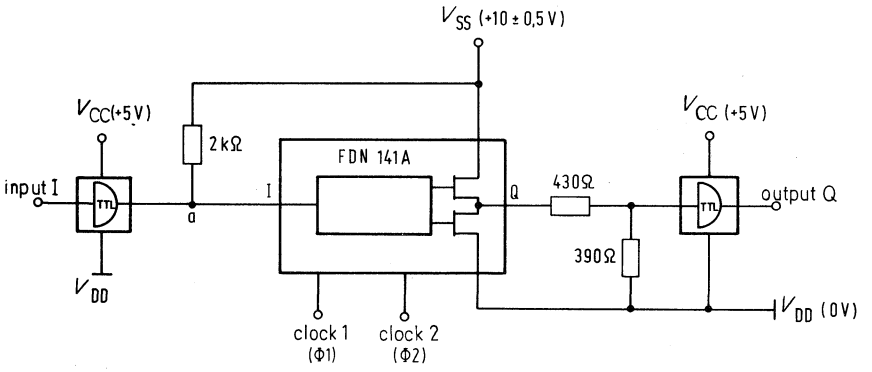
t_{tHLQ} = time interval of the transition of an output signal from –2 V to –9 V.

$t_{dHLQ}=t_{dLHQ}$ = delay time after which an output signal changes due to a clock transition from H to L.

$t_{d2HLI}=t_{d2LHI}$ = Minimum requirement for the sum of propagation delay and signal transition time.

FDN 141 A

Connection to TTL-circuits



The TTL-output (node a) must have been designed for +10 V.

Ordering code:
FDN 151 A: Q67000–N33

FDN 151 A

Dynamic 256-bit shift register with one clock input

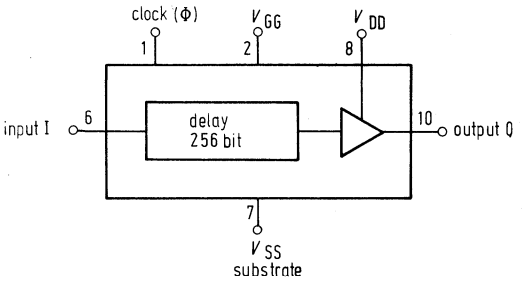
General description

The FDN 151 A is a dynamic 256-bit shift register of the MOS P-channel enhancement type. It is characterized by a low clock input-capacitance (max. 10 pf), a low clock amplitude-requirement (min 9 V), variable and clock-independent output voltages and a low power requirement (max. 0,8 mW/bit at 1 MHz).
The low-resistance push-pull output stage can be used to control MOS-, DTL-, TTL- or other loads directly, with an appropriate voltage supply.
This shift register is also available with guaranteed higher upper frequency ratings.

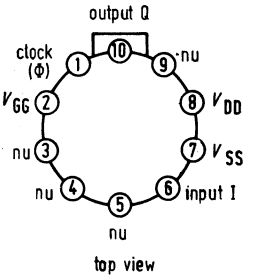
Special features

Bit-length programmable (change of only one mask required)
TTL-compatible
Only one clock input
Very low clock input-capacitance (max. 10 pf)
Low clock amplitude requirement (min. 9 V)
Guaranteed upper frequency rating (1 MHz)
Very low power requirement: Max. 0.25 mW/bit at 10 kHz
max. 0,80 mW/bit at 1 MHz
Variable output voltage, clock independent
NRZ output signal
Protection devices at all inputs and outputs
256 bit type exchangeable with EA 1205 and pL 5 R 256

Block-diagram



Pin-connections



Package type 3

Maximum ratings		lower limit B	upper limit A	unit
Voltage at all connections (relative to V_{ss}=0 V)	V	–30	+0,3	V
Total power dissipation	P_T		300	mW
Ambient operating temperature	T_A	0	70	°C
Storage temperature	T_S	–55	125	°C

FDN 151 A

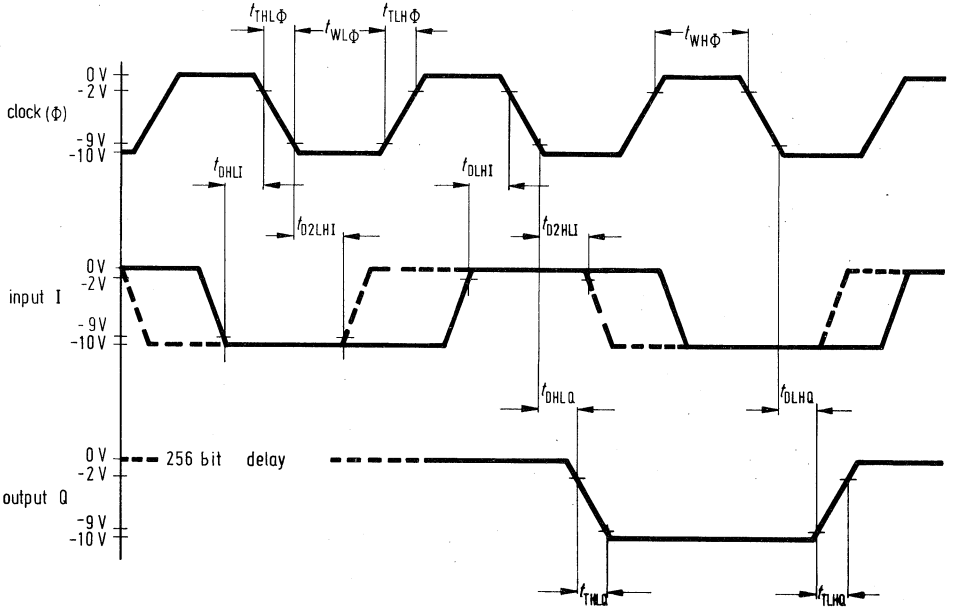
Operating characteristics at V_{DD}=–12 V to –14 V, V_{GG}=–26 V to –28 V, R_Q=1 MΩ, C_Q=20 pf, T_A=0° to 70 °C, unless stated otherwise.

			Test conditions	lower limit B	upper limit A	unit
Supply voltage		V_{DD}		–14	–5	V
		V_{GG}		–28	–26	V
Power consumption		P_T	f_Φ=1 MHz, V_{DD}=–14 V		150	mW
Signal input						
H-input voltage		V_{IH}		–1.5	+0.3	V
L-input voltage		V_{IL}		–28	–9	V
Input capacitance		C_I	V_I=0 V, $f\Phi$=1 MHz		3.5	pf
Leakage current		I_{I1}	V_I=–15 V, all other connections 0 V, T_A=25 °C	–1		μA
Overlap-time	$t_{d1HLI}=t_{d1LHI}$			20		ns
Delay-time	$t_{d2HLI}=t_{d2LHI}$			75		ns
Noise margin		M		1		V
Signal output						
H-output voltage		V_{OH}		–0.5	0	V
L-output voltage		V_{OL}		–14	–10	V
H-output resistance		R_{OH}	V_{DD}=–5 V		500	Ω
L-output resistance		R_{OL}	V_{DD}=–5 V		500	Ω
HL-transition time		t_{tHLQ}			100	ns
LH-transition time		t_{tLHQ}			100	ns
Delay-time	$t_{dHLQ}=t_{dLHQ}$				300	ns
Clock-input						
Clock frequency		f_Φ		0.01	1	MHz
H-input voltage		$V_{\Phi H}$		–2	+0.3	V
L-input voltage		$V_{\Phi L}$		–28	–9	V
Leakage current		$I_{\Phi 1}$	$V_{\Phi L}$=–15 V, all other connections 0 V, T_A=25 °C	–1		μA
		$I_{\Phi 1}$	$V_{\Phi L}$=–28 V, all other connections 0 V, T_A=25 °C	–100		μA
Input capacitance		C_Φ	V_Φ=0 V, f_Φ=1 MHz		3.5	pf
Pulse width		$t_{wL\Phi}$		0.4	50	μs
		$t_{wH\Phi}$		0.4	50	μs
HL-transition time	*)	$t_{tHL\Phi}$			100	ns
LH-transition time		$t_{tLH\Phi}$			100	ns

*) The transition time $t_{tHL\Phi}$ was specified to make sure that in a case of several shift registers being operated from the same clock, the timing of the output signal of one register is compatible with the read-in timing-requirement (t_{d1HLI} and t_{d2LHI}) of the following shift-register. For a single shift-register the signal transfer-times may be longer.

The supply current I_{DD} is dependent on the external load; for example, $I_{DD} < -1{,}5$ mA for R_Q=1 MΩ, C_Q=50 pf, V_{DD}=–13 V, f_Φ=1 MHz.
The maximum load capacitance is dependent on the maximum power dissipation.

Pulse-timing diagram

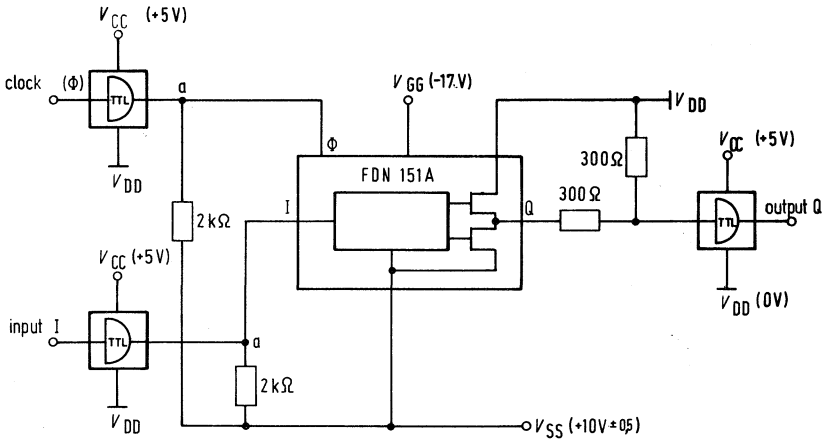


Explanations

$t_{wL\Phi}$ = time interval during which a clock pulse is at the L–level.
$t_{wH\Phi}$ = time interval during which a clock pulse is at the H–level.
$t_{tLH\Phi}$ = time interval during which a clock pulse changes from a –9 V to a –2 V level.
$t_{tHL\Phi}$ = time interval during which a clock pulse changes from a –2 V to a –9 V level.
$t_{d1HLI}=t_{d1LHI}$ = time interval during which an input signal must be stable before the clock voltage rises to –9 V, in order to be transferred into the shift register correctly.
$t_{d2HLI}=t_{d2LHI}$ = time interval during which an input signal must still be stable after the clock signal has risen to –9 V, in order to be transferred into the shift register correctly.
t_{tHLQ} = time interval during which the output signal changes from a –9 V to a –2 V level.
t_{tLHQ} = time interval during which the output signal changes from a –2 V to a –9 V level.
$t_{dHLQ}=t_{dLHQ}$ = delay time after which an output signal changes due to a clock transition from H to L.

FDN 151 A

Connection to TTL-circuits



The TTL-outputs (nodes a) must have been designed for +10 V.

Ordering code
GDJ 156 = Q67000–N23

GDJ 156

Two static 16-bit shift registers

Maximum ratings		lower limit B	upper limit A	unit
Voltage at all connections (relative to V_{SS}=0 V)	V	–30	+0,3	V
Ambient operating temperature	T_A	–55	85	°C
Storage temperature	T_S	–55	150	°C

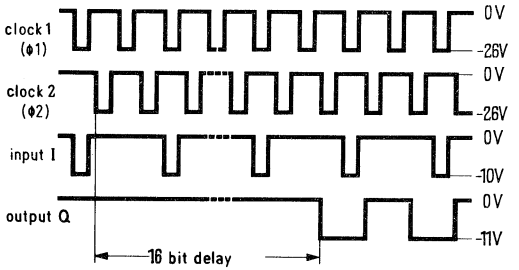
Operating characteristics at V_{DD}=–12 V to –14 V, V_{GG}=–26 V to –28 V, R_O=1 MΩ, C_O=10 pf, T_A=–55 to 85 °C unless stated otherwise

		Test conditions	lower limit B	typ	upper limit A	unit
Supply voltage	V_{DD}		–14		–12	V
	V_{GG}		–28		–26	V
Supply current	I_{DD}		–10			mA
	I_{GG}		–2			mA
Power consumption	P_T				196	mW
Signal input						
H-input voltage	V_{IH}		–2			V
L-input voltage	V_{IL}				–10	V
Input resistance	R_I	V_I=–20 V	20			MΩ
Input capacitance	C_I			3		pf
Noise margin	M		1			V
Pulse width	$t_{wHI}=t_{wLI}$		0,4+ $t_{tLH\Phi}$			
Signal output						
H-output voltage	V_{QH}		–1	–0.5		V
L-output voltage	V_{QL}			–12	–11	V
L-output voltage	V_{QL}	R_Q=27 KΩ		–11	–10	V
L-output voltage	V_{QL}	R_Q=4,7 KΩ			–5	V
Output resistance to substrate	R_{QH}	at H-output load current 0,5 mA			3	KΩ
Clock inputs						
Clock frequency	f_Φ		0		1	MHz
H-input voltage	$V_{\Phi H}$		–2			V
L-input voltage	$V_{\Phi L}$		–28		–26	V
Input resistance clock 1	$R_{\Phi I}$	$V_{\Phi 1}$=–26 V $V_{\Phi 2}$=0 V	2.6			MΩ
Input resistance clock 2	$R_{\Phi 2}$	$V_{\Phi 1}$=0 V $V_{\Phi 2}$=–26 V	2.6			MΩ
Input capacitance clock 1	$C_{\Phi 1}$	$V_{\Phi 1}=V_{\Phi 2}$=0 V		4	6	pf
Input capacitance clock 2	$C_{\Phi 2}$	$V_{\Phi 1}=V_{\Phi 2}$=0 V		4	6	pf
Pulse width clock 1	$t_{wL\Phi 1}$		0.4		10	µs
Pulse width clock 2	$t_{wL\Phi 2}$		0.4			µs
Delay time	$t_{dHL\Phi 2}=t_{dLH\Phi 2}$		0.01		10	µs
HL-transition time	$t_{tHL\Phi}$	10% to 90%			5	µs
LH-transition time	$t_{tLH\Phi}$	10% to 90%			5	µs

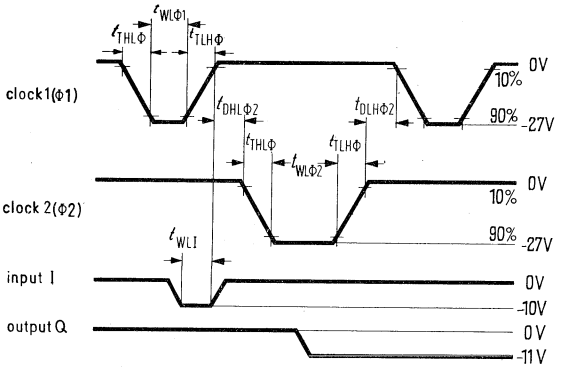
GDJ 156

Not for new developments

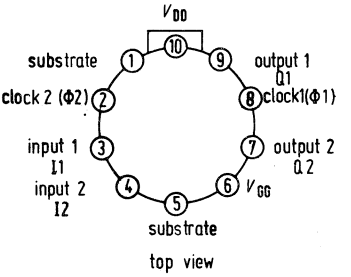
Function pulse-diagram



Pulse-timing diagram



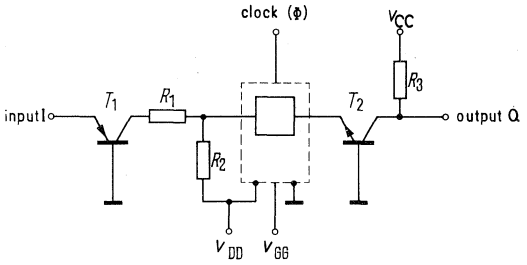
Pin-connections



Package type 3

GDJ 156

Basic diagram of a bufferstage for TTL



This bufferstage processes and delivers positive voltage signals. The resistance values depend on the supply voltages.

When transistor T1 is turned on, the dc-voltage at the junction of R1 and R2 should be from 0 V to –2 V. Resistor R1 protects the shift register against a positive voltage level when T_1, is conducting.

Each bit consists of a cross-coupled flip-flop; this way information can be stored between two clock pulses without a time limit.

For a long-time storage clock 2 must be kept on an L-level at the same time clock 1 on H. For a 1-bit shift, clock 2 must become H and clock 1 an L for the required pulse duration. The pulses of clock 1 and clock 2 must be non-overlapping at the L-level.

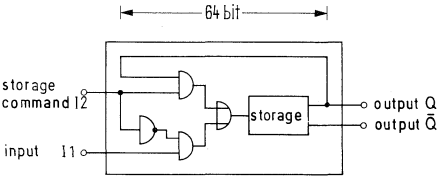
GDN 116 A

Ordering code
GDN 116A=Q67000–N30

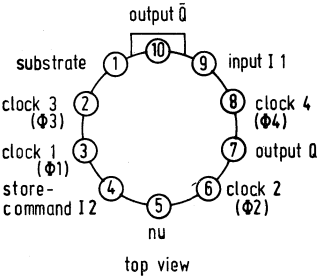
Dynamic 64-bit accumulator

The dynamic 64-bit serial-accumulator (GDN 116A) consists of a 64-bit shift register, together with the logic required to circulate or store information.
The power dissipation for each stage increases in proportion with the frequency.

Blockdiagram



Pin-connections



Package type 3

Not for new developments

Maximum ratings		lower limit B	upper limit A	unit
Voltage at all connections (relative to V_{SS}=0 V)	V	–30	+0,3	V
Ambient operating temperature	T_A	–55	85	°C
Storage temperature	T_S	–55	150	°C

Operating characteristics at R_Q=10 MΩ, C_Q=12 pf, T_A=–55° to 85°C, unless stated otherwise

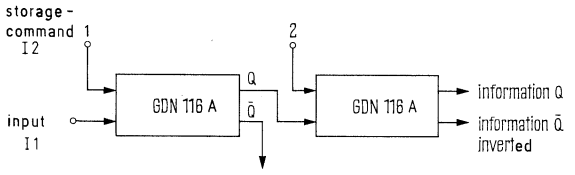
	Test conditions	lower limit B	typ	upper limit A	unit
Information- and storage imput					
H-input voltage	V_{IH}	–2		0	V
L-input voltage	V_{IL}	–24		–10	V
Leakage current	I_{IL} V_I=–20V	–5			μA
Input capacitance	C_{IL}			2	pf
Pulse width, information	t_{wI1}	100			ns
Pulse width, storage command	t_{wI2}	200			ns
Signal outputs	see note				
H-output voltage	V_{QH}	–2		0	V
L-output voltage	V_{QL}	–24		–11	V

		Test conditions	lower limit B	typ	upper limit A	unit
Clock-inputs						
H-input voltage	$V_{\Phi H}$		–1		+0,3	V
L-input voltage	$V_{\Phi L}$		–27		–24	V
Leakage current	$I_{\Phi L}$	V_Φ=–27 V	–100			μA
Input capacitance						
clock 1	$C_{\Phi 1}$				10	pf
clock 2	$C_{\Phi 2}$	plus capacitive load			10	pf
clock 3	$C_{\Phi 3}$				10	pf
clock 4	$C_{\Phi 4}$				10	pf
Clock frequency	f_Φ		0.01		2	MHz
Pulse width clock 1 and 3	$t_{WL\Phi 1}$ $t_{WL\Phi 3}$	at–24 V	100			ns
Pulse width clock 2 and 4	$t_{WL\Phi 2}$ $t_{WL\Phi 4}$		200			ns

Note: A resistive load to sustrate at the output discharges the output level L to H with a time constant t=RC.

Connection diagram

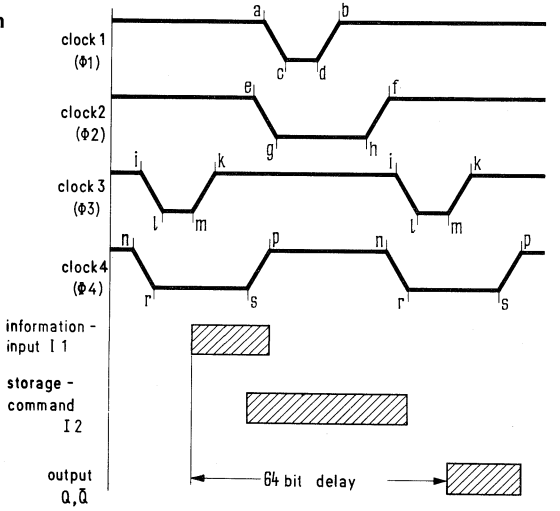
A serial-accumulator may be connected to a second one directly, without the need for additional elements.



GDN 116 A

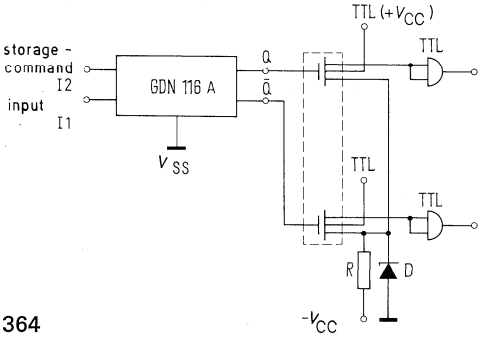
Not for new developments

Pulse-timing diagram

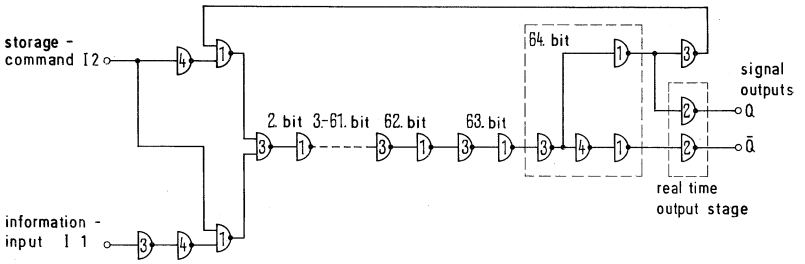


		lower limit B	upper limit A	unit
level read time	t_{bh}	100		ns
level read time	t_{ks}	100		ns
overlap, clock 1–4	t_{pa}	0		ns
overlap, clock 2–3	t_{fi}	0	1000	ns
overlap, clock 2–4	t_{tn}	0		ns
overlap, clock 4–2	t_{pe}	0		ns
charging time, clock 3	t_{rm}	100		ns
charging time, clock 1	t_{gd}	100		ns

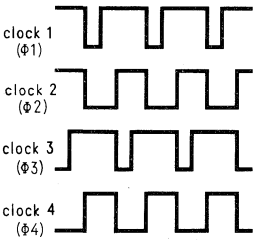
Diagram for buffer stages TTL, DTL etc.

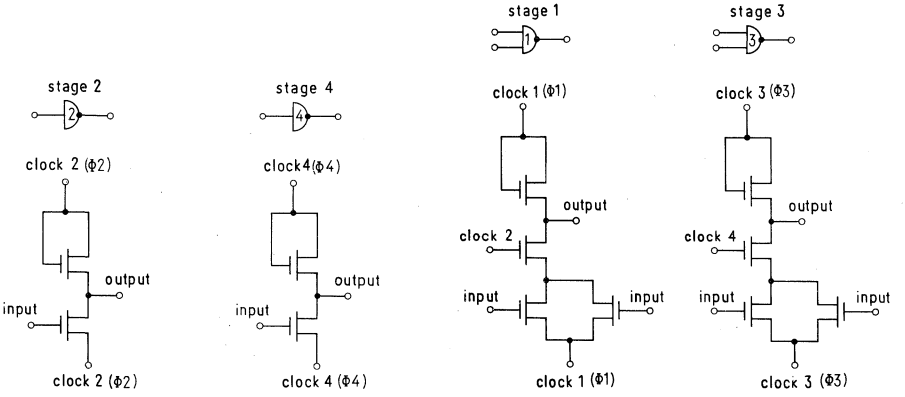


Block-diagram



Clock pulse diagram





Level read time	clock 2	clock 4	clock 2 and 1	clock 4 and 3
Charging time	clock 2	clock 4	clock 1	clock 3

GDQ 101
GDQ 106

Ordering code

GDQ 101 = Q67000–Q13
GDQ 106 = Q67000–Q14

Static 256-bit Read and Write memory (RAM)

Word-organization: 256 words of 1 bit each
Full decoding of an 8–bit address code
Typical access time: 700 ns
Non-destructive read
Directly TTL-compatible
Operating power requirement typ. 1,4 mW/bit, reduceable to 0,4 mW/bit
Simple extention of storage capacity through CS-signal
Protection of data during change of address through CS-signal
Protection against static charges at all connections
16–pin DIL-package

Not for new developments

Maximum ratings		lower limit B	upper limit A	unit
Drain supply voltage	V_{DD}	–15	+0,3	V [1]
Cell supply voltage	V_{ZZ}	–18	+0,3	V [1]
Gate supply voltage	V_{GG}	–30	+0,3	V [1]
Input signal voltage	V_I	–30	+0,3	V [1]
Output currents	I_{QL}	–1,5		mA
	I_{QH}		0,3	mA
Operating temperature range 1	T_A	0	70	°C
range 6	T_A	–40	85	°C
Storage temperature	T_S	–55	125	°C

Note [1]: Voltages relative to V_{SS}

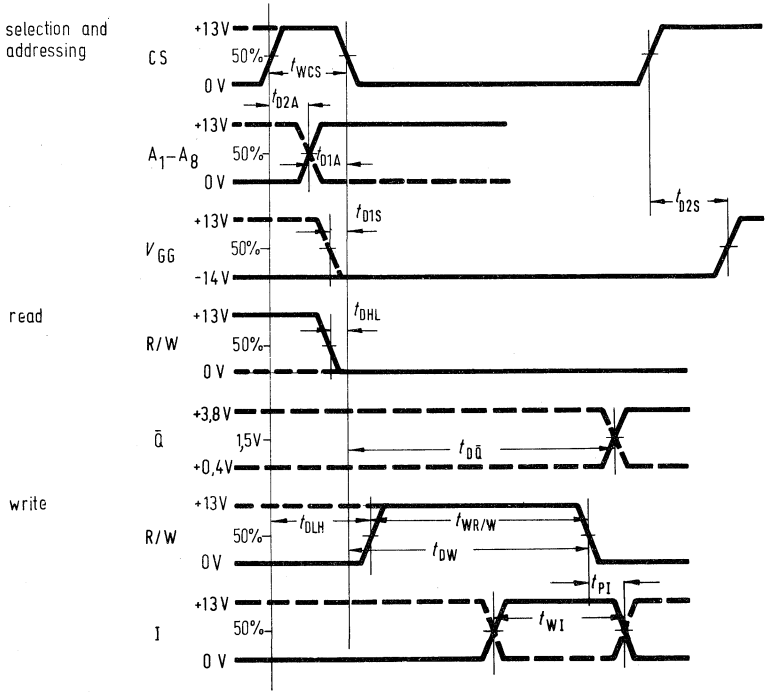
Static operating characteristics		Test conditions	lower limit B	typ	upper limit A	unit
Supply voltage	V_{SS}		+12	+13	+14	V
	V_{DD}			0		V
	V_{ZZ}		–4	–3	–2	V
	V_{GG}		–15	–14	–13	V
Supply current	I_{DD}	V_{SS}=+13 V V_{DD}=0 V		–12		mA
	I_{ZZ}	V_{ZZ}=–3 V		–6		mA
	I_{GG}	V_{GG}=–14 V		–4		mA
H-input voltage	V_{IH}	V_{SS}=+13 V	–17	–0.4	+0.3	V
L-input voltage	V_{IL}		+11	+13	+13.3	V
Reverse current for A_1 though A_8, R/W, CS,	I_{IL}	V_I=–25 V V_A=25°C	–1			μA
H-output voltage	V_{QH}	I_{OH}=0.03 mA		0		V
L-output voltage	V_{QL}	I_{OL}=–0,6 mA		+12,7		V
H-output current	I_{QH}	V_{OH}=+0,4 V		+0.17		mA
L-output current	I_{QL}	V_{OL}=+12 V		–0.6		mA

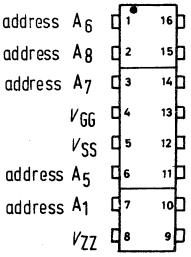
Dynamic operating characteristics at V_{SS}=+13 V, V_{DD}=0 V, V_{ZZ}=–3 V, V_{GG}=–14 V, C_A=15 pf, T_A=25°C

Operation	caracteristic tested		lower limit B	typ	upper limit A	unit
Selection and addressing	Width of inhibit signal CS	t_{WCS}	200			ns
	Advance time of addresses A_1–A_8	t_{d1A}	50			ns
	Delay time of addresses A_1–A_8	t_{d2A}	50			ns
	Advance time at turn-on of supply voltage V_{GG}	t_{d1S}	50			ns
	Delay time at turn-off of supply voltage V_{GG}	t_{d2S}	150			ns
Read	Advance time of signal R/W	t_{dHL}	50			ns
	Access time relative to CS	$t_{d\Phi}$		700	10000	ns
Write	Delay of signal R/W when writing	t_{dLH}	200			ns
	width of R/W signal	$t_{WR/W}$	200			ns
	Switching of R/W signal to read	t_{dW}	500			ns
	Write-time	t_{wI}	200			ns
	Overlap of information relative to R/W	t_{pI}	150			ns
	LH and HL transition times of the input signals	t_{tHLI}		20		ns
		$=t_{tLHI}$		20		ns

Not for new developments

Pulse timing diagram



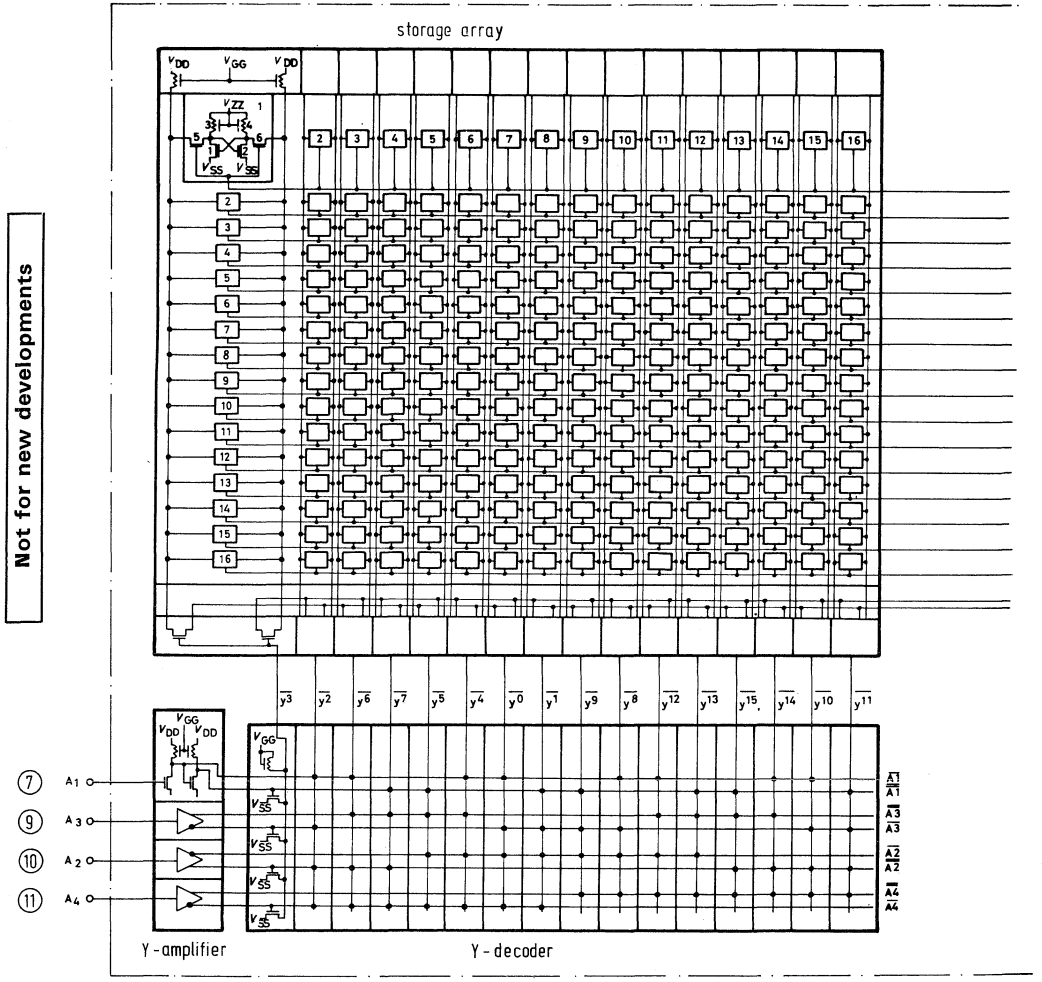


Pin connections
Top view
Package type 5

GDQ 101
GDQ 106

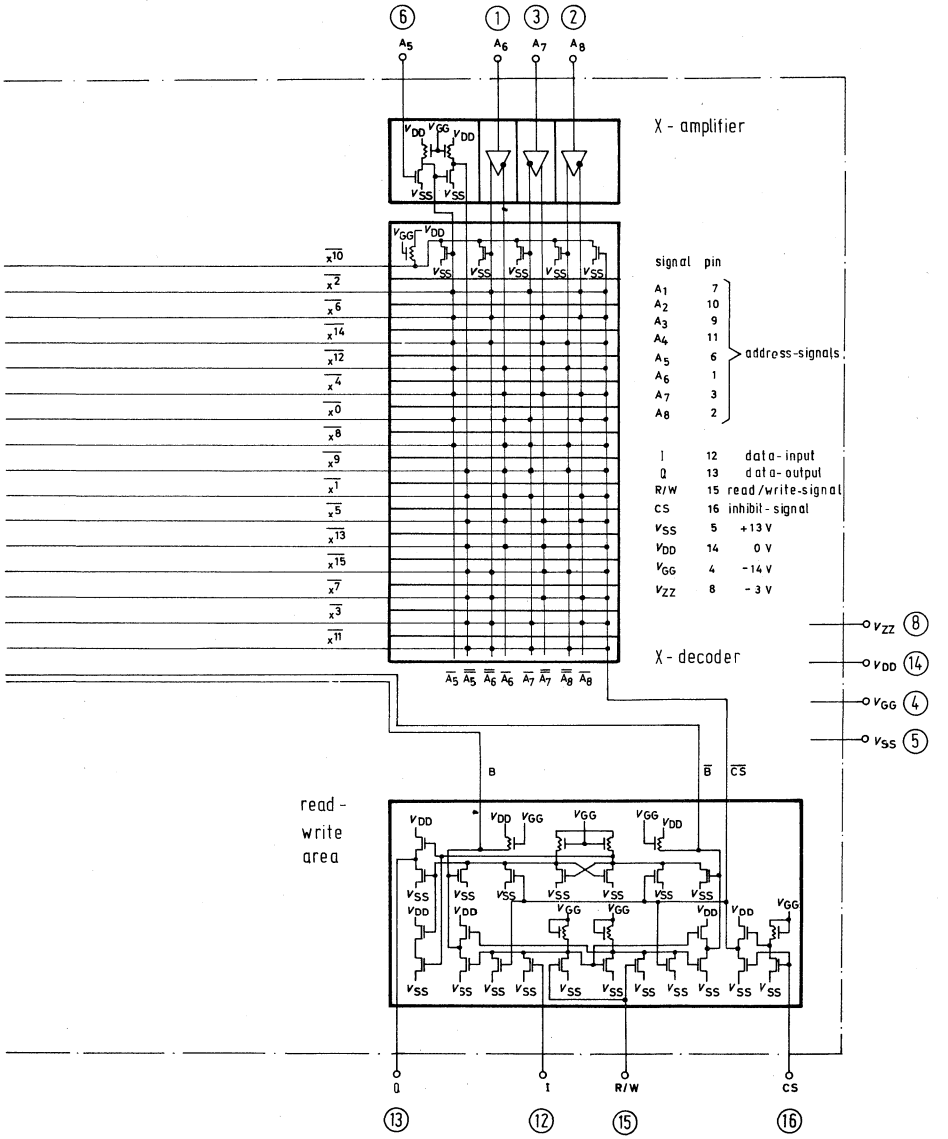
Not for new developments

Storage array with decoder



Note: $U_{DD}=V_{DD}$
$U_{GG}=V_{GG}$
$U_{ZZ}=V_{ZZ}$
$U_{SS}=V_{SS}$

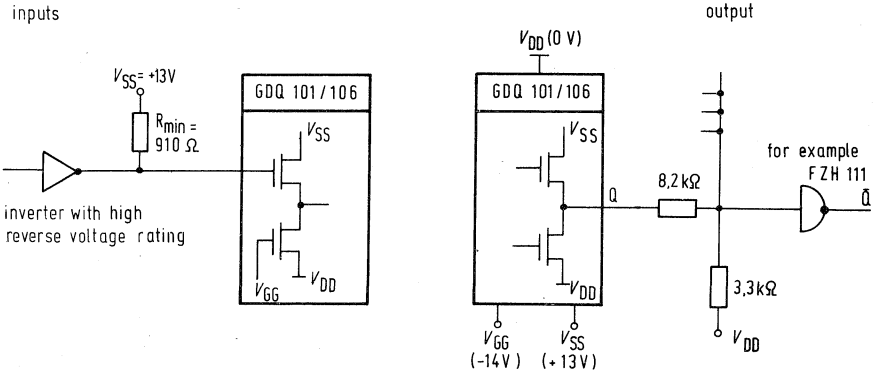
GDQ 101
GDQ 106



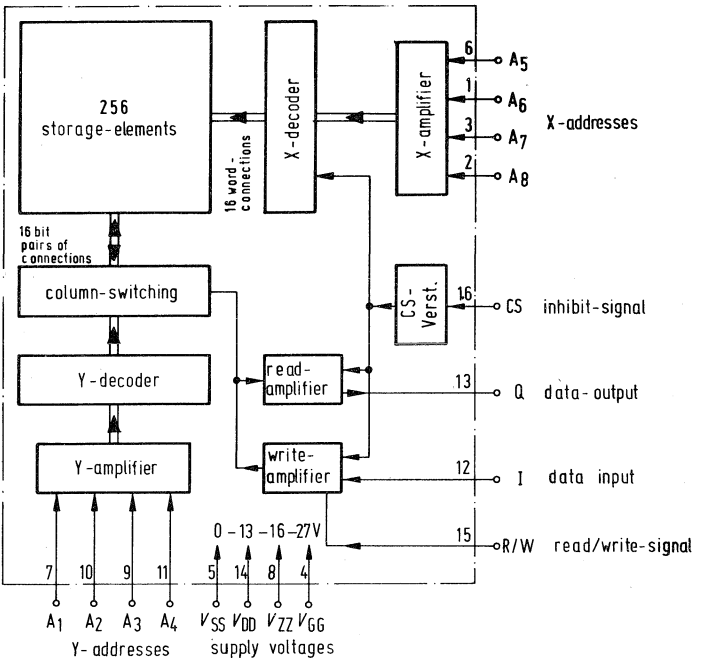
GDQ 101
GDQ 106

Not for new developments

Connection to TTL-circuits



Block-diagram



Ordering codes

GDR 101 = Q67000–Q15
GDR 106 = Q67000–N27

GDR 101
GDR 106

Read-Only-Memories (ROMs)

The ROMs of types GDR 101/106 are highly integrated monolithic silicon circuits of the p-channel, enhancement field effect transistor type.

Short cycle times and a low power requirement result from the application of a dynamic four-phase technique, which employs two external clock signals and works in both a synchronous and asynchronous fashion.

A specifically fabricated mask defines the data-contents stored; this way the highest degree of flexibility with respect to word-organization is made possible.

Standard storage capacities: 2048 bit
2240 bit
2304 bit

Special features

Cycle time 800 ns
Power requirement 150 mW
Protection devices at all inputs and outputs
TTL compatible (output buffer)
Wired-AND application
Operating temperature –40° to + 85°C (GDR 106)
24–pin DIL metal-ceramic package

Applications

Pattern-generator: 7-segment decoder
16-segment decoder
Code converter: Selectric/ASCII-code converter
Function-tables: Sine-, cosine-generators
Micro-programs
Arithmetic operations
Logic functions
Multipurpose applications

Type-spectrum of data organization

The design of this type of ROMs permits the following organizations:

GDR 101
GDR 106

Type-spectrum

Type designation	Capacity (bit)	Words	Bit/word	Parallel outputs (bit)	Address-or chip-select connections	Programming
GDR 101-1100	2048	2048	1	1	0	(according to choice)
GDR 101-1200		1024	2	2	1	
GDR 101-1400		512	4	4	2	
GDR 101-1800		256	8	8	3	
GDR 101-1130		2×512	1+3	1+3	1	
GDR 101-1170		2×256	1+7	1+7	2	
GDR 101-1260		2×256	2+6	2+6	2	
GDR 101-1350		2×256	3+5	3+5	2	
GDR 101-2700	2240	64	35	7	5 row-select connections or 3 bit row decoding	(according to choice)
GDR 101-2701	2240	64	35	5	(as above)	Dot-pattern generator for vertical scanning, ASCII-code
GDR 101-2500	2240	64	35	5	3 bit line-decoding	(according to choice)
GDR 101-2501	2240	64	35	5	(as above)	Dot-pattern generator for horizontal scanning (TV), ASCII-code
GDR 101-390X	2304	256	9	9	2	(according to choice)
GDR 101-3180		2×256	1+8	1+8	1	
GDR 101-3270		2×256	2+7	2+7	1	
GDR 101-3900	2304	**Multipurpose-ROM** 2 Starbust-generators, 7-segment decoder, selectric/ASCII code converter				

Package: Type 6

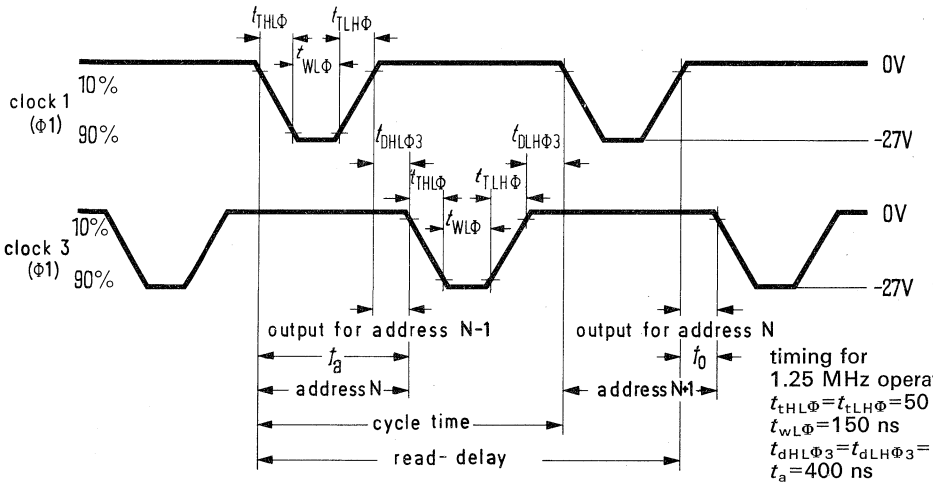
Maximum ratings		lower limit B	upper limit A	unit
Supply voltage	V_{DD}	–30	+0,3	V
clock voltage	V_{Φ}	–30	+0,3	V
Ambient operating temperature (range 1)	T_A	0	70	°C
(range 6)	T_A	–40	85	°C
Storage temperature	T_S	–55	150	°C

Operating characteristics at V_{DD}=–12 V to –28 V, R_Q=20 KΩ, C_Q=10 pf, T_A=–55°C to 85°C, unless stated otherwise.

		Test conditions	lower limit B	typ	upper limit A	unit
Clock inputs						
H-input voltage	$V_{\Phi H}$		–2		+0,3	V
L-input voltage	$V_{\Phi L}$		–28		–24	V
Input resistance, clock 1	$R_{\Phi 1}$		2,6			MΩ
Input resistance, clock 3	$R_{\Phi 3}$		2,6			MΩ
Input capacitance, clock 1	$C_{\Phi 1}$	$V_{\Phi 1}$=–26 V, $V_{\Phi 3}$=0 V		100		pf
input capacitance, clock 3	$C_{\Phi 3}$	$V_{\Phi 1}$=0 V, $V_{\Phi 3}$=–26 V		40		pf
Clock frequency	f_{Φ}		0.01		1.25	MHz
Pulse width, clock 1 and clock 3	$t_{wL\Phi}$		150			ns
Delay time	$t_{dHL\Phi 3}$ = $t_{aLH\Phi 3}$		150			ns
LH-transition time	$t_{tLH\Phi}$	10% to 90%		75	1000	ns
HL-transition time	$t_{tHL\Phi}$					
Parallel address inputs						
H-input voltage	V_{AH}		–2		+0.3	V
L-input voltage	V_{AL}		–24		–12	V
Input resistance	R_A	V_A=–20 V	20			MΩ
Input capacitance	C_A				5	pf
Information output						
output resistance to substrate	R_{QH}	at H-level, load current 2.5 mA			1	kΩ
	R_{QL}	at L-level, V_Q=–20 V		2		MΩ
Load current	I_Q		–3			mA
Read delay			1			μs
Power consumption						
9 outputs	P			120		mW
8 outputs	P			120		mW
4 outputs	P			130		mW
2 outputs	P			135		mW
1 output	P			140		mW
Supply current	I_{DD}		–3			mA

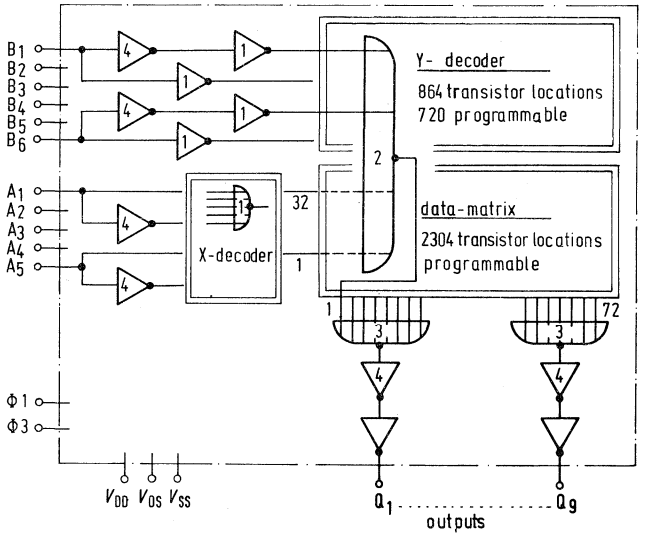
GDR 101
GDR 106

Pulse timing diagram



timing for
1.25 MHz operation
$t_{tHL\Phi}=t_{tLH\Phi}=50$ ns
$t_{wL\Phi}=150$ ns
$t_{dHL\Phi3}=t_{dLH\Phi3}=150$ ns
$t_a=400$ ns
cycle time=800 ns
read delay=1 μs
read only
during to addresses stable
during t_a

Block diagram



	1	2	3	4
preparation	Φ_1	Φ_1	Φ_3	Φ_3
read	$\overline{\Phi_1}$	Φ_3	$\overline{\Phi_3}$	Φ_1

Ordering of a custom ROM-program

1. General information

Customer: Company name and address
Project engineer:
Phone
Telex

Word organization

Type	Words	Bit/word	Chip-selection
GDR 106-1100	2048	1	B_1 B_2 B_3
106-1200	1024	2	□
106-1400	512	4	□□
106-1800	256	8	□□□

Outputs

Type [1]	Words	Bit No. 1 2 3 4 5 6 7 8
GDR 106-1100	□ 2048	Pin No. 3
	□ 0 to 255	Pin No. 3
	255 to 511	4
	etc.	:
		10
106-1200	□ 1024	Pin No. 3 7
	□ 0 to 255	Pin No. 3 7
	256 to 511	Pin No. 4 8
	etc.	5 9
		6 10
106-1400	□ 512	Pin No. 3 5 7 9
	□ 0 to 255	Pin No. 3 5 7 9
	256 to 511	Pin No. 4 6 8 10
106-1800	□ 256	Pin No. 3 4 5 6 7 8 9 10

[1]) Mark type selected
[2]) State logic conditions for chip-selection:
"I"=V_{SS}–12 V to V_{SS}–28 V
"0"=V_{SS}+0,3 V to V_{SS}–2,0 V.

2. Data formats

The custom-data may be supplied in several formats:
2.1 Print or typewriting
2.2 Punched tape
2.3 Topographic datapattern
2.4 Other formats agreed to by the customer and manufacturer
In the following, "I" at an output means a high resistance and a high negative voltage relative to V_{SS}; accordingly, "O" means a low resistance and a low negative voltage (<–2.0 V) relative to V_{SS}.

2.1 Print or typewriting

A datalist prepared in this form should contain the word-address as a decimal number in the first column, followed by the data as shown below:

Type GDR 106-1100, 2048×1

	Bit No. 1
0	0
1	0
2	1
:	:
:	:
2047	0

Type GDR 106-1200, 1024×2

	Bit No. 1	2
0	0	0
1	1	0
2	1	0
:	:	:
1023	0	1

Type GDR 106-1400, 512×4

	Bit No. 1	2	3	4
0	0	1	0	0
1	1	1	0	0
2	0	1	1	1
:	:	:	:	:
511	0	0	0	1

Type GDR 106-1800, 256×8

	Bit No. 1	2	3	4	5	6	7	8
0	0	1	1	0	0	0	1	1
1	1	1	0	0	1	1	0	0
2	1	0	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:
255	0	0	1	0	0	0	1	1

2.2 Punched tape

The data may be supplied on an 8-track punched tape in ASCII-code.
The following format is preferred:
1. 256 lines of 8 databits per line
2. These lines have been numbered from 000 through 255
3. Each 3-digit line number is followed by a space, the 8 databits, "carriage return" (CR), "line feed" (LF) and "rubout" (RO) in this sequence.
4. A bell-signal (code 207) follows the last CR-LF-RO sequence.

The meaning of this arrangement for various wordorganizations is demonstrated by the following examples (fig. 1).

2.3. Topographic datapattern

This pattern (fig. 2) designates the programmable portions of the ROM, i.e. the y-decoder and the data-matrix. In this form, complex word-organizations can be defined.

2.4. Other data-formats may be negotiated by the customer and manufacturer.

Fig. 1. Data-formats on punched tape in ASCII-code

GDR 106-1100, 2048 words of 1 bit each

```
        00001111  A3
        00110011  A4
        01010101  A5
        ||||||||
        Bit No.
        ||||||||
Line    ||||||||
 ↓      11111111
```

		B_1	B_2	B_3	B_4	B_5	B_6	A_1	A_2
000	01101101	0	0	0	0	0	0	0	0
001	11000111	0	0	0	0	0	0	0	1
002	00111011	0	0	0	0	0	0	1	0
⋮	⋮					⋮			
255	10001100	1	1	1	1	1	1	1	1

GDR 106-1200, 1024 words of 2 bit each

```
        0 0 1 1  A4
        0 1 0 1  A5
        | | | |
Line    | | | |
 ↓      Bit No.
 ↓      | | | |
 ↓      12121212
```

		B_2	B_3	B_4	B_5	B_6	A_1	A_2	A_3
000	01100111	0	0	0	0	0	0	0	0
001	11000101	0	0	0	0	0	0	0	1
⋮	⋮				⋮				
255	00100111	1	1	1	1	1	1	1	1

GDR 101
GDR 106

GDR 106-1400, 512 words of 4 bit each

Line	Bit No. 12341234	B_3	B_4	B_5	B_6	A_1	A_2	A_3	A_4
000	11000110	0	0	0	0	0	0	0	0
001	00010011	0	0	0	0	0	0	0	1
⋮	⋮					⋮			
255	00100111	1	1	1	1	1	1	1	1

GDR 106-1800, 256 words of 8 bit each

Line	Bit No. 12345678	B_4	B_5	B_6	A_1	A_2	A_3	A_4	A_5
000	11000111	0	0	0	0	0	0	0	0
001	00110001	0	0	0	0	0	0	0	1
255	10001100	1	1	1	1	1	1	1	1

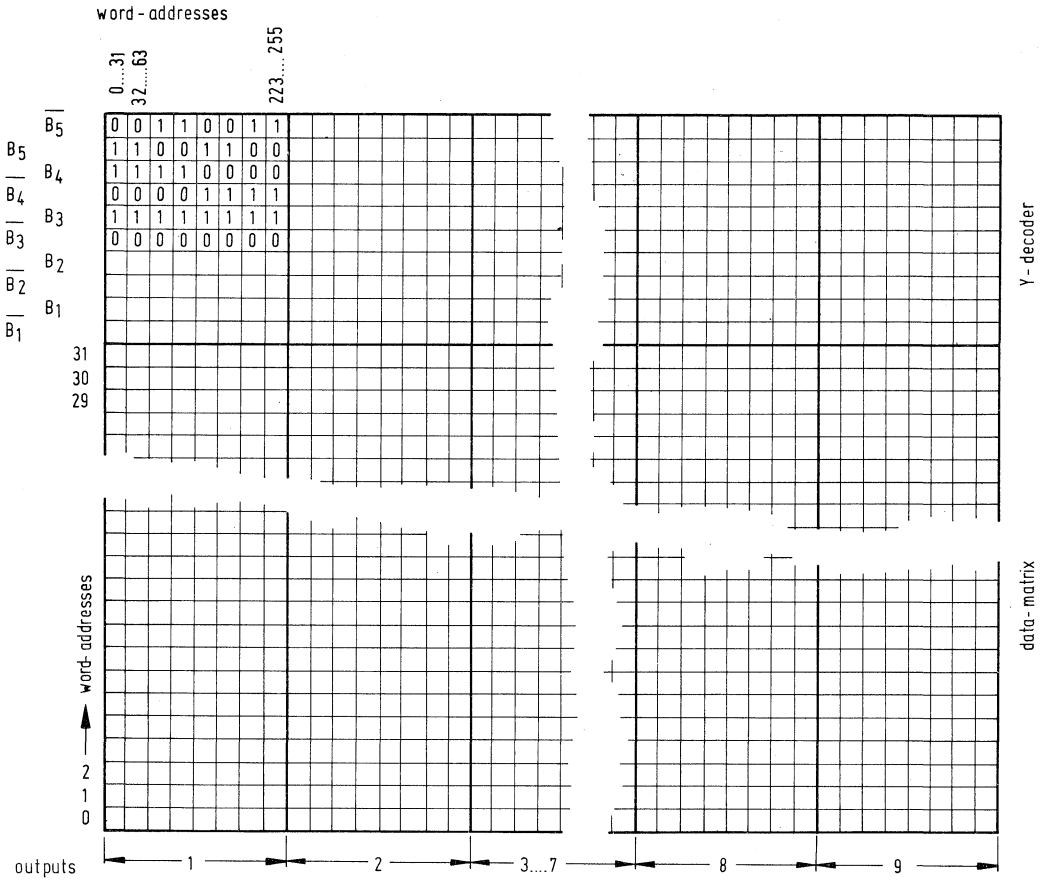


Fig. 2. Topographic data-format, ROM capacity 2304 bit.

GDR 101
GDR 106

Pin No.	Type-No. 1100	1200	1400	1800	1130	1170	1260	1350	2700	2500	3900	3180	3270
1	B_1	CS	CS_1	CS_1	CS	CS_1	CS_1	CS_1	A_5	CS	V_{DD}	V_{DD}	V_{DD}
2	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q_1	P_1	P_1
3	Q_1	Q_1	Q_1	Q_1	P_1	P_1	P_1	P_1	Q_1	Q_1	Q_1	Q_1	P_2
4	–	–	–	Q_2	–	Q_1	P_2	P_2	Q_2	Q_2	Q_3	Q_2	Q_1
5	–	–	Q_2	Q_3	Q_1	Q_2	Q_1	P_3	Q_3	Q_3	Q_4	Q_3	Q_2
6	–	–	–	Q_4	–	Q_3	Q_2	Q_1	Q_4	Q_4	Q_5	Q_4	Q_3
7	–	Q_2	Q_3	Q_5	Q_2	Q_4	Q_3	Q_2	Q_5	Q_5	Q_6	Q_5	Q_4
8	–	–	–	Q_6	–	Q_5	Q_4	Q_3	Q_6	–	Q_7	Q_6	Q_5
9	–	–	Q_4	Q_7	Q_3	Q_6	Q_5	Q_4	Q_7	–	Q_8	Q_7	Q_6
10	–	–	–	Q_8	–	Q_7	Q_6	Q_5	–	–	Q_9	Q_8	Q_7
11	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}	V_{OS}
12	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1	Φ_1
13	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
14	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3	Φ_3
15	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	I_5	I_5	A_1	A_1	A_1
16	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	I_4	I_4	A_2	A_2	A_2
17	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	I_3	I_3	A_3	A_3	A_3
18	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	I_2	I_2	A_4	A_4	A_4
19	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	I_1	I_1	A_5	A_5	A_5
20	B_6	B_6	B_6	B_6	B_6	B_6	B_6	B_6	I_6	I_6	B_6	B_6	B_6
21	B_5	B_5	B_5	B_5	B_5	B_5	B_5	B_5	A_1	A_1	B_5	B_5	B_5
22	B_4	B_4	B_4	B_4	B_4	B_4	B_4	B_4	A_2	A_2	B_4	B_4	B_4
23	B_3	B_3	B_3	CS_3	B_3	B_3	B_3	B_3	A_3	A_3	CS_1	B_3	B_3
24	B_2	B_2	CS_2	CS_2	B_2	CS_2	CS_2	CS_2	A_4	I_7	CS_2	CS	CS

(V_{OS}) = Offset-Spannung
CS = Chip-Select

Complete program-pattern of type GDR 101-3900

	Address inputs								ROM-program																							
									00 outputs								01 outputs								10 outputs								11 outputs							
	B_3	B_4	B_5	A_1	A_2	A_3	A_4	A_5	9	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
33	1	0	X	X	0	0	0	0	1	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
34	1	0	X	X	0	0	0	1	1	0	1	1	0	1	1	1	0	1	0	0	0	0	1	0	0	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	1	0	1
35	1	0	X	X	0	0	1	0	1	1	0	0	1	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1	1	1	1	0	0	1	1	1	0	1	1	1	0
36	1	0	X	X	0	0	1	1	0	1	1	0	1	1	1	1	0	0	1	1	1	0	1	0	0	1	0	1	1	0	0	1	1	0	1	1	0	1	1	1	1	0	1	0
37	1	0	X	X	0	1	0	0	1	1	1	0	1	1	0	1	0	1	0	1	0	1	1	0	0	1	0	0	1	0	0	1	1	1	0	1	0	1	0	0	1	1	0	1
38	1	0	X	X	0	1	0	1	0	1	0	0	1	1	1	0	1	1	1	1	0	0	1	0	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	1	1	1	1	0
39	1	0	X	X	0	1	1	0	0	0	0	1	1	1	0	1	0	0	1	1	0	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	1	0	1	0	1	1	1	0
40	1	0	X	X	0	1	1	1	1	0	0	0	0	1	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1	0	1	0	1	0	0	0	1	1	1	0	1
41	1	0	X	X	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0
42	1	0	X	X	1	0	0	1	0	1	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	1
43	1	0	X	X	1	0	1	0	1	1	1	0	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	1	1	1	0	0
44	1	0	X	X	1	0	1	1	0	1	1	1	1	1	0	0	0	0	1	0	1	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	1	1	0	1	0
45	1	0	X	X	1	1	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	1	0	0	1	1	0	1	1	1	0	1	0	0	0	1	0	1	1	1	0
46	1	0	X	X	1	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0	1	1	1	0	1	0	1	0	1	0	0	1	1	1	1	1	1	0	1	0	0	1	0
47	1	0	X	X	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1	1	1	0	1	0	1	1	1	0	0	0	1	0	0	0	1	1	1	0
48	1	0	X	X	1	1	1	1	0	1	1	1	0	1	1	0	0	1	1	1	0	1	1	1	0	1	0	1	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0	1	0
49	1	1	X	X	0	0	0	0	1	1	0	1	1	0	1	1	0	0	1	0	1	1	0	1	0	1	0	0	0	1	1	0	1	1	0	0	0	1	0	1	0	1	1	0	0
50	1	1	X	X	0	0	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	1	1	0	0	0	1	0	1	0	1	0	1	0	0	1	1	0
51	1	1	X	X	0	0	1	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1	0	0	1	0
52	1	1	X	X	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1	1	1	0	1	0	0	1	0	1	1	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	1
53	1	1	X	X	0	1	0	0	0	1	1	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	0	1	0	1	0	0	1	1	0
54	1	1	X	X	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1	0	0	0	1	0	0	1	0	1	0	1	1	1	1	0	0	1	0	0	0	0	1	0	1	0	1
55	1	1	X	X	0	1	1	0	0	1	0	1	0	1	0	1	0	0	1	1	1	1	1	1	0	1	0	1	1	0	0	0	0	1	1	0	1	1	0	0	0	1	0	1	0
56	1	1	X	X	0	1	1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	1	0	0	0	1	1	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0
57	1	1	X	X	1	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0
58	1	1	X	X	1	0	0	1	1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	1	1	0	1	1	1	1	1	1	0	0	1	1	0	1	0	1	1	0	0	0	0
59	1	1	X	X	1	0	1	0	1	1	1	1	1	1	0	0	0	1	1	1	0	1	0	0	0	1	1	1	0	0	1	1	0	1	0	1	0	1	0	0	1	1	0	0	1
60	1	1	X	X	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	0	0	1	0	0
61	1	1	X	X	1	1	0	0	0	0	1	0	0	1	0	0	1	1	0	0	1	0	1	0	1	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	1	0	1	0	1
62	1	1	X	X	1	1	1	0	1	1	1	0	0	1	1	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0
63	1	1	X	X	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	1	0	1	0	1	1	0	0	0	1	0	1	0	1
64	1	1	X	X	1	1	1	1	0	0	0	1	0	0	0	1	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1

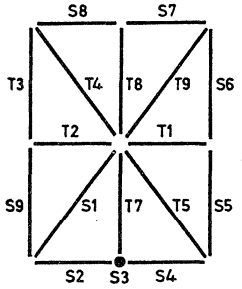
Complete program-pattern of type GDR 101-3900 (continued)

	Address inputs								ROM-program																							
									00 outputs								01 outputs								10 outputs							
	B_3	B_4	B_5	A_1	A_2	A_3	A_4	A_5	9	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
1	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1
2	0	0	X	X	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	0	1	0
3	0	0	X	X	0	0	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0
4	0	0	X	X	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
5	0	0	X	X	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	1	0	1	0
6	0	0	X	X	0	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	1	0	0
7	0	0	X	X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	0	0	1	1	0	0	0	1	1	1	0	1	1	0	1	0
8	0	0	X	X	0	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
9	0	0	X	X	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	X	X	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	1	0
11	0	0	X	X	1	0	1	0	0	1	0	0	1	1	0	0	1	1	1	1	0	0	0	1	1	1	0	1	1	0	1	1	0	1	0
12	0	0	X	X	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0
13	0	0	X	X	1	1	0	0	0	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0
14	0	0	X	X	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0
15	0	0	X	X	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0
16	0	0	X	X	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0
17	0	1	X	X	0	0	0	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0
18	0	1	X	X	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1
19	0	1	X	X	0	0	1	0	0	1	1	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
20	0	1	X	X	0	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
21	0	1	X	X	0	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	0	1	1	0	1	1	1	1	0	0	0	0	0
22	0	1	X	X	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1
23	0	1	X	X	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1
24	0	1	X	X	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0
25	0	1	X	X	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	1	0
26	0	1	X	X	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
27	0	1	X	X	1	0	1	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1	1	0	1	0
28	0	1	X	X	1	0	1	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0
29	0	1	X	X	1	1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	0
30	0	1	X	X	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	0
31	0	1	X	X	1	1	1	0	1	1	1	0	1	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	1	0	0
32	0	1	X	X	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0

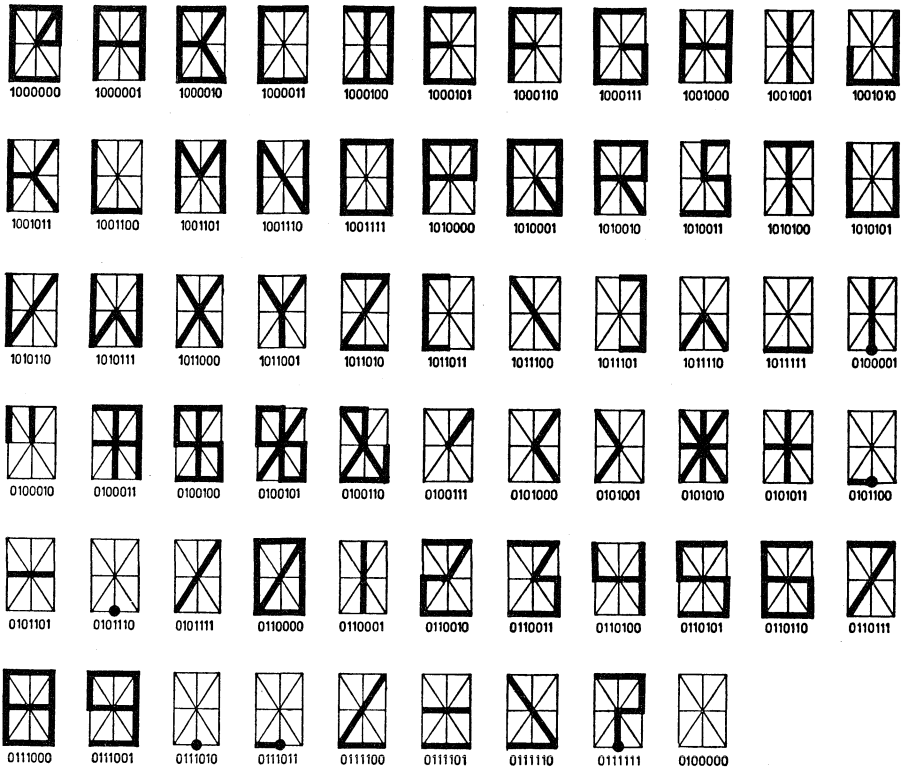
Explanation of the program-pattern of type GDR 101-3900

1. Sub-program: 16-segment character generator. 17 Control signals are required for the display of a 16-segment character including decimal point. For 64 characters, 128 words are required. The complete sub-program for each character must be stored in two bit-words, because this ROM has only 9 outputs.

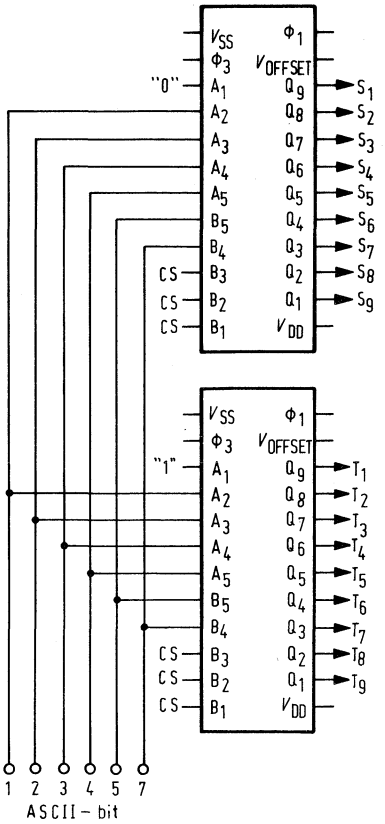
The following figure shows the segments of those characters which are controlled by the first (S) and the second (T) word. Bit T_5 is not used, word T comprises 8 and word S 9 control signals.



1. Sub-program: Display of the 16-segment characters



Block-diagram regarding 16-segment decoder

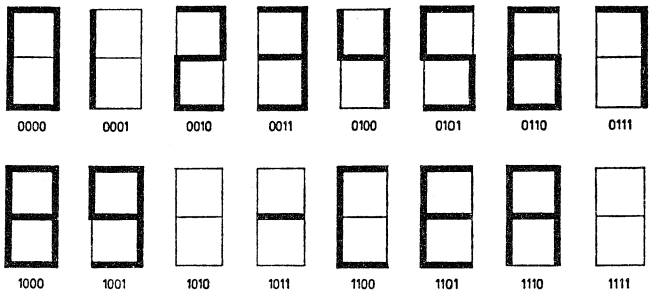


Connection B_3 must be put on "0".

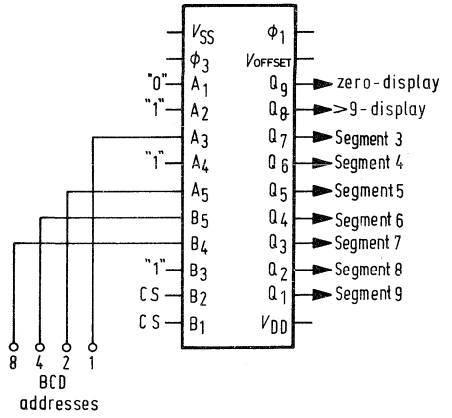
2. Sub-program: Seven segment display

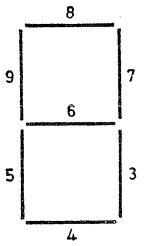
This program of the ROM GDR 101–3900 generates seven control signals, besides a signal for the display of a zero and a carry-signal, for a 7-segment character display. The input code is a type of quasi – BCD code.

Patterns of the 7-segment display with the respective code words



Control signal connections for the segments

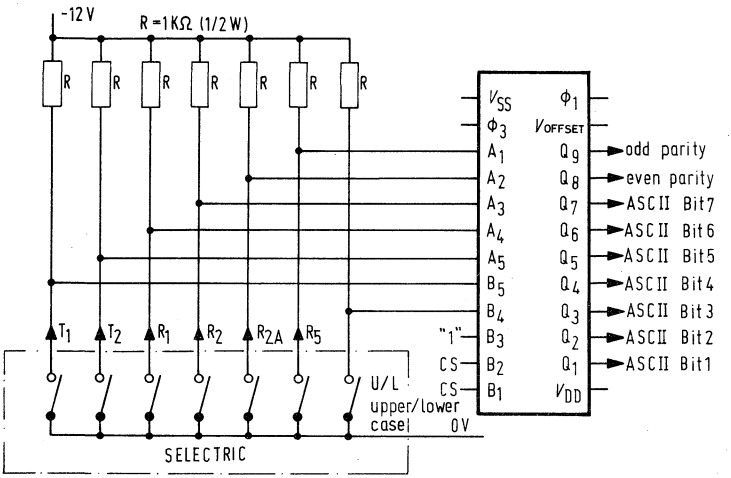




3. Sub-program: SELECTRIC/ASCII code converter

When used as a SELECTRIC to ASCII code converter, type GDR 101-3900 changes the input signals of a teletype (7 input signals in SELECTRIC code) into ASCII-code with an even or odd parity. The control circuit for a machine with conventional wiring is shown by the figure below.
6 output signal leads of the SELECTRIC keyboard (R_1, R_2, R_{2A}, R_5, T_1 und T_2) are used. The U/L (upper/lower case) key produces input signal B_4 for the ROM.

Control circuit for the SELECTRIC/ASCII code converter



GDR 101
GDR 106

SELECTRIC signals with the address-bits for the code converter

SELECTRIC-contact		T_1	T_2	R_1	R_2	R_{2A}	R_5	SELECTRIC-contact		T_1	T_2	R_1	R_2	R_{2A}	R_5
Character								Character							
A / a	G 1	0	1	1	1	0	0	W / w	G 1	0	1	1	1	1	1
	K 0	0	1	1	1	0	0		K 0	0	1	1	1	1	1
B / b	G 1	1	0	1	1	1	1	X / x	G 1	1	0	0	0	0	0
	K 0	1	0	1	1	1	1		K 0	1	0	0	0	0	0
C / c	G 1	1	0	1	1	0	0	Y / y	G 1	1	1	0	1	1	1
	K 0	1	0	1	1	0	0		K 0	1	1	0	1	1	1
D / d	G 1	1	0	0	1	0	0	Z / z	G 1	0	0	0	0	0	1
	K 0	1	0	0	1	0	0		K 0	0	0	0	0	0	1
E / e	G 1	1	0	0	1	0	1	(/)	G 1	0	0	0	0	0	0
	K 0	1	0	0	1	0	1		K 0	0	0	0	0	0	0
F / f	G 1	1	1	1	0	0	0	@ / 2	G 1	0	0	1	0	0	1
	K 0	1	1	1	0	0	0		K 0	0	0	1	0	0	1
G / g	G 1	1	1	0	0	0	0	# / 3	G 1	0	0	1	0	0	0
	K 0	1	1	0	0	0	0		K 0	0	0	1	0	0	0
H / h	G 1	1	0	0	1	1	1	$ / 4	G 1	0	0	0	1	1	0
	K 0	1	0	0	1	1	1		K 0	0	0	0	1	1	0
I / i	G 1	0	1	1	1	0	1	% / 5	G 1	0	0	0	1	0	1
	K 0	0	1	1	1	0	1		K 0	0	0	0	1	0	1
J / j	G 1	1	1	0	0	0	1	¢ / 6	G 1	0	0	1	1	0	1
	K 0	1	1	0	0	0	1		K 0	0	0	1	1	0	1
K / k	G 1	1	0	1	1	0	1	& / 7	G 1	0	0	0	1	0	0
	K 0	1	0	1	1	0	1		K 0	0	0	0	1	0	0
L / l	G 1	1	0	0	1	1	0	* / 8	G 1	0	0	1	1	0	0
	K 0	1	0	0	1	1	0		K 0	0	0	1	1	0	0
M / m	G 1	0	1	0	0	0	0	(/ 9	G 1	0	0	1	1	1	1
	K 0	0	1	0	0	0	0		K 0	0	0	1	1	1	1
N / n	G 1	1	0	1	0	0	1	) / 0	G 1	0	0	0	1	1	1
	K 0	1	0	1	0	0	1		K 0	0	0	0	1	1	1
O / o	G 1	0	1	0	1	1	0	— / -	G 1	1	1	1	1	1	1
	K 0	0	1	0	1	1	0		K 0	1	1	1	1	1	1
P / p	G 1	1	1	0	1	0	1	+ / =	G 1	1	1	1	0	0	1
	K 0	1	1	0	1	0	1		K 0	1	1	1	0	0	1
Q / q	G 1	1	1	1	1	0	1	o / !	G 1	0	1	0	0	0	1
	K 0	1	1	1	1	0	1		K 0	0	1	0	0	0	1
R / r	G 1	0	1	0	1	0	0	: / ;	G 1	1	1	0	1	0	0
	K 0	0	1	0	1	0	0		K 0	1	1	0	1	0	0
S / s	G 1	0	1	0	1	1	1	" / ,	G 1	0	1	0	1	0	1
	K 0	0	1	0	1	1	1		K 0	0	1	0	1	0	1
T / t	G 1	1	0	0	0	0	1	' / '	G 1	1	1	1	1	0	0
	K 0	1	0	0	0	0	1		K 0	1	1	1	1	0	0
U / u	G 1	1	0	1	0	0	0	. / .	G 1	0	1	1	0	0	1
	K 0	1	0	1	0	0	0		K 0	0	1	1	0	0	1
V / v	G 1	0	1	1	0	0	0	? / /	G 1	1	1	0	1	1	0
	K 0	0	1	1	0	0	0		K 0	1	1	0	1	1	0

ASCII-signal ">" corresponds to SELECTRIC signal "C" (cent)
ASCII-signal "<" corresponds to SELECTRIC signal "o" (degree)

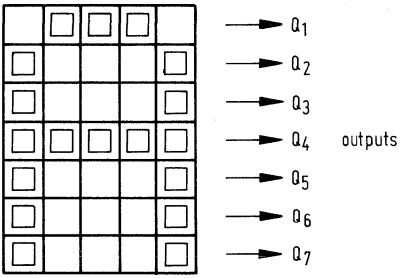
Explanation of the program patterns of types GDR 101-2701/2501

5×7-bit generator for vertical scanning character

GDR 101-2701

A_1	1	0	0	0	0
A_2	0	1	0	0	0
A_3	0	0	1	0	0
A_4	0	0	0	1	0
A_5	0	0	0	0	1

GDR 101-2701

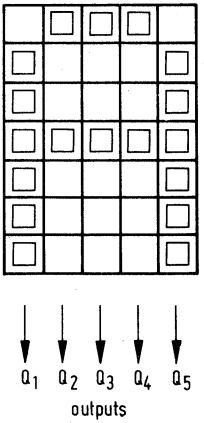


5×7 bit character generator for horizontal scanning

GDR 101-2501

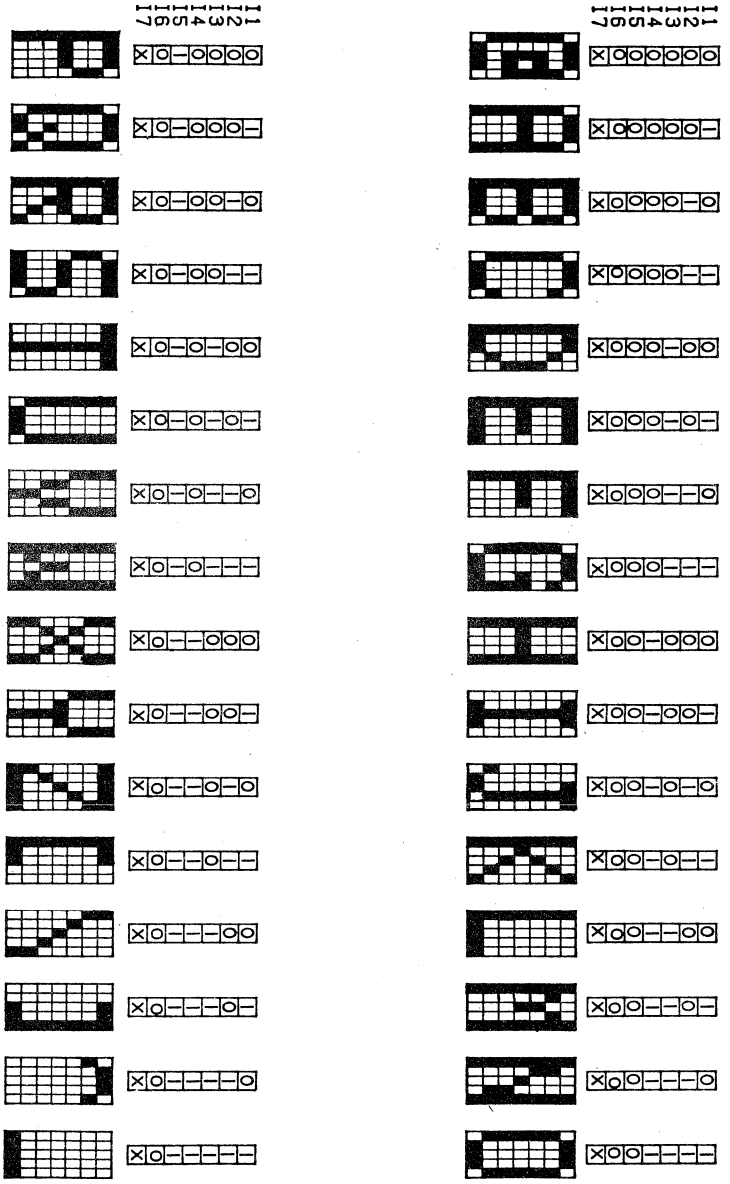
A_3	A_2	A_1
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

DR 101-2501

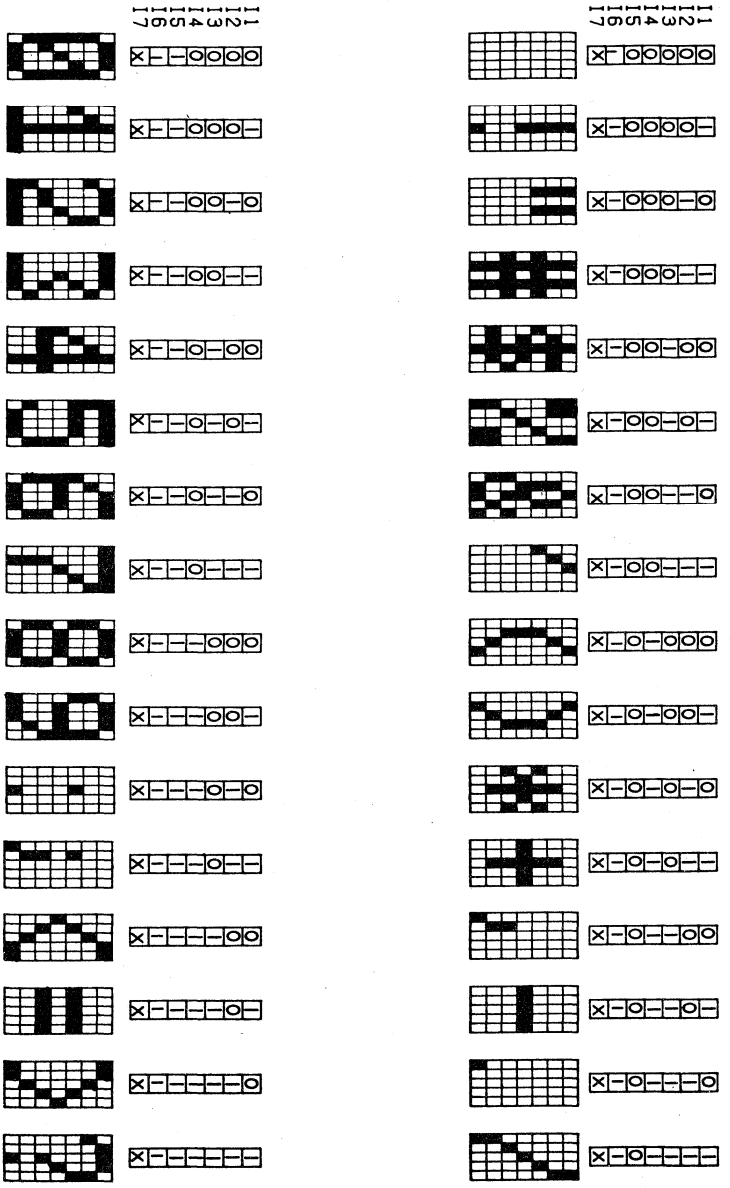


GDR 101
GDR 106

Character representation of the 5×7 bit character generators GDR 101-2701 and GDR 101-2501



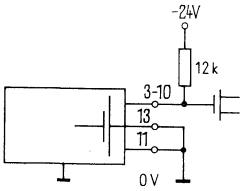
GDR 101
GDR 106



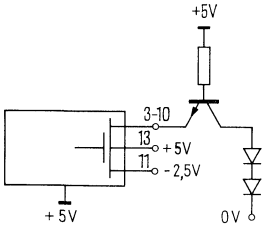
GDR 101
GDR 106

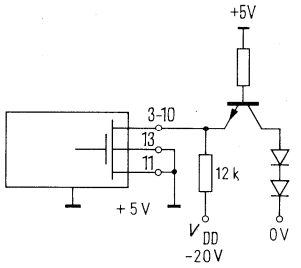
Diagrams of interface-stages

MOS-interface

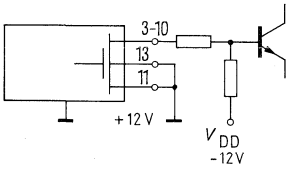


TTL-interface





Transistor-interface



Ordering codes

SAJ 131 = Q67000–J126
SAJ 131 A=Q67000–J170
SAJ 135=Q67000–J127
SAJ 135 A=Q67000–J285

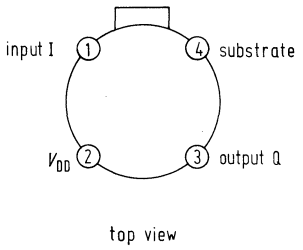
SAJ 131
SAJ 131 A
SAJ 135
SAJ 135 A

Static frequency divider 1000/1

Preliminary data

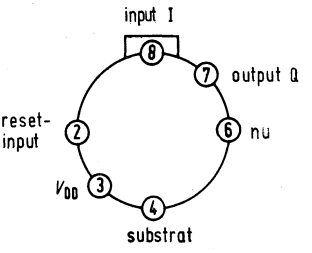
Types SAJ 131 and SAJ 135 are static MOS frequency dividers with a ratio 1000/1, in a package type 18 A 4 DIN 41876 (similar to TO-72). Upon request, this divider can be supplied with an external reset as SAJ 131 A or SAJ 135 A, respectively, in a package type 5 H 6 DIN 41873 (similar to TO-78). Fabrication of frequency dividers with a ratio 2048/1 is also possible if desired.

Pin-connections



top view

Package type 1 (SAJ 131, SAJ 135)



top-view

Package type 2 (SAJ 131 A, SAJ 135 A)

Maximum ratings		lower limit B	upper limit A	unit
Supply voltage	V_{DD}	–20	+0.3	V
Input voltage	V_I	–20	+0.3	V
Output current	I_Q	–2		mA
Operating temperature				
(range 1)	T_A	0	70	°C
(range 5)	T_A	–25	70	°C
Storage temperature	T_S	–55	125	°C

Static operating characteristics		Test conditions	lower limit B	typ	upper limit A	unit
Supply voltage	V_{DD}		–19	–18	–17	V
Supply current	I_{DD}		–4			mA
H-input voltage	V_{IH}		–2			V
L-input voltage	V_{IL}				–12	V
Input resistances	R_I		10			MΩ
H-output voltage	V_{QH}	I_Q=–1.0 mA	–7			V
L-output voltage	V_{QL}				–15	V
H-output current	I_{QH}	R_Q=10 kΩ			–1	mA
L-output current	I_{QL}	R_Q=10 kΩ	–10			μA

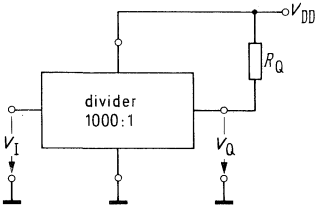
Output conditions and counting state of the circuit are not defined after the supply voltages have been turned on. In a continuous frequency dividing operation, the output level is normally L and switches to H with each 1000th input pulse for the duration of one pulse.

Dynamic operating characteristics 1000/1 divider		Test conditions	lower limit B	typ	upper limit A	unit
Signal input						
Input frequency	f_I	see fig. 3	0		25	kHz
Pulse width	t_{wLI}		10			µs
Pulse width	t_{wHI}		15			µs
HL-transition time	t_{tHLI}				2	µs
LH-transition time	t_{tLHI}					
Signal output						
Pulse width	t_{wHQ}					µs
Delay time	t_{dLH}				15	µs
HL-transition time	t_{tHLQ}				5	µs
LH-transition time	t_{tLHQ}				5	µs

2048/1 divider
The dynamic operating characteristics can be supplied upon request. The initial condition upon turn-on is not defined. The ouput changes its logic level after every 2048 input pulses (duty cycle 50%).
Frequency dividers with a higher maximum frequency rating are available.

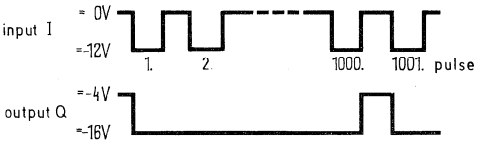
Connection

fig. 1



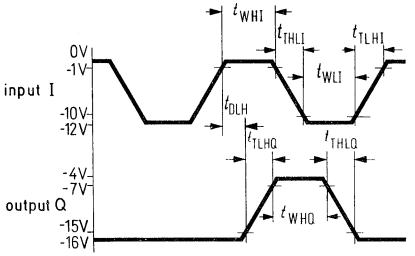
Function pulse diagram, 1000/1 divider

fig. 2



Pulse timing diagram, 1000/1 divider

fig. 3



Analog integrated circuits

Quality-data for analog integrated circuits

1. Warranty

If incoming testing shows that the AQL (Acceptance Quality Level) figures stated are exceeded, the customer is entitled to refuse acceptance and demand replacement of the shipment received.

2. AQL-figures

The AQL-figures define a maximum number of defective units acceptable in a shipment received.

Electrical defects

Single AQL, gradual electrical defects (1)	0.65
Single AQL, critical electrical defects (2)	0.40
ε AQL, electrical defects	0.45

Mechanical defects

Single AQL, gradual mechanical defects (3)	1.00
Single AQL, critical mechanical defects (4)	0.65
ε AQL, mechanical defects	1.00

Breakdown of defects

ad 1: Defects affecting the function in a minor way (electrical data too low or too high, noise etc.)

ad 2: Catastrophic failures (short circuits, no control) and defects seriously limiting the function (oscillation, high noise level, data short of minimum specifications by more than 50%)

ad 3: Slight mechanical defects (missing type-marking, marking difficult to identify, wrong dimensions, heavy stamping burrs at the leads, bent leads).

ad 4: Catastrophic failures (broken or cracked packages, wrong stamping, wrong position of the package-nose or marking of connection No. 1, leads not solderable).

3. Receiving-quality

The figures shown in the table are warranty-figures. The Average Qutgoing Quality (AOQ) of shipments is considerably higher, i.e. the proportion of defective units is much smaller than indicated by the AQL-figures.

4. Random sample testing

The AQL-figures are warrented for tests in accordance with random sampling test plan MIL Std. 105 D inspection level II.

Quality-figures for analog integrated circuits

Random-sampling test-plan for normal inspection (Mil-Std. 105 D, inspection level II)

Lot-size	sample -size	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1
9 to 15	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑ ↓
16 to 25	5	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↑ ↓
26 to 50	8	↓	↓	↓	↓	↓	↓	↓	0 1	↑ ↓	↓	1 2
51 to 90	13	↓	↓	↓	↓	↓	↓	1 0	↑ ↓	↓	1 2	2 3
91 to 150	20	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4
151 to 280	32	↓	↓	↓	↓	0 1	↑ ↓	↓	1 2	2 3	3 4	5 6
281 to 500	50	↓	↓	↓	0 1	↑ ↓	↓	1 2	2 3	3 4	5 6	7 8
501 to 1200	80	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3200 to 10000	200	0 1	↑ ↓	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	↑	↑ ↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑
35001 – 150000	500	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑
150001 – 500000	800	1 2	2 3	3 4	4 6	7 8	10 11	14 15	21 22	↑	↑	↑
500000 and more	1250	2 3	3 4	5 6	7 8	1011	14 15	21 22	↑	↑	↑	↑

Ac = permissible number of defective sample elements: lot accepted
Re = exceeding permissible number of defective sample elements: lot rejected

Additional requirement

As the combination "Acceptance 0 and Rejection 1" has a low degree of significance the next larger sample-size is to be used.

A. Analog integrated circuits for applications in the entertainment field

Summary of types

■ Not for new developments

Ordering codes:

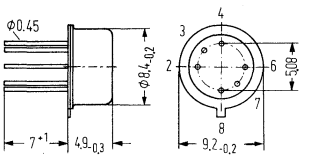
TAA 111: Q61901-A111
TAA 121: Q61901-A121

TAA 111
TAA 121

Three-stage AF-amplifier

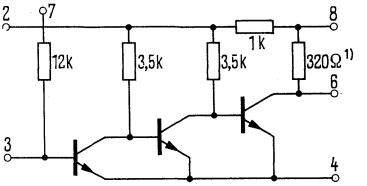
The semiconductor-circuits TAA 111 and TAA 121 are especially well suited as amplifiers for battery-operated sets with minimum space requirement. The case must not be connected to ground or any other potential.

Package outline



Package type 5 H 6 DIN 41873
(similar to TO 78)
weight about 1 g
Dimensions in mm

Circuit diagram



1) TAA 111 only

Maximum ratings

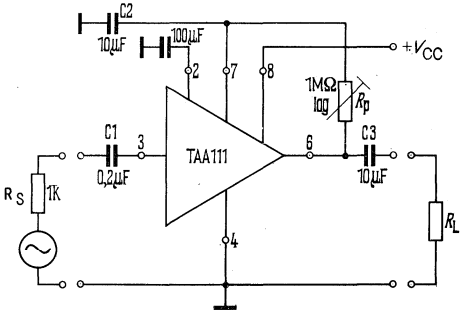
	TAA 111, TAA 121	
Supply voltage	V_{CC} 7	V
Ambient operating temperature	T_A –30 to 100	°C
Junction temperature	T_j 150	°C
Storage temperature	T_S –40 to 125	°C
Total power dissipation (T_A=45 °C)	P_r 350	mW
Thermal resistance (system-air)	R_{thSA} ≤ 300	°C/W

TAA 111
TAA 121

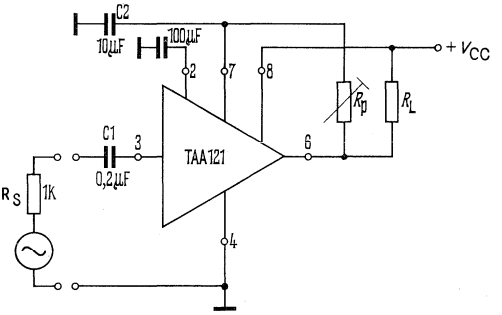
Operating characteristics (V_{CC}=4.5 V, T_A=25 °C), referring to the circuit shown below (V_{CC}=4.5 V, R_L=500 Ω). The quiescent point is adjusted with potentiometer R_p for minimum distortion at an ac output voltage V_{Qeff}=1 V.

		TAA 111	TAA 121	
Pot.-resistance	R_p	300 (40 to 1000)	300 (40 to 1000)	kΩ
Supply current (V_{CC}=4.5 V)	I_{SAT}	10 (<16)	8	mA
Supply current (V_{CC}=7 V)	I_{SAT}	17 (< 30)	–	mA
Voltage gain (f=1 kHz)	G_v	65 (> 62)	74	db
Distortion factor (V_{Qeff}=1 V, f=1 kHz)	d	1 (< 3)	1	%
Input Impedance	Z_{in}	≥ 3	≥ 3	kΩ
Lower cutoff frequency (–3 db[1])	f_e	80	80	Hz
Upper cutoff frequency (–3 db)	f_u	150	150	kHz
Output noise voltage (DIN 45405, R_S=1 kΩ)	V_N	4 (< 8)		mV
Noise voltage (referred to the input, DIN 45405, R_S=1 kΩ)	V_N	–	< 4	μV

Test circuits: TAA 111



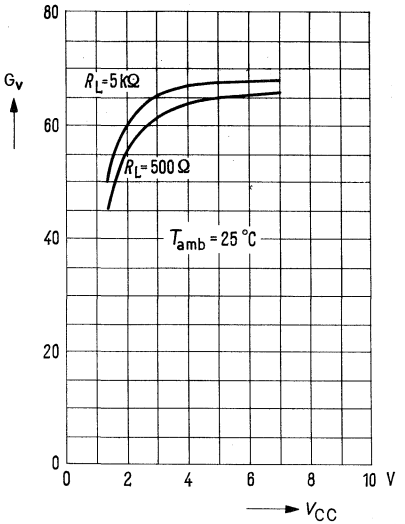
TAA 121



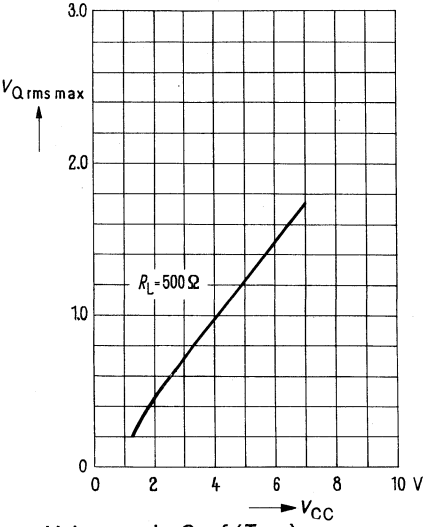
The values for C_1, C_2 and C_3 are approximations. The quiescent point of the circuit is adjusted using the potentiometer R_p (1 MΩ log.)

[1]) Depends on external circuit

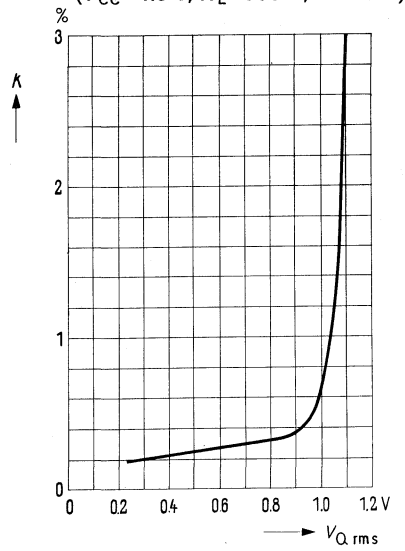
Voltage gain $G_v=f(V_{CC})$
(f=1 kHz, R_L=parameter)



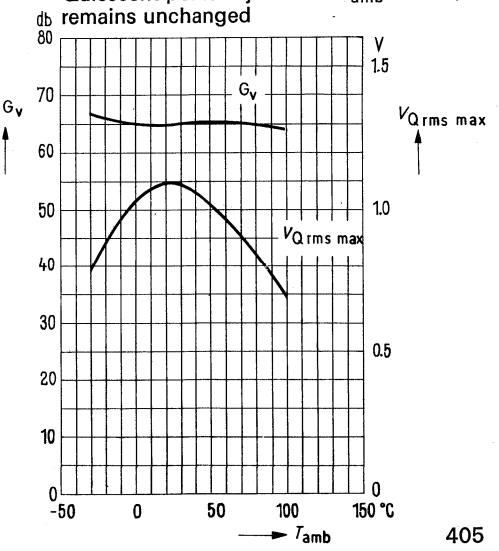
Output voltage $V_{Q\,rms\,max}=f(V_{CC})$
(f=1 kHz, k_{tot}=3%, T_{amb}=25 °C)



Distortion factor $k=f(V_{Qrms})$
(V_{CC}=4.5 V, R_L=500 Ω, f=1 kHz)



Voltage gain $G_v=f(T_{amb})$;
(f=1 kHz, V_{CC}=4.5 V, R_L=500 Ω)
Output voltage $V_{Qrms\,max}=f(T_{amb})$
(f=1 kHz, k_{tot}=3%, V_{CC}=4.5 V, R_L=500 Ω)
Quiescent point adjusted at T_{amb}=25 °C,
remains unchanged



TAA 131
TAA 141

Ordering codes:

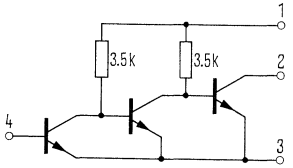
TAA 131: Q61901-A131
TAA 141: Q61901-A141

Three-stage AF-amplifier

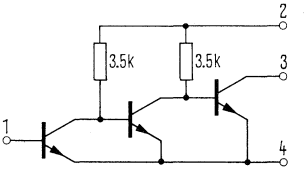
The integrated circuits TAA 131 and TAA 141 are especially well suited for small battery-operated sets. The case of the TAA 141 must not be connected to ground or any other potential.

Circuit diagrams

TAA 131

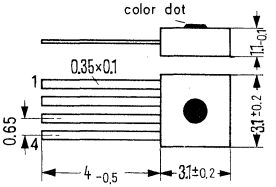


TAA 141



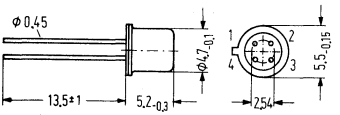
Package outlines

TAA 131



Plastic coating (U 38)
Weight approx. 0.02 g

TAA 141



Case 18 A 4
DIN 41876 (similar to TO 72)
Weight approx. 0.4 g

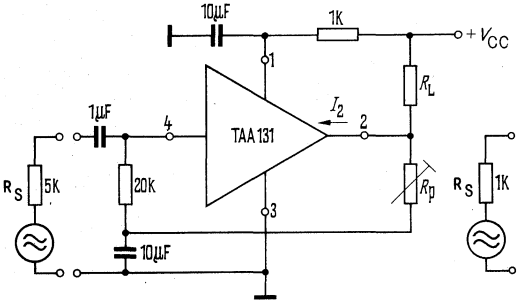
Maximum ratings		TAA 131	TAA 141	
Supply voltage	V_{CC}	5	5	V
Output stage collector current	$I_{2(3)}$ [1]	12	12	mA
Junction temperature	Tj	150	150	°C
Ambient operating temperature	T_{amb}	–20 to 90	–30 to 100	°C
Storage temperature	T_S	–40 to 125	–35 to 125	°C
Total power dissipation (T_{amb}=90 °C)	P_{tot}	50	60	mW
Thermal resistance (system – air)	R_{thSA}	≤ 600	≤ 600	°C/W

[1]) depends on external circuit

Operating characteristics (T_{amb}=25 °C)
referring to the circuit shown below

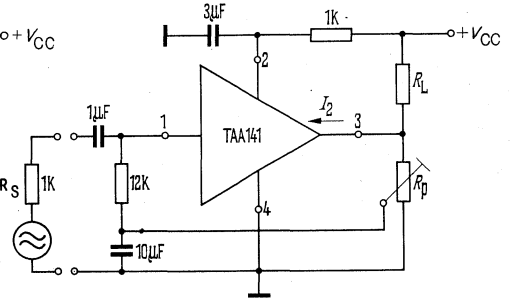
		TAA 131	TAA 141	
Pot.-resistance	R_p	400 (40-1000)	–	kΩ
Supply current (V_{CC}=1.3 V)	I_{SAT}	<1.2	–	mA
Supply current (V_{CC}=3 V)	I_{SAT}	–	<4	mA
Voltage gain (f=1 kHz)	G_V	57 (>50)	70 (>63)	db
Distortion factor (V_{Qrms}=0.1 V, f=1 KHz)	k	<10	–	%
Distortion factor (V_{Qrms}=0.9 V, f=1 KHz)	k	–	5 (<10)	%
Lower cutoff frequenvy (–3 db)[1]	f_l	<40	<40	Hz
Upper cutoff frequency (–3 db)	f_u	<20	<20	kHz
Noise voltage (referred to the input)				
DIN 45405, R_S=5 KΩ	V_N	<5	–	μV
R_S=1 KΩ	V_N	–	<4	μV

Test circuit: TAA 131



V_{CC}=13 V
R_L=500 Ω
Using R_p adjust I_2 to 0.75 mA

TAA 141

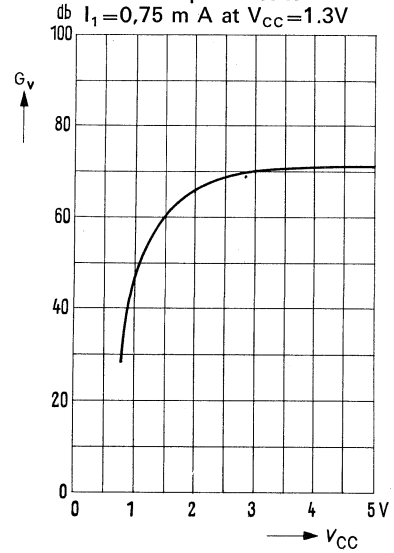


V_{CC}=3 V
R_L=470 Ω
Using R_p adjust I_2 to 0.75 mA

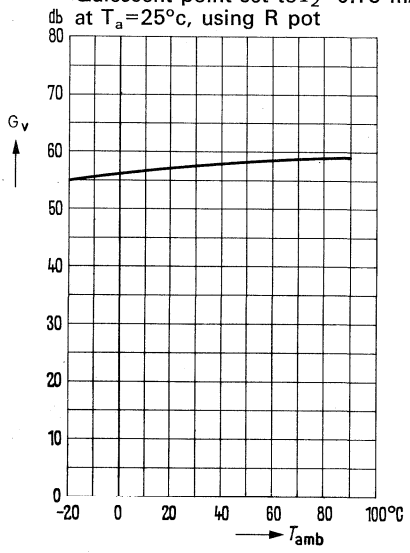
[1]) depends on external circuit

TAA 131
TAA 141

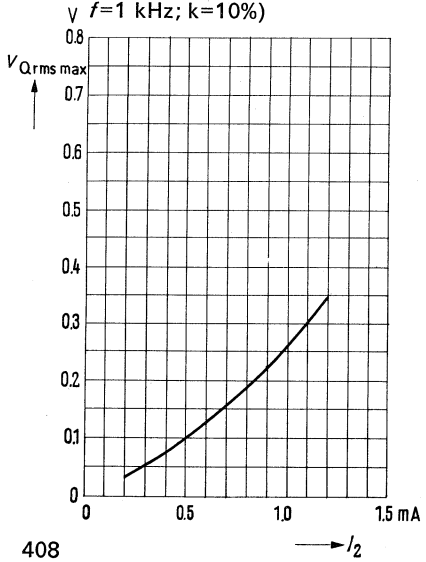
Voltage gain $G_V=f(V_{CC})$
$R_L=500\ \Omega$; $f=1$ kHz
Quiescent point set to
$I_1=0{,}75$ m A at $V_{CC}=1.3V$



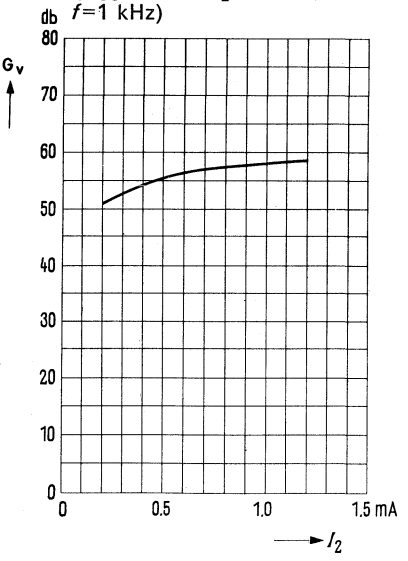
Voltage Gain $G_V=f(T_{amb})$
($V_{CC}=1.3V$; $R_L=500\Omega$; f=I kHz
Quiescent point set to $I_2=0.15$ mA
at $T_a=25°c$, using R pot



Output voltage $V_{Q\ eff\ max}=f(I_2)$
($V_{CC}=1.3$ V; $R_L=500\ \Omega$;
$f=1$ kHz; k=10%)



Voltage gain $G_V=f(I_2)$
($V_{CC}=1.3$ V; $R_L=500\ \Omega$;
$f=1$ kHz)



Ordering codes

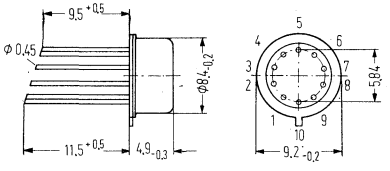
TAA 151	Q67000-A1
TAA 151 S	Q67000-A55

TAA 151
TAA 151 S

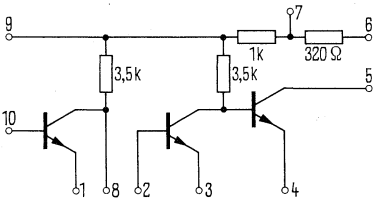
Three-stage linear amplifier

The integrated circuits TAA 151 and TAA 151 S are linear amplifiers which are universally applicable up to approx. 600 kHz. Pin 4 must always be connected to the lowest potential, pin 7 to the highest potential.

Case outlines



Circuit diagram



Case 5 J 10 DIN 41873
(similar TO-100)
Weight approx. 1,1g

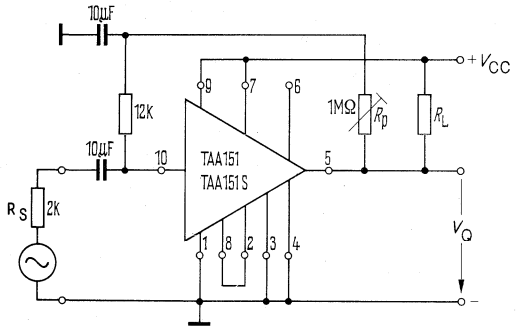
Maximum ratings

		TAA 151	TAA 151 S	
Supply voltage	V_{CC}	7	12	V
Ambient operating temperature	T_{amb}	–30 to 100	–30 to 100	°C
Junction temperature	T_j	150	150	°C
Storage temperature	T_S	–40 to 125	–40 to 125	°C
Total power dissipation (T_{amb}=45°C)	P_{tot}	350	350	mW
Voltages	$V_9/_3$	7	12	V
	$V_8/_1$	7	12	V
	$V_7/_4$	7	12	V
	$V_5/_4$	7	12	V
	$V_1/_{10}$	6	6	V
	$V_3/_2$	6	6	V
	$V_8/_{10}$	20	25	V
Currents	I_2	10	10	mA
	$-I_5$	40	40	mA
	$-I_8$	20	20	mA
	I_{10}	10	10	mA
Thermal resistance (system-air)	R_{thSA}	<300	<300	°C/W

TAA 151
TAA 151 S

Operating characteristics of the first transistor (T_A=25°C)		**TAA 151**	**TAA 151 S**	
Collector-emitter voltage	$V_{8/1}$	>7	>12	V
Current gain ($V_{8/1}$=1 V, I_8=1 mA)	B	80 (>30)	80 (>30)	
Collector-emitter saturation voltage (I_8=10 mA, I_{10}=1 mA	$V_{8/1\,sat}$	<1	<1	V
Noise figure ($V_{8/1}$=5 V, I_8=100 μA, R_G=2 KΩ, f=1 kHz)	N_{db}	2 (<10)	2(<10)	db
Noise figure ($U_{8/1}$=5 V, I_8=100 μA, R_G=2 kΩ, f=30 Hz to 15 kHz)	N_{db}	6(<10)	6(<10)	db
For the test circuit below the following values apply	at V_{CC}	7	12	V
	at R_L	150	150	Ω
	at R_S	2	2	kΩ
Voltage gain ($G_V=\frac{V_Q}{V_S}$, f=1 kHz)	G_V	>70	>70	db
Distortion factor ($V_{Q\,rms}$=1 V, f=1 kHz)	k	<5	<5	%

Test circuit



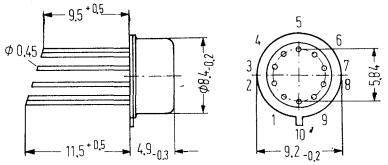
Ordering code
TAA 420: Q67000-A44

TAA 420

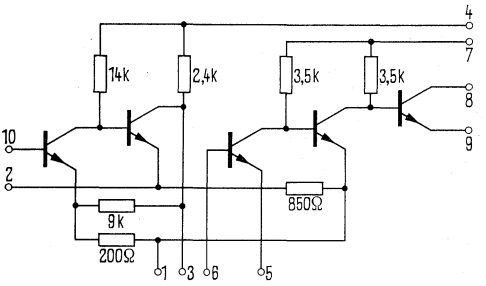
Five-stage AF-amplifier

The collector of the second stage and the base of the third stage of this AF-amplifier have been made accessible to permit a gain and distortion control. The input stage is of a low-noise type.

Case outline



Circuit diagram



Case 5 J 10 DIN 41873
(similar TO-100)
weight approx 1.1g

Maximum ratings

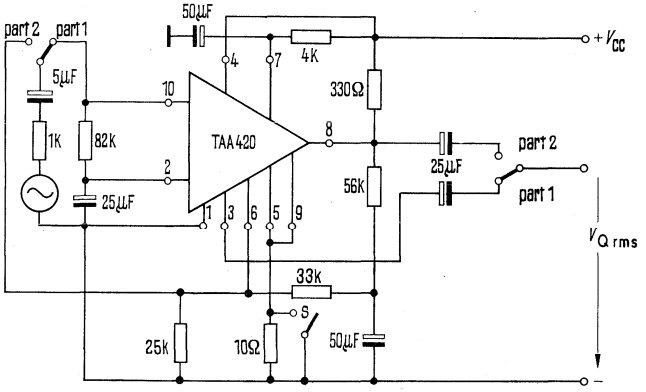
		TAA 420	
Supply voltage	V_{CC}	12	V
Ambient operating temperature	T_{amb}	–15 to 80	°C
Junction temperature	T_j	150	°C
Storage temperature	T_S	–40 to 125	°C
Total power dissipation (T_{Case}=45°C)	P_{tot}	350	mW
Thermal resistance			
system-air	R_{thSA}	300	°C/W
system-case	R_{thSC}	70	°C/W

TAA 420

Operating characteristics
(T_{amb}=25°C, V_{CC}=7.5 V, f=1 kHz)

Supply current	I_{CC}	12	mA
Front end (1st part)			
Voltage gain	G_v	31	db
Distortion factor (V_{Qrms}=1 V)	k	<4	%
Input impedance	Z_{in}	>40	kΩ
Noise voltage (referred to the input)			
R_S= 1 kΩ } DIN	V_N	2	μV
R_S=18 kΩ } 45405	V_N	9	μV
Cutoff frequency	f_c	⩾20	kHz
Output stage (2nd part)			
Voltage gain (Switch S closed)	G_v	>70	db
Votage gain (Switch S open)	G_v	29	db
Distortion factor (V_{Qrms}=2 V, S open)	k	<4	%
Cutoff frequency	f_c	⩾20	kHz

Test circuit

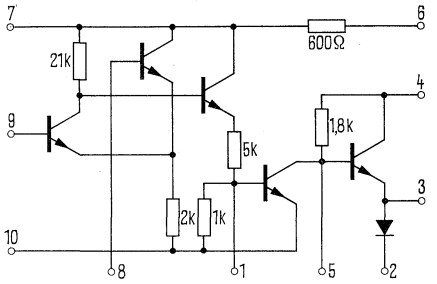


Ordering code
TAA 435: Q67000-A81

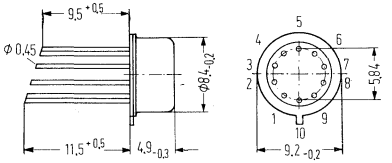
TAA 435

AF-amplifier (pre-amplifier and driver stage)

Circuit diagram



Case outline



Case 5J 10 DIN 41873
(similar TO-100)
Weight approx. 1.1 g)

Maximum ratings

		TAA 435	
Supply voltage	V_{CC}	18	V
Input voltage	$-V_{9/10}$	5	V
Output voltage	$V_{4/10}$	24	V
	$V_{3/10}$	20	V
Drive current	I_4	70	mA
Total power dissipation (T_{amb}=45°C)	P_{tot}	400	mW
Ambient operating temperature	T_{amb}	–25 to 80	°C
Junction temperature	T_j	125	°C
Storage temperature	T_s	–40 to 125	°C
Thermal resistance (system-air)	R_{thSA}	<300	°C/W

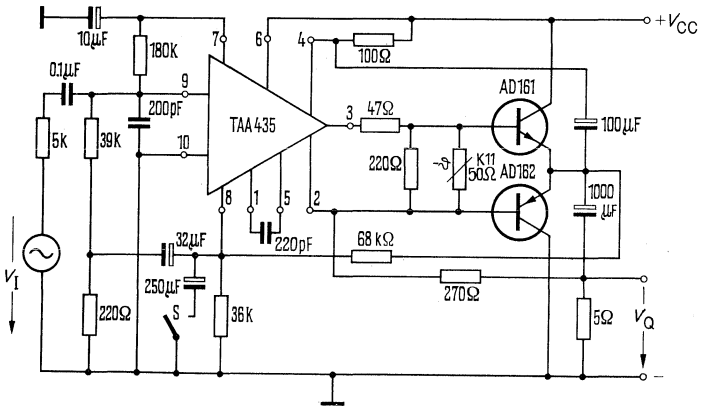
TAA 435

Static operating characteristics (V_{CC}=10-18 V, T_{amb}=25°C)

Diode forward voltage drop ($-I_2$=30 mA)	$V_3/_2$	0.8	V
Collector-emitter voltage (I_4=50 mA)	$V_4/_3$	<3.5	V

Dynamic operating characteristics (T_{amb}=25°C, V_{CC}=14 V)

Voltage gain (switch S open)[1]	G_v	50	db
Voltage gain (switch S closed) [2]	G_v	80	db
Input impedance	Z_{IN}	>70	kΩ
Noise figure (f=60 to 10000 Hz)	N	6	db
Output power (k=10%)	P_Q	≧4	W
Distortion factor (P_Q=1 W)	k	≦1	%



[1]) with negative feedback
[2]) without negative feedback

Ordering code

TAA 981: Q67000-A149

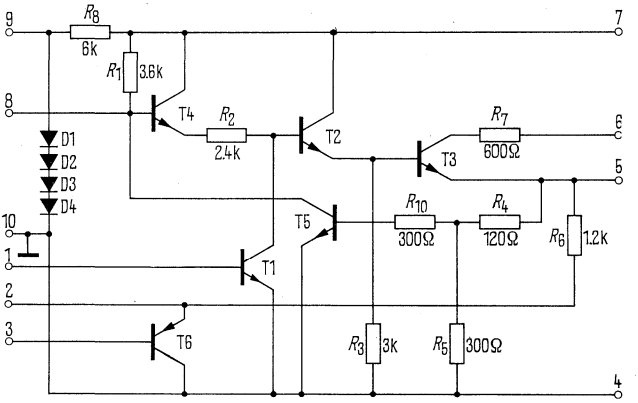
TAA 981

AM/FM IF-amplifier

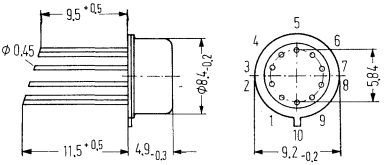
Combined AM/FM IF-amplifier for ac-or battery-operated radio receivers. It provides

a good regulation for AM-operation,
a good limiting for FM-operation,
a low current requirement,
a low sensitivity against supply voltage changes.

Circuit diagram



Case outline



Case 5 J 10 DIN 41873
(similar TO-100)
weight approx. 1g

Maximum ratings

	TAA 981	
Supply voltage	V_{CC}	11 V
Ambient operating temperature	T_{amb}	–15 to 80 °C
Storage temperature	T_s	–40 to 125 °C

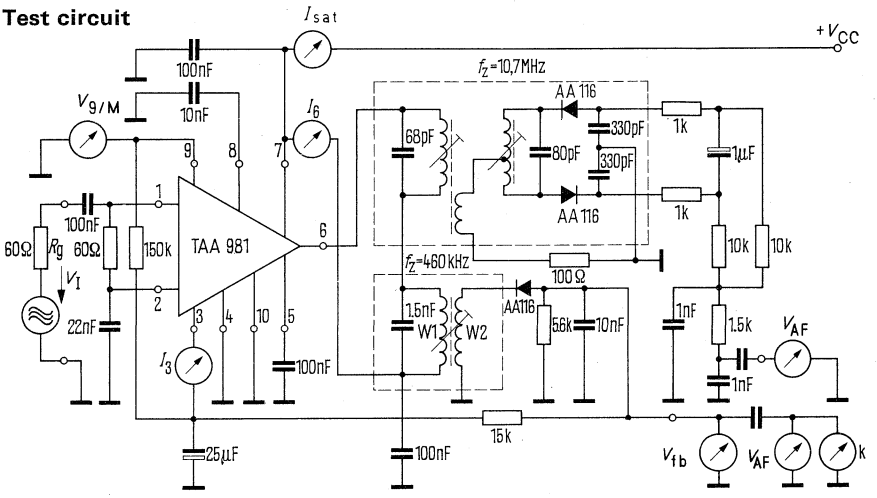
TAA 981

Operating characteristics (T_{amb}=25°C)

Range of operation	V_{CC}	4.5 — 11	V
AM-operation (f_I=460 kHz, V_{CC}=5 V)			
Total supply current (no signal)	I_{CC}	3.6	mA
Collector-current Tr 3 (no signal)	I_6	2	mA
Stabilized voltage	$V_9/_M$	2.8 (2.6–3.2)	V
Voltage gain	G_v	80	db
Range of regulation	$\triangle G_v$	50	db
Input starting regulation[1])	V_{IN}	50	μV
Regulation feedback voltage (V_{IN}=50 μV; f_{mod}=1 kHz; m=80%	$-V_{fb}$	200(>100)	mV
AF output voltage (U_{IN}=50 μV; f_{mod}=1 kHz; m=80%)	V_{AF}	120	mV
Min. input voltage causing overdrive	V_{OD}	15	mV
AM-operation (f_I=460 kHz, V_{CC}=9 V)			
Total supply current (no signal)	I_{CC}	6	mA
Collector-current Tr 3 (no signal)	I_6	2	mA
Stabilized voltage	$V_9/_M$	2.9 (2.6–3.2)	V
Voltage gain	G_v	90	db
Range of regulation	$\triangle G_v$	60	db
Input voltage starting regulation[1])	V_{IN}	15	μV
Regulation feedback voltage (V_{IN}=15 μV; f_{mod}=1 kHz; m=80%)	$-V_{fb}$	200 (>100)	mV
AF output voltage (V_{IN}=15 μV; f_{mod}=1 kHz; m=80%)	V_{AF}	120	mV
Min. input voltage causing overdrive	V_{OD}	25	mV
Distortion factor (V_{IN}=15 mV; f_{mod}=1 kHz; m=80%)	k	< 10	%
AF output voltage (V_{IN}=15 mV; f_{mod}=1 kHz; m=80%)	V_{AF}	300	mV
Base current Tr 6 (V_{IN}=15 mV; f_{mod}=1 kHz; m=80%)	I_3	< 30	μA
Input impedance (V_{IN}=50 μV)	Z_{IN}	12.50/100	Ω/pf
FM-operation (f_I=10.7 MHz, V_{CC}=5 V, $\triangle f$=75 kHz, f_{mod}=1 kHz)			
Voltage gain	G_v	76	db
Input voltage starting limiting[2])	V_{IN}	300	mV
AF output voltage	V_{AF}	200	mV
FM-operation (f_I=10.7 MHz, V_{CC}=9 V, $\triangle f$=75 kHz, f_{mod}=1 kHz)			
Voltage gain	G_v	86	db
Input voltage starting limiting[2])	V_{IN}	225	μV
AF output voltage (V_{IN}=100 mV)	V_{AF}	300	mV
AM suppression factor (m=30%)	V_{FM}/V_{AM}	50	db
Input impedance (V_{IN}=2 mV)	Z_{IN}	150/70	Ω/pf

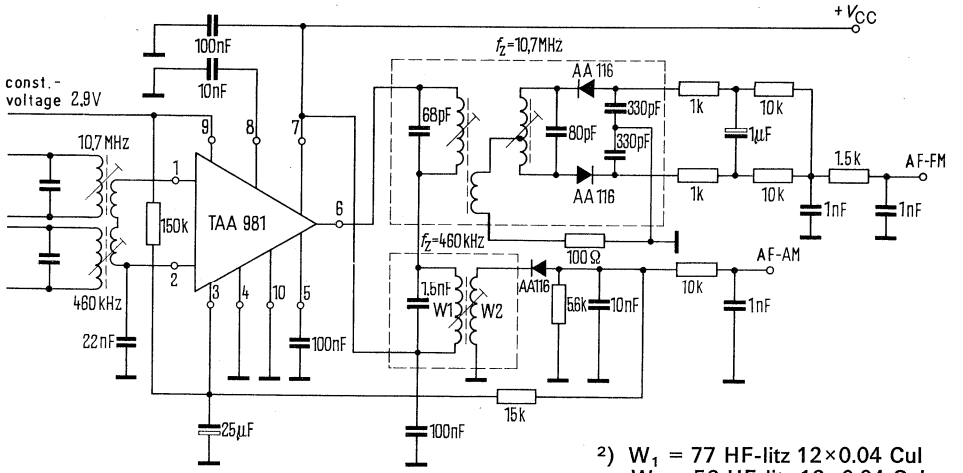
[1]) Start of regulation is defined as the input voltage for which $\triangle V_{IN}/\triangle V_{AF}$=10/3 db.
[2]) Start of limiting is defined as the input voltage at which the AF-output voltage has dropped by 3 db; reference-potential is V_{IN}=100 mV.

Test circuit



[1]) W_1 = 77 HF-litz 12×0.04 CuI
W_2 = 55 HF-litz 12×0.04 CuI

Application circuit



[2]) W_1 = 77 HF-litz 12×0.04 CuI
W_2 = 56 HF-litz 12×0.04 CuI

TAA 991
TAA 991 D

ordering code

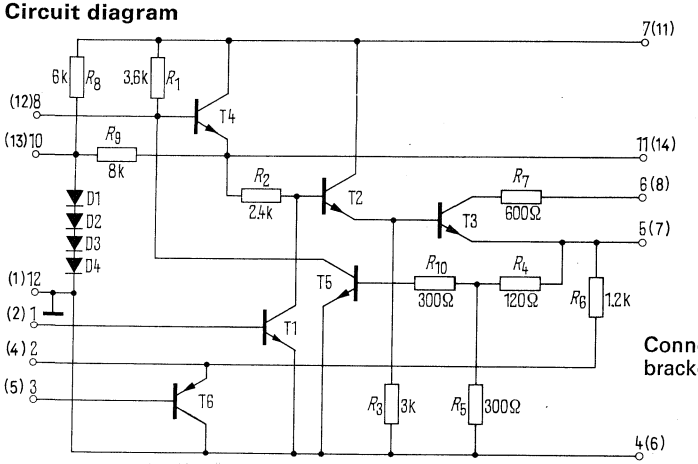
■ TAA 991: Q67000-A150
TAA 991 D: Q67000-A289

AM/FM IF-amplifier

Combined AM/FM IF-amplifier for radio receivers. The circuit is suited for ac-and battery-operated sets. An additionally available control voltage (connection B) permits control of a RF preamplifier stage.

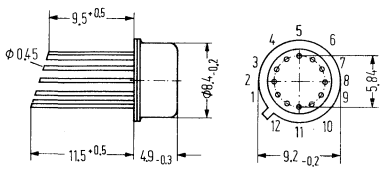
Good regulation for AM operation.
Good limiting qualities for FM operation.
Low current requirement.
Low supply voltage-dependence.

Circuit diagram

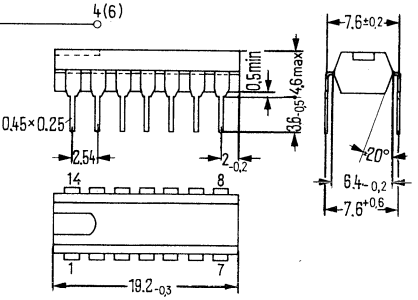


Connections shown in brackets are for TAA 991 D

Package outlines



Case 5 J 12 DIN 41 873
(similar TO-101)
weight approx. 1.2 g
■ Case discontinued for new products!



[1]) Plastic plug-in package, 14 pins
20 A 14 DIN 41 866 (TO 116)
Weight approx. 1.1 g
Dimensions in mm

Maximum ratings

	TAA 991, TAA 991 D	
Supply voltage	V_{CC} 11	V
Ambient operating temperature	T_{amb} −15 to 80	°C
Storage temperature	T_S −30 to 125	°C

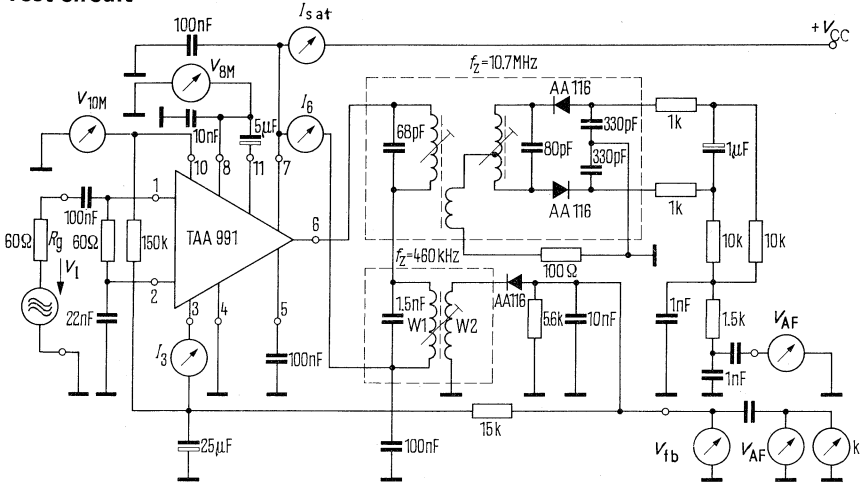
Operating characteristics (T_{amb}=25 °C)

Range of operation	V_{CC}	4.5 to 11	V
AM-operation (f_I=460 kHz, V_{CC}=5 V)			
Total supply current (no signal)	I_{CC}	3.6	mA
Collector current Tr 3 (no signal)	I_6	2	mA
Stabilized voltage	$V_9/_M$	2.8 (2.6–3.2)	V
Voltage gain	G_V	80	db
Range of regulation	$\triangle G_V$	50	db
Input voltage starting regulation[1])	V_{IN}	50	μV
Regulation feedback voltage (V_{IN}=50 μV; f_{mod}=1 kHz; m=80%)	$-V_{fb}$	200 (>100)	mV
AF output voltage (V_{IN}=50 μV; f_{mod}=1 kHz; m=80%)	V_{AF}	120	mV
Min. input voltage causing overdrive	V_{OD}	15	mV
AM-operation (f_I=460 kHz, V_{CC}=9 V)			
Total supply current (no signal)	I_{CC}	6	mA
Collector current Tr 3 (no signal)	I_6	2	mA
Stabilized voltage	$V_9/_M$	2.9 (2.6–3.2)	V
Voltage gain	G_v	90	db
Range of regulation	$\triangle G_v$	60	db
Input voltage starting regulation[1])	V_{IN}	15	μV
Regulation feedback voltage (V_{IN}=15 μV; f_{mod}=1 kHz; $_m$=80%)	$-V_{fb}$	200 (>100)	mV
AF output voltage (V_{IN}=15 μV; f_{mod}=1 kHz; m=80%)		120	mV
Min. input voltage causing overdrive	V_{OD}	25	mV
Distortion factor (V_{IN}=15 mV; f_{mod}=1 kHz; m=80%)	k	<10	%
AF output voltage (V_{IN}=15 mV; f_{mod}=1 kHz; m=80%)	V_{AF}	300	mV
Base current Tr 6 (V_{IN}=15 mV; f_{mod}=1 kHz; m=80%)	I_3	<30	μA
Input voltage starting preamplifier-regulation	V_{IN}	1	mV
Preamp. reg.-voltage ($V_{IN}\leq$200 μV)	$V_8/_M$	>2.8	V
Preamp. reg.-voltage ($V_{IN}\geq$3 mV)	$V_8/_M$	<0.5	V
Input impedance (V_{IN}=50 μV)	Z_{IN}	1250/100	Ω/pf
FM-operation (f_I=10.7 MHz, V_{CC} =5 V, Δf=75 kHz, f_{mod}=1 kHz)			
Voltage gain	G_v	76	db
Input voltage starting limiting[2])	V_{IN}	300	μV
AF-output voltage	V_{AF}	200	mV
FM-operation (f_I=10.7 MHz, V_{CC}=9 V, Δf=75 kHz, f_{mod}=1 kHz)			
Voltage gain	G_v	86	db
Input voltage starting limiting[2])	V_{IN}	225	μV
AF-output voltage (V_{IN}=100 mV)	V_{AF}	300	mV
AM suppression factor (m=30%)	V_{FM}/V_{AM}	50	db
Input impedance (V_{IN}=2 mV)	Z_{IN}	150/70	Ω/pf

[1]) Start of regulation is defined as the input voltage for which $\Delta V_{IN}/\Delta V_{AF}$=10/3 db.
[2]) Start of limiting is defined as the input voltage at which the AF output voltage has dropped by 3 db; reference-potential is V_{IN}=100 mV.

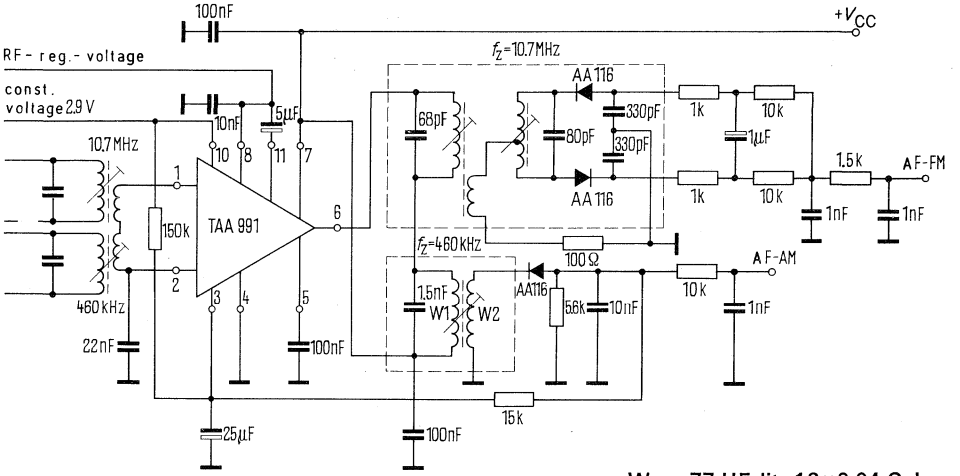
TAA 991
TAA 991 D

Test circuit



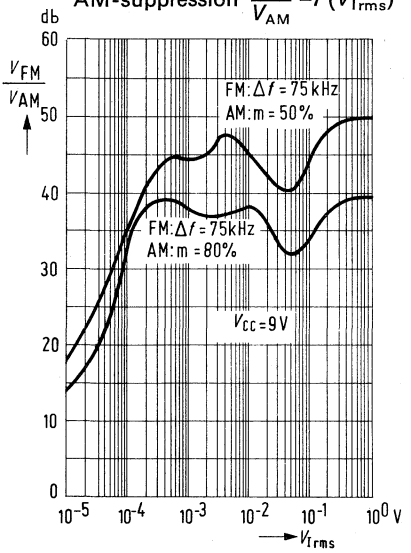
W_1=77 NF-litz 12×0.04 CuI
W_2=55 HF-litz 12×0.04 CuI

Application circuit

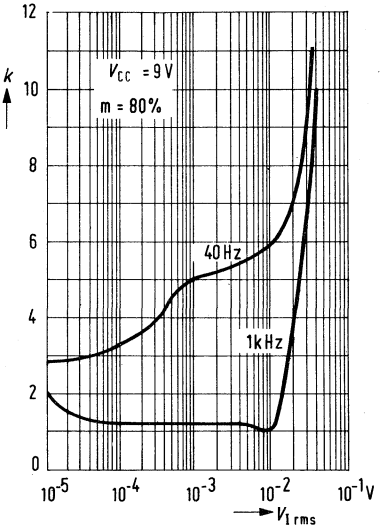


W_1 = 77 HF-litz 12×0.04 CuI
W_2 = 55 HF-litz 12×0.04 CuI

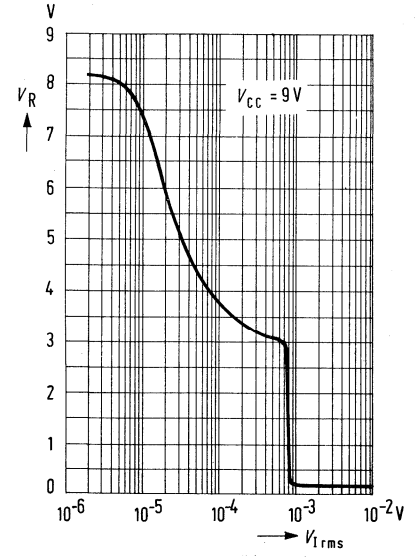
AM-suppression $\frac{V_{FM}}{V_{AM}} = f(V_{Irms})$



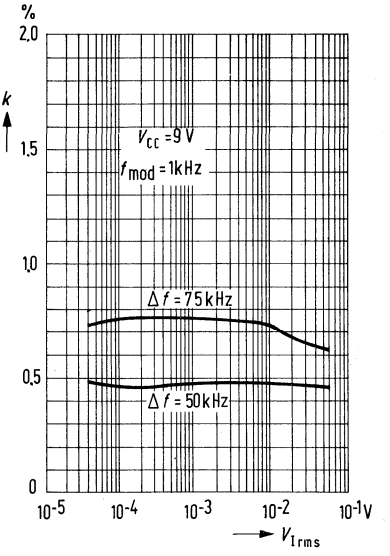
Distortion factor $k = f(V_{Irms})$



Reg.-voltage $V_R = f(V_{Irms})$

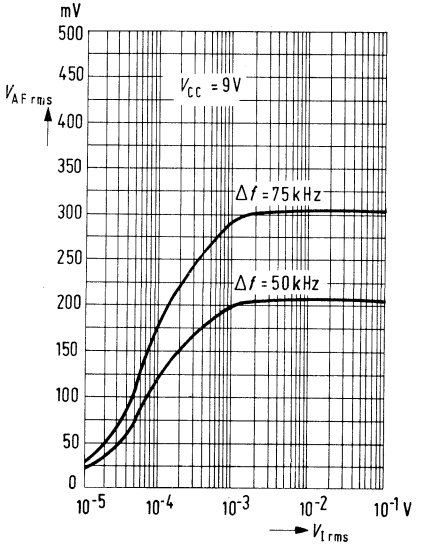


Distortion factor $k = f(V_{Irms})$

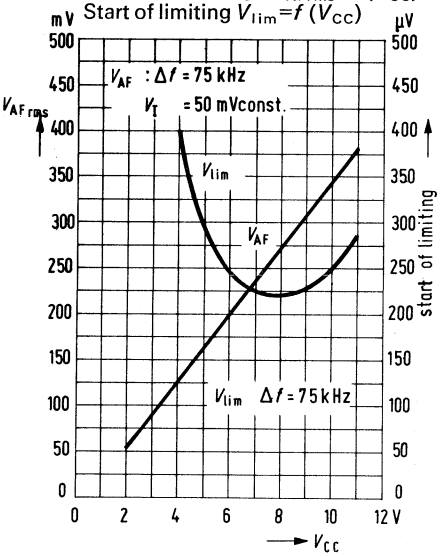


FM-operation (f_{IF}=10.7 MHz)

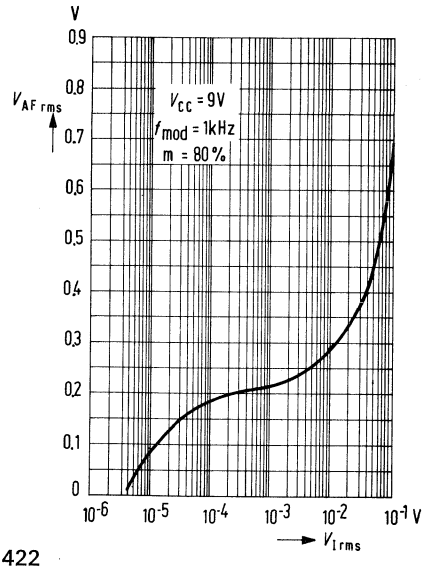
AF-output voltage $V_{AFrms}=f(V_{Irms})$



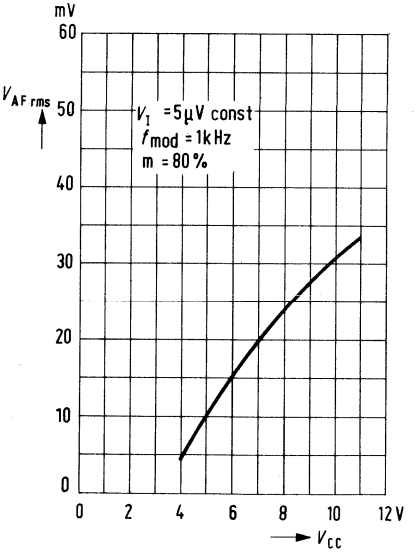
AF-output voltage $V_{AFrms}=f(V_{CC})$
Start of limiting $V_{lim}=f(V_{CC})$



AF-output voltage $V_{AFrms}=f(V_{Irms})$



AF-output voltage $V_{AFrms}=f(V_{CC})$



Ordering code

TBA 120: Q67000-A151
TBA 120 A: Q67000-A175

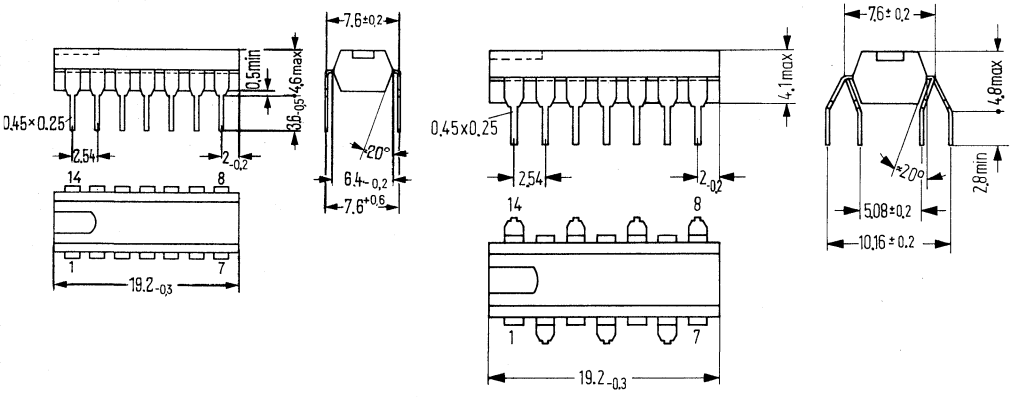
TBA 120
TBA 120 A

FM-IF amplifier and demodulator

Symmetrical six-stage amplifier with symmetrical coincidence-demodulator for the amplification, limiting and demodulation of frequency-modulated signals. Especially suited for radio receivers and the sound-IF portion in TV-sets. These circuits are applicable as limiter-amplifiers, as controlled demodulators or modulators or as mixers with excellent suppression of the input frequency.

Outstanding limiting qualities.
Very good frequency-stability of the converter-characteristic.
Wide supply voltage range (5 to 15 V).
Low external component requirement (for example filter-capacitors).

Package outlines:



Plastic plug-in package 20 A 14 DIN 41866
TO-116; (14 pins, DIL=dual-in-line)
Weight approx. 1.1 g

Plastic plug-in package 20 A 14 DIN 41866 (sim.)
(14 pins, QIL=quad-in-line)
Weight approx. 1.1 g

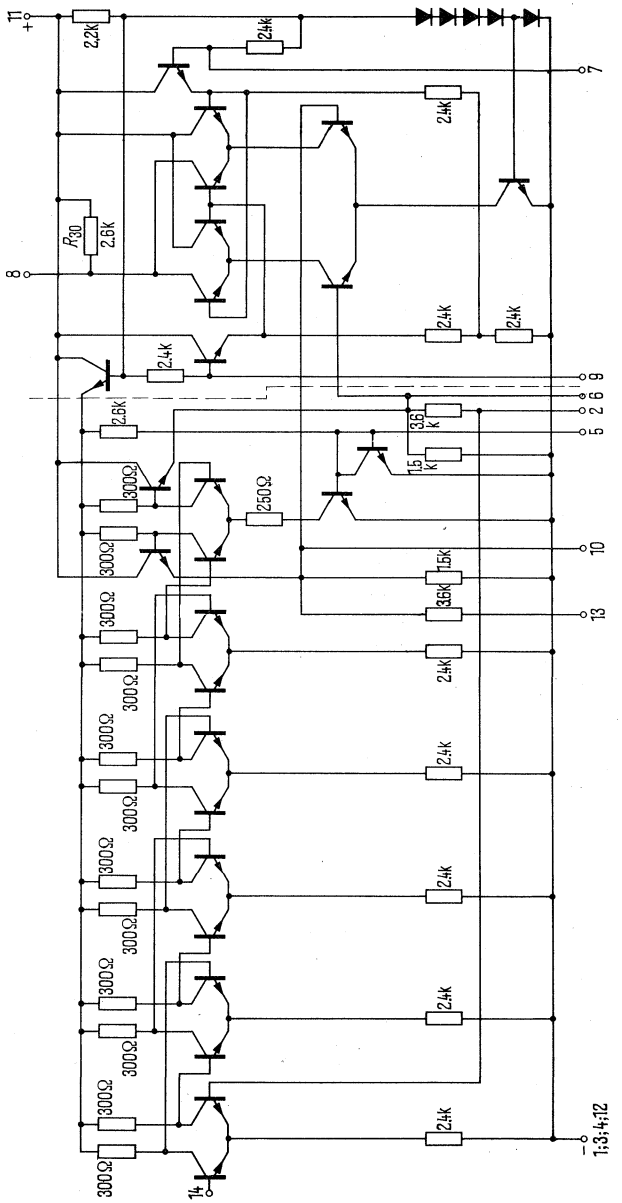
Maximum ratings

	TBA 120, TBA 120 A	
Supply voltage	V_{CC}	15	V
Range of operation	V_{CC}	5–15	V
Frequency range	f	0–35	MHz
Ambient operating temperature	T_{amb}	–15 to + 70	°C
Storage temperature	T_S	–40 to +125	°C

Operating characteristics (T_{amb}=25 °C, V_{CC}=12 V)

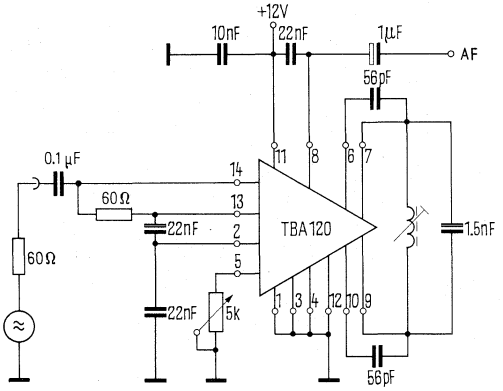
		min	typ	max	
Total current requirement	I_{CC}	12.5	16.5	20.5	mA
IF voltage gain (f=5.5 MHz)	G_v		60		db
IF output voltage at limiting, each output	V_{QPP}		240		mV
V_{AF}-output voltage (f=5.5 MHz, Δf=±25 kHz, V_I=10 mV, f_{mod}=1 kHz, Q_B≈45)	V_{AFrms}		0.85		V
V_{AF}-output voltage (f=5.5 MHz, Δf=±50 kHz, V_I=10 mV, f_{mod}=1 kHz, Q_B≈45)	V_{AFrms}	1.2	1.7		V
Distortion factor (f=5.5 MHz, Δf=±25 kHz, V_I=10 mV, f_{mod}=1 kHz, Q_B≈45)	k		1.8	3	%
Input voltage starting limiting (f=5.5 MHz, Δf=±50 kHz, f_{mod}=1 kHz, Q_B≈45)	V_{lim}		50	100	μV
Input impedance (f=5.5 MHz)	Z_I		15/7.8		kΩ/pf
Input impedance (f=10.7 MHz)	Z_I		7.2/6.2		kΩ/pf
Output resistance (pin 8)	R_Q	1.9	2.6	3.3	kΩ
Range of volume control	$\frac{V_{AFmax}}{V_{AFmin}}$		60		db
DC-portion of the output signal (V_I=0)	V_8	6.1	7.3	8.6	V
AM-suppression (f=5.5 MHz, V_I=10 mV, m=30%, f_{mod}=1 kHz)	a_{AM}		55		db

Circuit diagram for TBA 120 and TBA 120 A

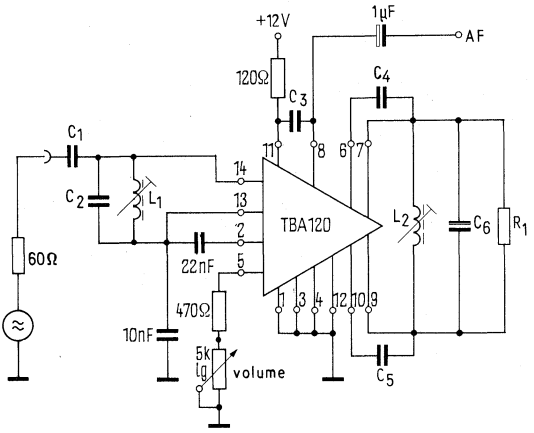


TBA 120
TBA 120 A

Test circuit



Recommended application-circuit

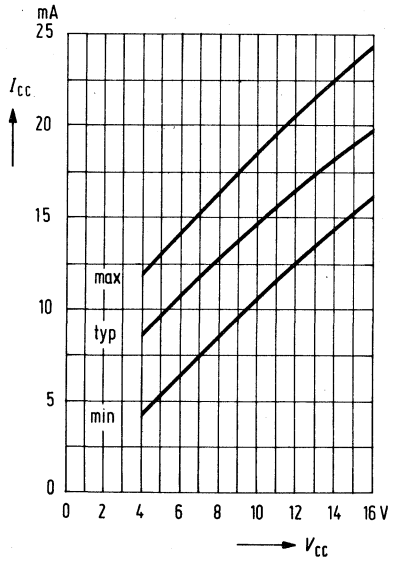


External circuit component data for various applications

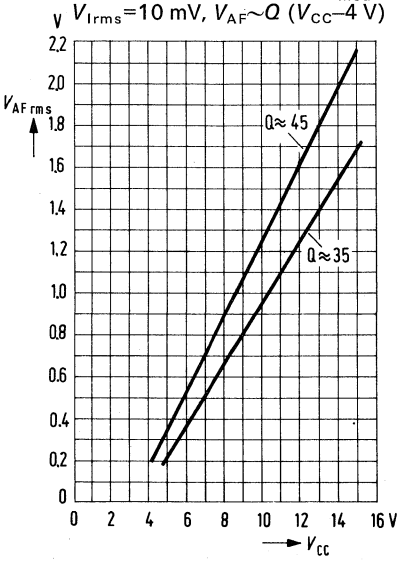
	Sound IF in TV sets	FM-IF in radio sets	
	5.5 MHz	10.7 MHz Mono	10.7 MHz Stereo
C_1	47 pF	27 pF	47 pF
C_2	220 pF	120 pF	150 pF
C_3	22 nF	22 nF	470 pF
C_4	56 pF	27 pF	30 pF
C_5	56 pF	27 pF	30 pF
C_6	1.5 pF	470 pF	330 pF
L_1	20 turns	20 turns	15 turns
L_2	8 turns	8 turns	12 turns
R_1	∞	∞	1 kΩ

A capacitive decoupling at supply voltage input 11 is not necessary. The 22 nF capacitor between pins 8 and 11, together with the integrated resistor R 30, constitutes the de-emphasis and may be reduced if required.
The distance of the peaks on the S-curve can be adjusted with the Q of the phase-shifting circuit. Zero-crossing corresponds to resonance-frequency. The two coupling capacitors of equal size connected between pins 6/7 and 9/10 should be dimensioned to produce approx. 250 mV p-p at the tank circuit at resonance.

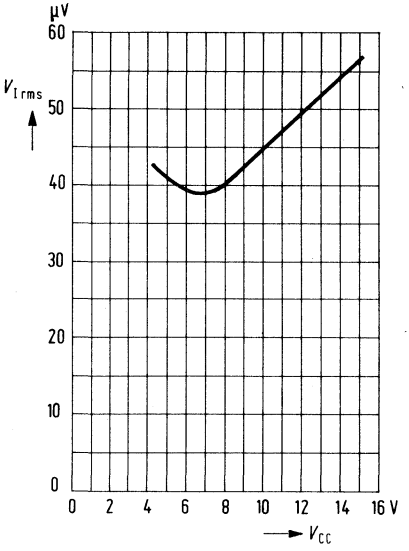
Current requirement $I_{CC}=f(V_{CC})$



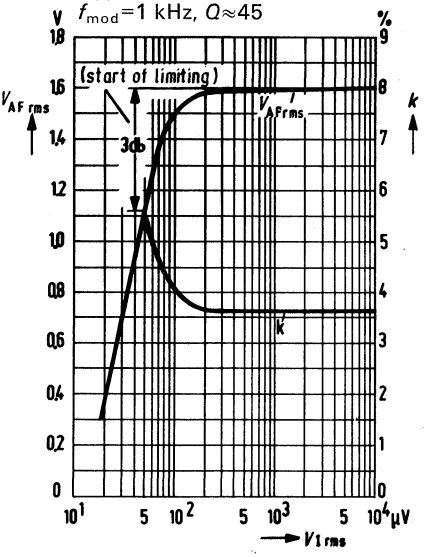
AF-output voltage $V_{AFrms}=f(V_{CC})$
f=5.5 MHz, $\Delta f=\pm 50$ kHz, f_{mod}=1 kHz,
V_{Irms}=10 mV, $V_{AF}\sim Q$ (V_{CC}–4 V)



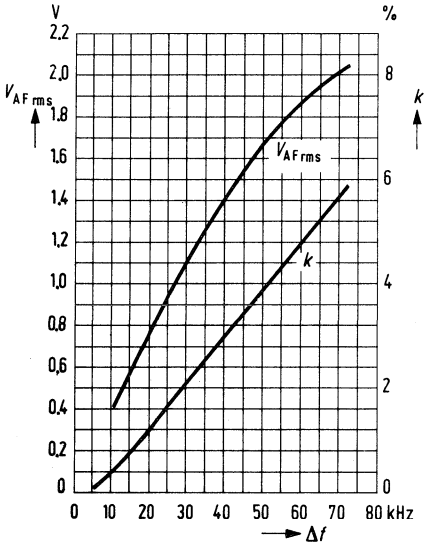
Start of limiting at $V_{Irms}=f(V_{CC})$
f=5.5 MHz, $\Delta f=\pm 50$ kHz, f_{mod}=1 kHz,
$Q\approx 45$



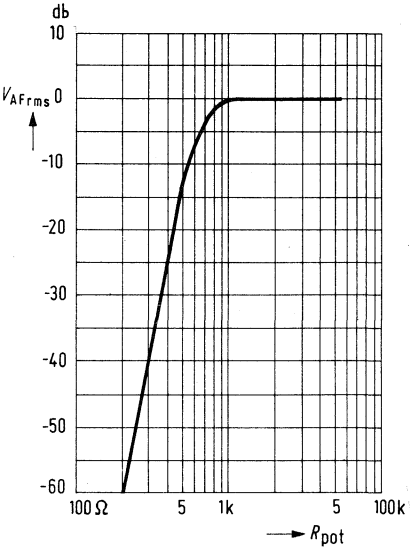
AF-output voltage $V_{AFrms}=f(V_{Irms})$
Distortion factor $k=f(V_{Irms})$
V_{CC}=12 V, f=5.5 MHz, $\Delta F=\pm 50$ kHz,
f_{mod}=1 kHz, $Q\approx 45$



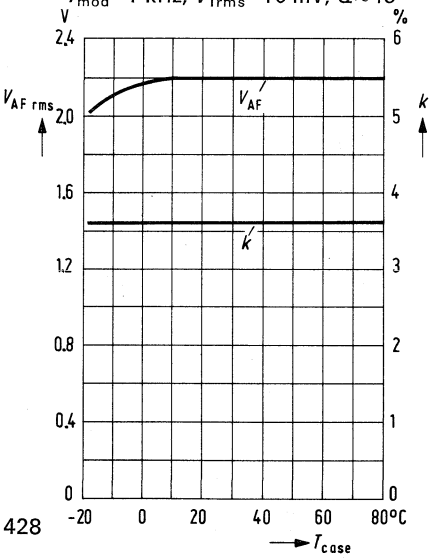
AF-output voltage $V_{AFrms}=f(\Delta f)$
Distortion factor $k=f(\Delta f)$
V_{CC}=12 V, f=5.5 MHz, f_{mod}=1 kHz
V_{Irms}=10 mV, $Q\approx45$



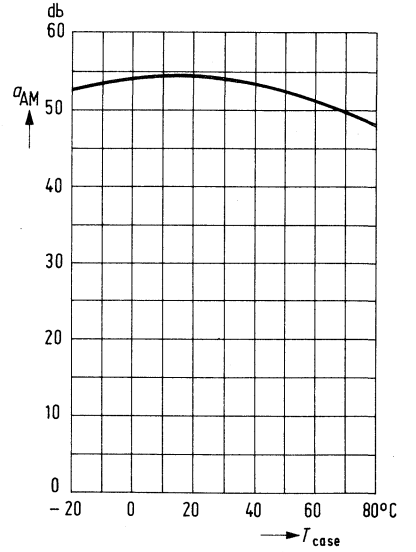
Volume control $\Delta V_{AF}=f(R_{pot})$
V_{CC}=12 V, f=5.5 MHz, Δf=±50 kHz,
f_{mod}=1 kHz, V_{Irms}=10 mV, $Q\approx45$
R_v=470 Ω



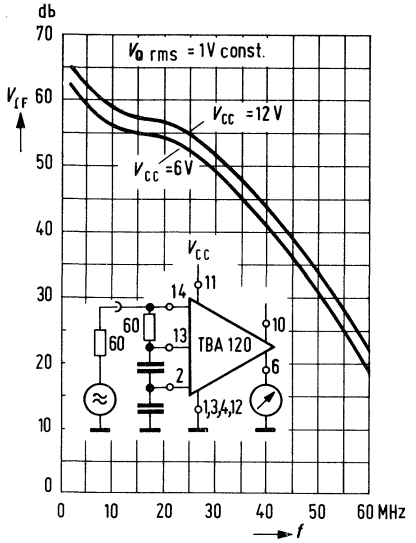
AF-output voltage $V_{AFrms}=f(T_{case})$
Distortion factor $k=f(T_p)$
V_{CC}=15 V, f=5.5 MHz, Δf=±50 kHz,
f_{mod}=1 kHz, V_{Irms}=10 mV, $Q\approx45$



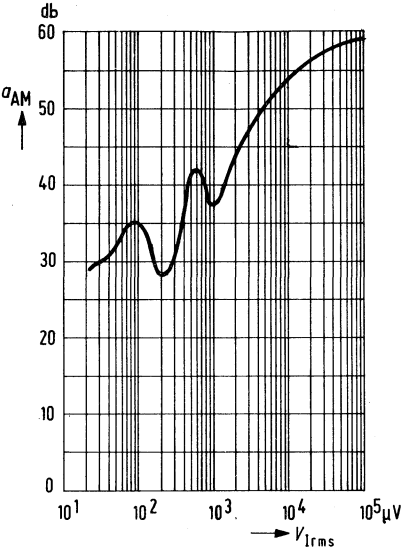
AM-suppression $a_{AM}=f(T_{case})$
V_{CC}=12 V, f=5.5 MHz, f_{mod}=1 kHz,
m=30%, V_{Irms}=10 mV, $Q\approx45$



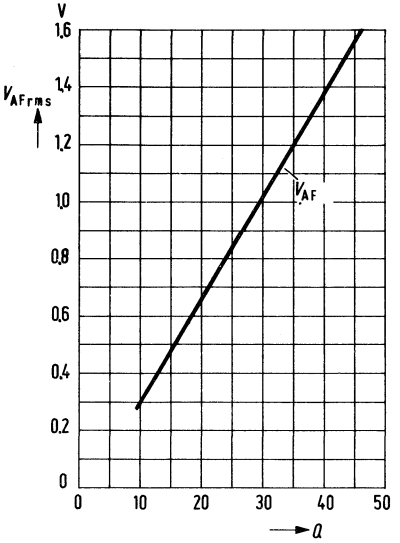
IF-amplification $G_{IF}=f(f)$



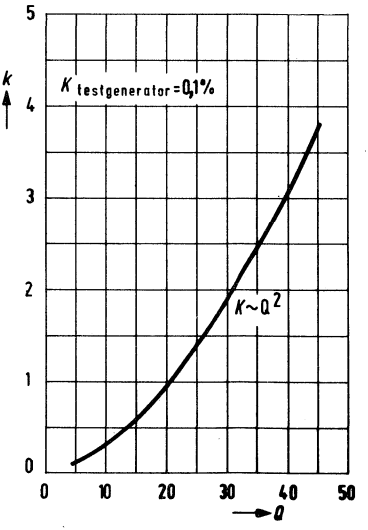
AM-suppression $a_{AM}=f(V_{Irms})$
V_{CC}=12 V, f=5.5 MHz, Δf=±50 kHz,
f_{mod}=1 kHz, m=30%, $Q\approx 45$



AF-output voltage $V_{AFrms}=f(Q)$
V_{CC}=12 V, f=5.5 MHz, Δf=±50 kHz,
f_{mod}=1 kHz, V_{Irms}=10 mV,



Distortion factor $k=f(Q)$
V_{CC}=12 V, f=5.5 MHz, Δf=±50 kHz,
f_{mod}=1 kHz, V_{Irms}=10 mV



TBA 120 S
TBA 120 AS

Ordering code

TBA 120 S: Q67000-A490
TBA 120 AS: Q67000-A525

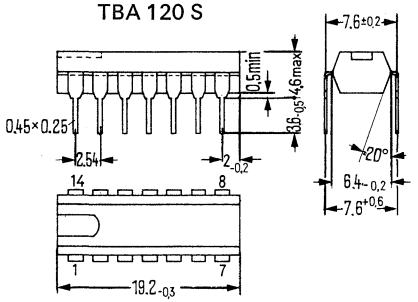
FM-IF-amplifier and demodulator

Preliminary data

Symmetrical 8-stage amplifier with symmetrical coincidence-demodulator for the amplification, limiting and demodulation of frequency-modulated signals, especially suited for the sound IF-portion in TV-sets and as FM-IF-amplifiers in radio sets. The circuit is directly interchangeable with TBA 120 (pin-compatible).

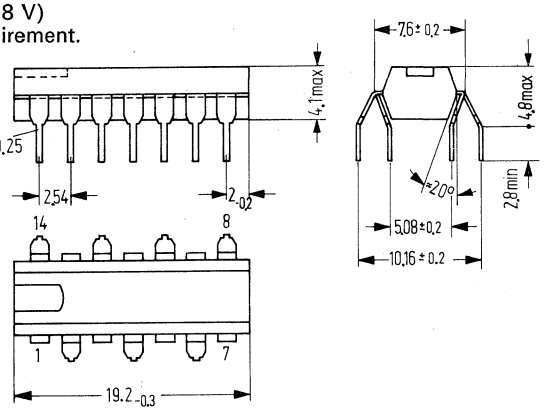
Outstanding limiting qualities
Very good frequency-stability of the converter-characteristic
Wide supply voltage range (6 to 18 V)
Very low external component requirement.

TBA 120 S



Plastic plug-in package 20 A 14 DIN 41866 (TO-116)
(14-pins, DIL) weight approx. 1.1 g

TBA 120 AS



Plastic plug-in package 20 A 14 DIN 41866 (14-pins, QIL) weight approx. 1.1 g

Maximum ratings

		TBA 120 S TBA 120 AS	
Supply voltage	V_{CC}	18	V
Ambient operating temperature	T_{amb}	–15 to +70	°C
Storage temperature	T_S	–40 to +125	°C
Total power dissipation	P_{tot}	400	mW
max. 1 min	P_{tot}	500	mW
Z-current	I_{12}	15	mA
max. 1 min.	I_{12}	20	mA
Voltage	V_5	4	V
Current	I_3	5	mA
Current	Ik	2	mA
Shunt resistance (max.)	$R_{13/14}$	1	kΩ
Thermal resistance (system-air)	R_{thSA}	≤120	°C/W
Operating range	V_{CC}	6 to 18	V
Frequency range	f	0 to 12	MHz

Operating characteristics of the amplifier with demodulator
(V_{CC}=12 V; T_{amb}=25° C)

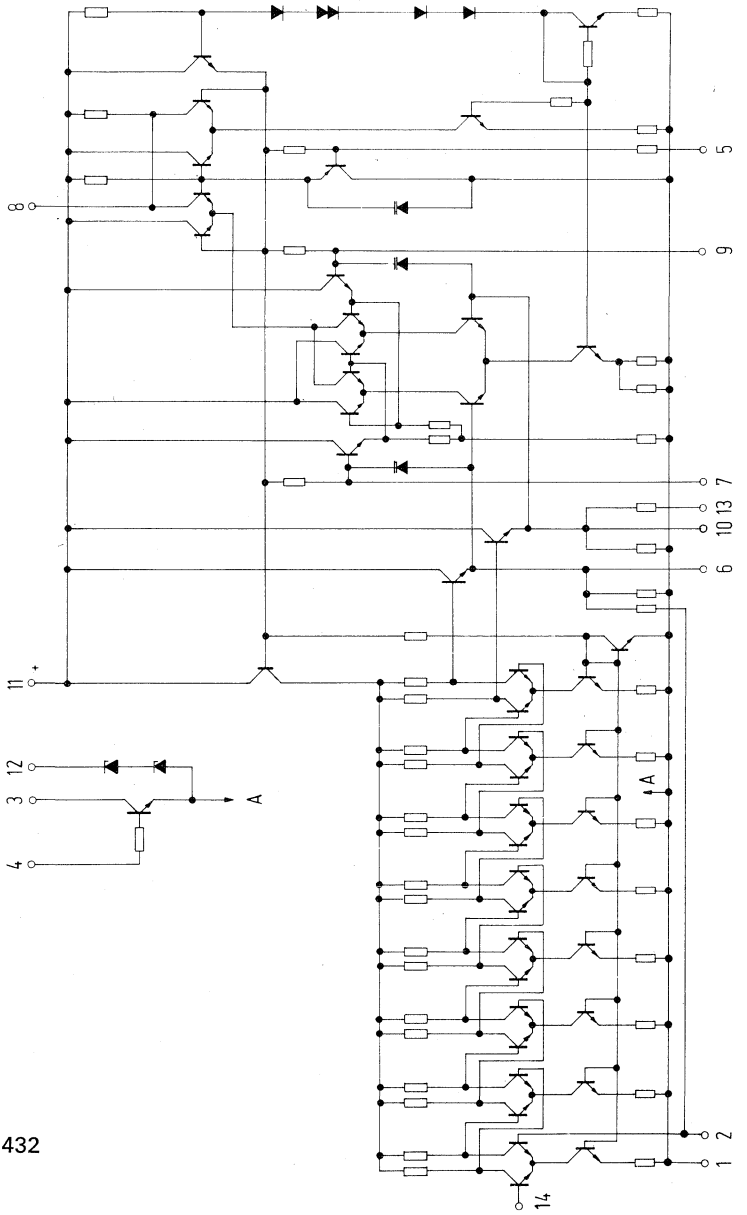
		min	typ	max	
Total current requirement ($R_5=\infty$; for R_5=0: I_{CC}+2 mA)	I_{CC}	10	14	18	mA
IF-voltage gain V_6/V_{14} (f=5.5 MHz)	G_v		68		db
IF-output voltage at limiting, each output	$V_{Q\,pp}$		250		mV
AF-output voltage	$V_{AF\,rms}$		1.1		V
f=5.5 MHz; Δf=±50 kHz; V_I=10 mV; f_{mod}=1 kHz; W=45; k=4%					
AF-output voltage f=5.5 MHz; Δf=±50 kHz; V_I=10 mV; f_{mod}=1 kHz; Q=20, k=1%	$V_{AF\,rms}$		0.55		V
Input voltage starting limiting f=5.5 MHz; Δf=±50 kHz; f_{mod}=1 kHz; Q=45	V_{lim}		30	60	μV
Input inpedance (f=5.5 MHz)	Z_I	15/6	40/4.5		kΩ/pf
Output resistance (pin 8)	R_Q		2.6		kΩ
Range of volume control	$\frac{V_{AF\,max}}{V_{AF\,min}}$		70		db
DC-portion of the output signal (V_I=0)	V_8		7.3		V
AM-suppression f=5.5 MHz; f=±50 Hz; V_I=500 μV; f_{mod}=1 kHz; m=30%	a_{AM}	45	55		db
Potentiometer resistance (–1 db down)	R_5		3.7	4.7	kΩ
Voltage (–1 db down)	V_5		2.4	2.6	kΩ
Potentiometer resistance (–70 db down)	R^5	1.0	1.4		kΩ
Voltage (–70 db down)	V_5		1.3		V

Characteristics of the auxiliary circuit

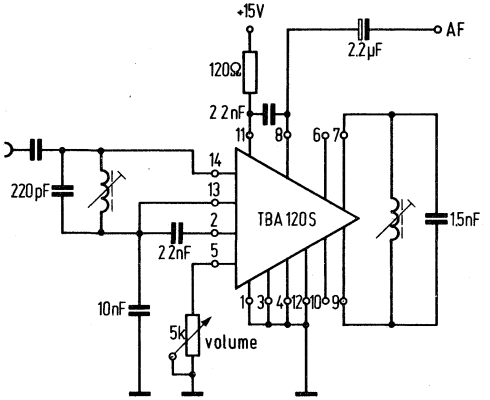
Z-voltage I_{12}=5 mA	V_{12}	11.2	12	13.2	V
Z-resistance	R_z		30		Ω
Breakdown voltage I_4=0; I_3=500 μA	$V_{CEO\,T43}$	13			
Current gain I_3=1 mA	h_{FE}	30	20		V

TBA 120 S
TBA 120 AS

Circuit diagram



Recommended application circuit
(5.5 MHz)

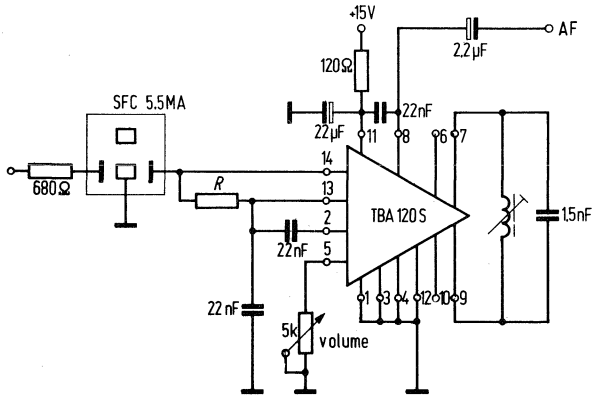


Pins 3 and 4 are connected to the collector and base of a transistor, respectively, which may be used as an AF-preamplifier ($I_C \leq 5$ mA) or as a bass/treble switch (dc on- or off-switching of an RC-circuit).
At pin 12 a Zener-diode (12 V) is accessible which can be used to stabilize the supply voltage of this integrated circuit or the voltage of other circuit elements in the set ($I_Z \leq 15$ mA).
The integrated circuit TBA 120 S is supplied in different groups. Parameter is the volume. A decrease of 30 db requires a resistor between pin 5 and ground with a resistance value depending on the group-number as shown below. The group-number is imprinted on the package.

Group	II	III	IV	V	
R 5	1.9–2.2	2.1–2.5	2.4–2.9	2.8–3.3	kΩ

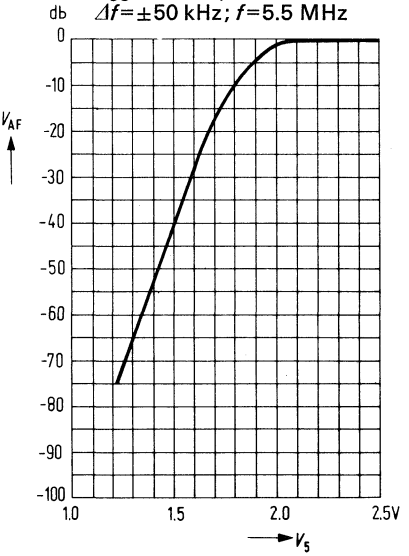
TBA 120 S with ceramic filter (Murata)

For a good selectivity, the ceramic filter should be combined with an LC-circuit

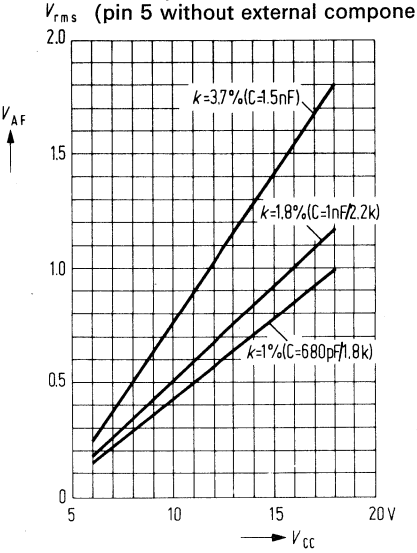


Frequency	Filter	Resistance R
10.7 MHz	SFC 10.7 MA	300 to 390 Ω
5.5 MHz	SFC 5.5 MA	560 to 680 Ω
4.5 MHz	SFC 4.5 MA	1000 to 1200 Ω

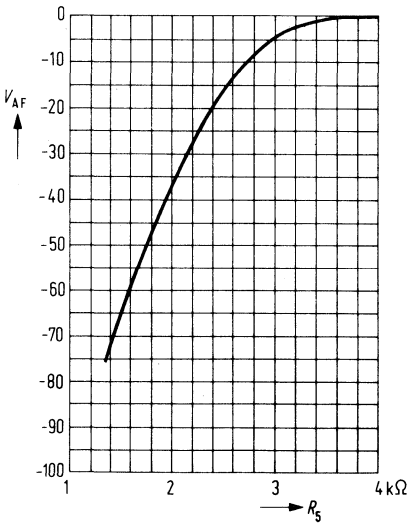
Output level $V_{AF}=f(V_5)$
$V_{CC}=12$ V, $V_I=10$ mV
$\Delta f=\pm 50$ kHz; $f=5.5$ MHz



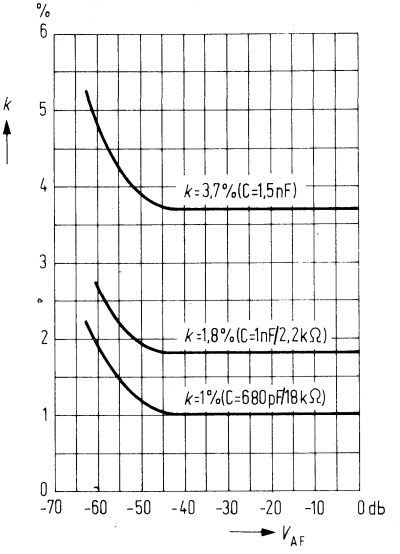
AF-output voltage $V_{AFrms}=f(V_{CC})$
60 Ω input, $\Delta f=\pm 50$ kHz
(pin 5 without external component)



Output level $V_{AF}=f(R_5)$
$V_{CC}=12$ V; $V_I=10$ mV
$\Delta f=\pm 50$ kHz; $f=5.5$ MHz

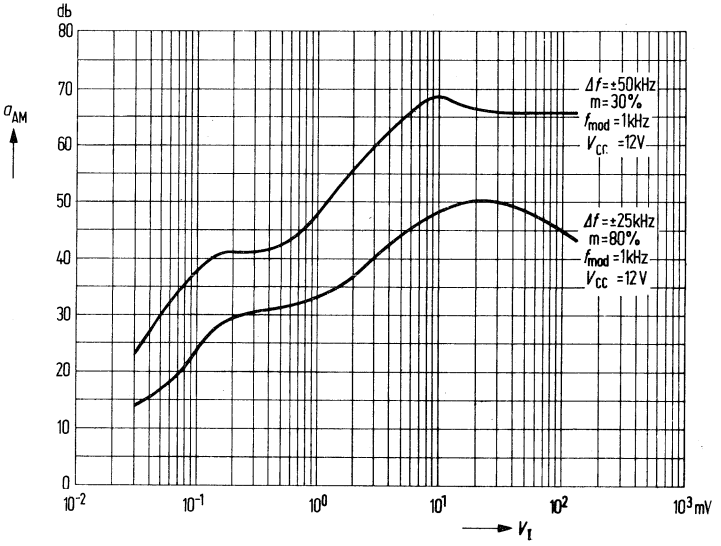


Distortion factor $k=f(V_{AF})$
$V_{CC}=12$ V; $f=5.5$ MHz; $\Delta f=\pm 50$ kHz



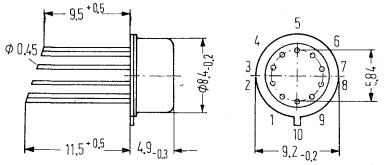
TBA 120 S
TBA 120 AS

AM-suppression $a_{AM}=f(V_{IN})$



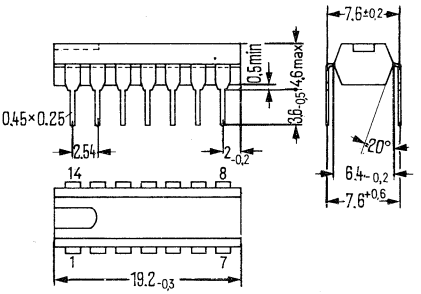
Package outlines for TBA 400 and TBA 400 D

TBA 400



Package 5 J 10 DIN 41873
(similar TO-100)
Weight 1.1 g

TBA 400 D



Plastic plug-in package 20 A 14 DIN 41866
14 pins
Weight approx. 1.1 g

Ordering code

TBA 400: Q67000-A228
TBA 440 D: Q67000-A623

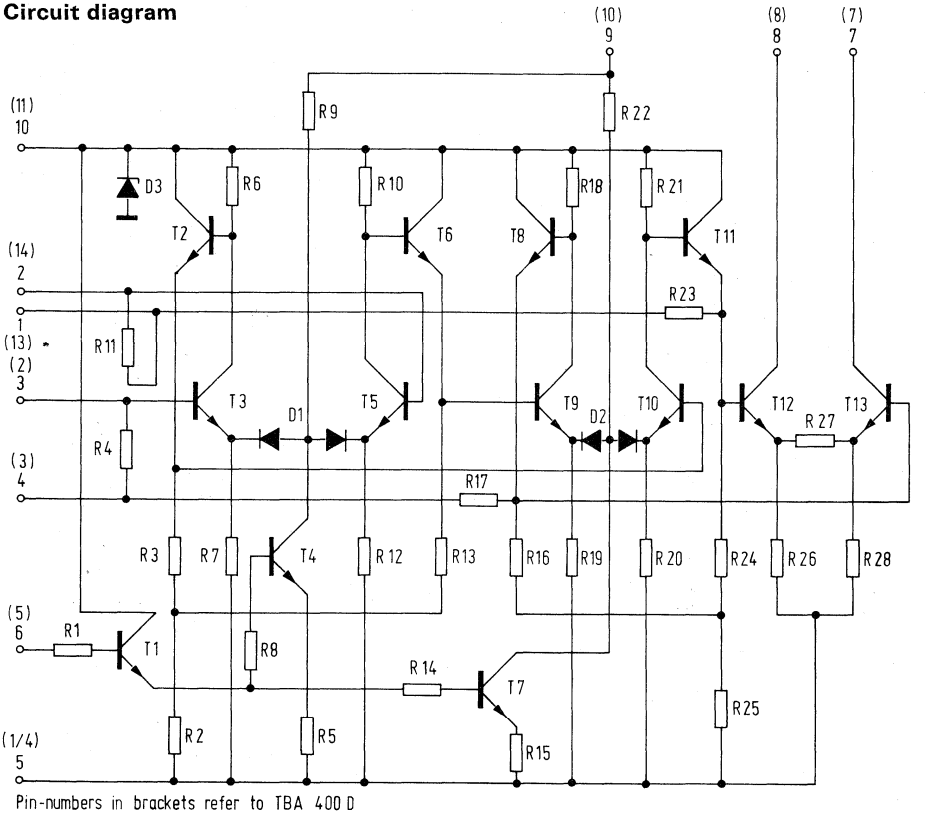
TBA 400
TBA 400 D

Gain-controlled broadband-amplifier

Gain-controlled 3-stage monolithic integrated broadband-amplifier with symmetrical input and output, especially suited for an application as video-IF-amplifier in TV-sets:

- 75 db gain, 60 db control range.
- Very good linearity of the gain over the entire control range.
- Distortion-free processing of input signals up to 240 mV_{rms}
- Noise-figure at 30 db down control typically 8 db.

Circuit diagram



Pin-numbers in brackets refer to TBA 400 D

Package-outlines see page 436

Pin-numbers in brackets refer to TBA 400 D

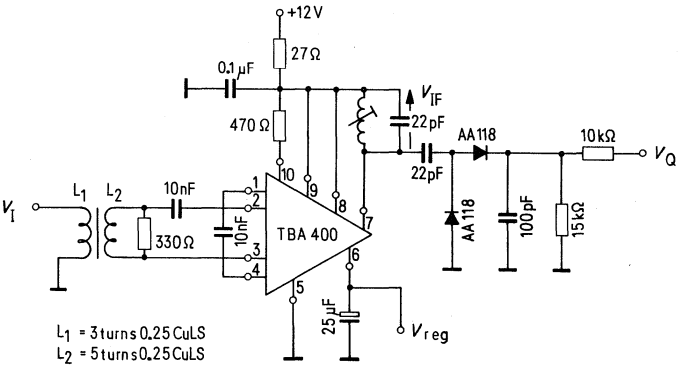
TBA 400
TBA 400 D

Maximum ratings

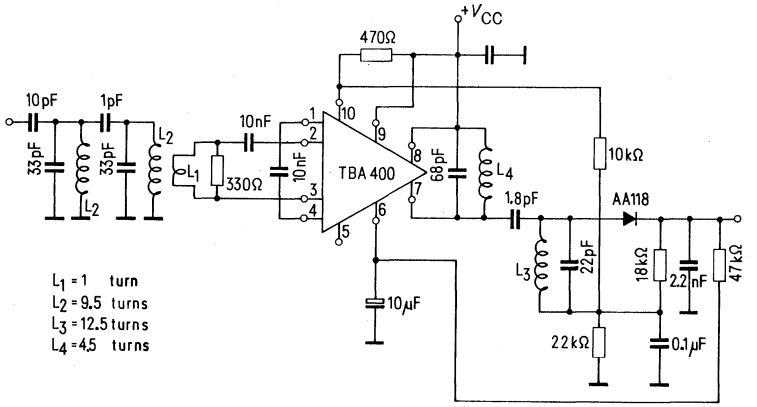
		TBA 400	
Supply voltage	V_{CC}	14	V
Regulating current	I_6	1	mA
Ambient operating temperature	T_{amb}	–15 to + 80	°C
Storage temperature	T_S	–40 to +125	°C
Total power dissipation	P_{tot}	400	mW
Range of operation	V_{CC}	7 to 14	V
Frequency range	f	0 to 200	MHz

Operating characteristics (V_{CC}=12 V, T_{amb}=25 °C)		min	typ	max	
Total current requirement	I_{CC}		25	32	mA
Output currents	I_7, I_8	2.7	4.5	6.3	mA
Difference in output currents (V_R=0)	I_7–I_8		0.4	0.9	mA
Difference in output currents (V_R=4)	I_7–I_8		0.5	1.6	mA
Regulating voltage (V_{Umax})	V_6			1	V
Regulating voltage (V_{Umin})	V_6	4.0			V
Regulating current (V_{Umin}, V_{Reg}=4 V)	I_6			33	μA
Input impedance ($V_{max}f$=36 MHz)	Z_I		0.33/17		kΩ/pf
Input impedance ($V_{min}f$=36 MHz)	Z_I		1.5/0		kΩ/pf
Output voltage (f=36 MHz, V_R≤1 V (V_{max}) V_I=120 μV)	V_{rms}	1.1	2.0		V
Output voltage (f=36 MHz, V_R=4 V (V_{min}); f_{mod}=1 kHz, m=80%, k=5%)	V_{Qrms}		2.9		V
Input voltage (f=36 MHz, V_R≥4 V [V_{min}], f_{mod}=1 kHz, m=80%, k=5%)	$V_{Imax\ rms}$		240		mV
Voltage gain (f_m=36 MHz, Q_B=9)	$\frac{V_{Qrms}}{V_{Irms}}$		75		db
Voltage gain	$\frac{V_{Video}}{V_{Irms}}$		73		db
Control range (f=33 to 40 MHz)	$\frac{V_{Umax}}{V_{Umin}}$	55	60		db

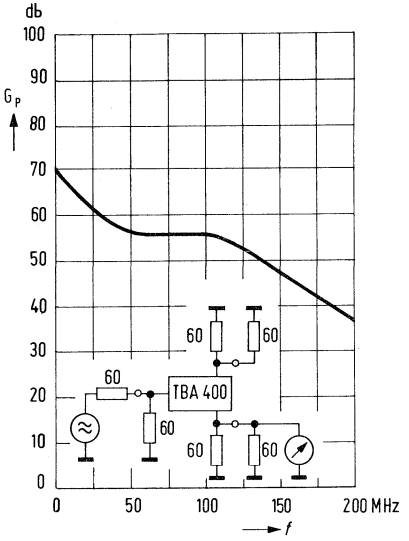
Test circuit



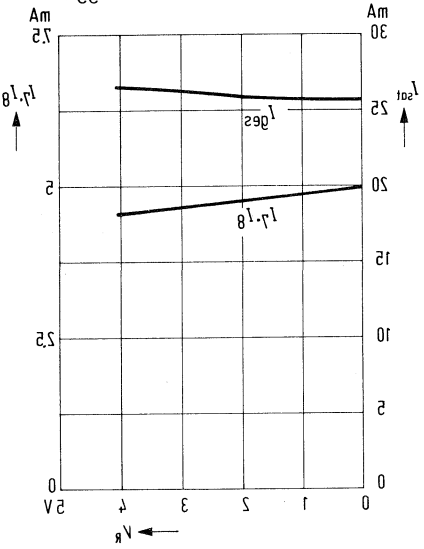
Application circuit for 39,2 MHz



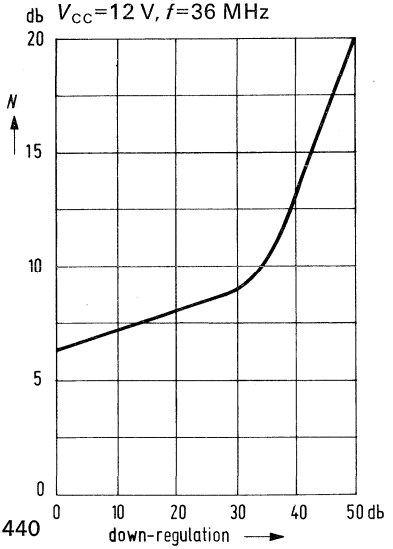
Power gain $G_p = f(f)$
V_{CC}=12 V, f=36 MHz, V_Q=16 mV
constant



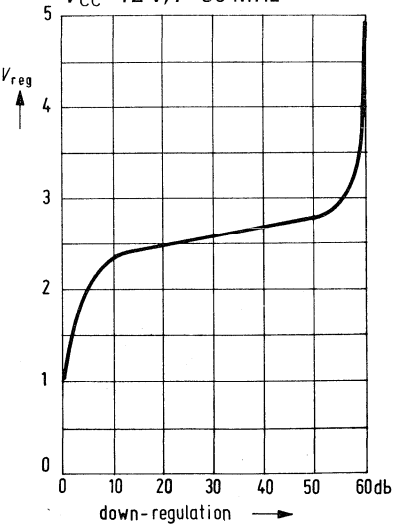
Total current requirement $I_{Sat} = f(V_R)$
Output currents $I_7/I_8 = f(V_R)$
V_{CC}=12 V



Noise N=f (down-regulation)
V_{CC}=12 V, f=36 MHz



Regulation-characteristic
$V_{Reg} = f$ (down-regulation)
V_{CC}=12 V, f=36 MHz



Ordering code

TBA 440 =Q67000–A282
TBA 440 Q=Q67000–A577 ■

TBA 440
TBA 440 Q

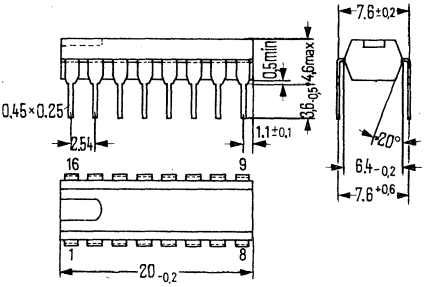
Gain-controlled video IF-amplifier with demodulator

This circuit comprises a high-gain regulated video-IF-amplifier, a controlled demodulator and two low-resistance video-outputs with positive and negative signal, as well as the complete clocked regulation and tuner regulation-delay.
For application in black and white and colour TV-sets.

- Complete video-IF in one integrated circuit
- Wide range of regulation with low noise and high levels of control
- High sensitivity
- Controlled demodulator – therefore minimum 1.07 MHz disturbances
- Low-resistance video-outputs
- Positive and negative BAS-signal
- Internal temperature stabilization

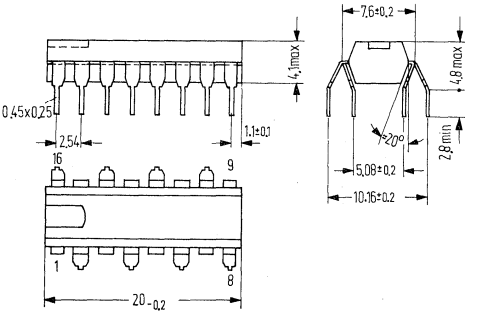
Package outlines

TBA 440



Plastic plug-in package 20 A 16 DIN 41866
16 pins (dual-in-line)
Weight approx. 1.2 g

TBA 440 Q



Plastic plug-in package 20 A 16 DIN 41866
16 pins (quad-in-line)
Weight approx. 1.2 g
■ Package not for new developments

Maximum ratings

Supply voltage	V_{CC}	15	V
Supply voltage (max. 1 min)	V_{CC}	16.5	V
Voltage at pin 5	V_5	20	V
Voltage at pin 4	V_4	5	V
Ambient operating temperature	T_{Amb}	–25 to +60	°C
System-temperature	T_{Sys}	125	°C
Power dissipation ($T_A \leq 55$ °C)	P_T	700	mW
Thermal resistance (system-air)	R_{ThSA}	100	°C/W
DC-resistance between pins 8 and 9	$R_{8\text{-}9}$	20	Ω

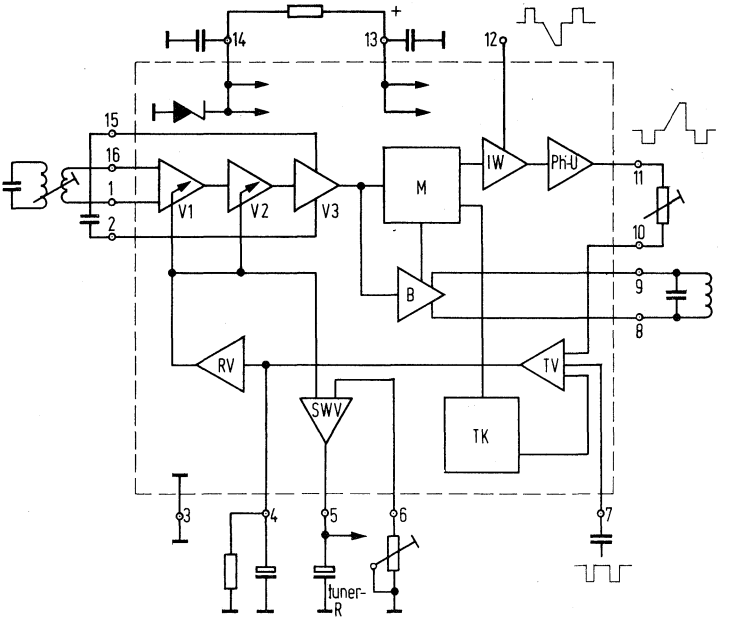
TBA 440
TBA 440 Q

Operating characteristics (T_{amb}=25 °C, V_{CC}=13 V, I_{14}=40 mA, unless stated otherwise)

		min	typ	max	
Range of operation	V_{13}	10	13	15	V
	I_{14}	30	40	50	mA
Current requirement (V_{13}=15 V)	I_{13}		18		mA
Operating voltage (I_{14}=40 mA, V_I=0)	V_{14}		6		V
DC-voltage at output (V_I=0)	V_{11}		6		V
DC-voltage at output (V_I=0)	V_{12}		2		V
Regulating current for tuner pre-stage (10 db above start of tuner regulation, $V_5 \geq 2$ V)	I_5	3			mA
IF regulating voltage for V_{max}	V_4	0		0.5	V
IF regulating voltage for V_{min}	V_4	2.5		5	V
Clock-pulse voltage	$-V_7$	2		5	V_{pp}
Resistance for output voltage V_{11}=3 V_{pp}	$R_{10\text{-}11}$		3		kΩ
Output current to ground	I_{11}, I_{12}			5	mA
Output current to pos. supply	I_{11}, I_{12}			−1	mA
Input resistance at V_{max}	$Z_{1\text{-}16}$		1.8/2		kΩ/pf
Input resistance at V_{min}	$Z_{1\text{-}16}$		1.9/0		kΩ/pf
Input voltage[1]) for V_{11}=2 V_{pp}	V_I		100		μV
Input voltage[1]) for V_{11}=3 V_{pp}	V_I		150		μV
Video bandwidth	B_{Video}		9		MHz
Range of regulation	ΔV_u	50	55		db
Intermodulation-separation (1.07 MHz) relative to colour-carrier[2])	a		55		db

[1]) V_{IN} effective synchronous pulse level measured across 60 Ω, fed-in with transformer 3 : 5.
[2]) Measured with demodulator-capacitor 22 pf at any down-regulation. ΔV_{11}=0.3 to 1.5 V_{pp} (yellow). IF colour-carrier level a_{CC}=−2 db; sound carrier level −24 db, relative to picture-carrier.

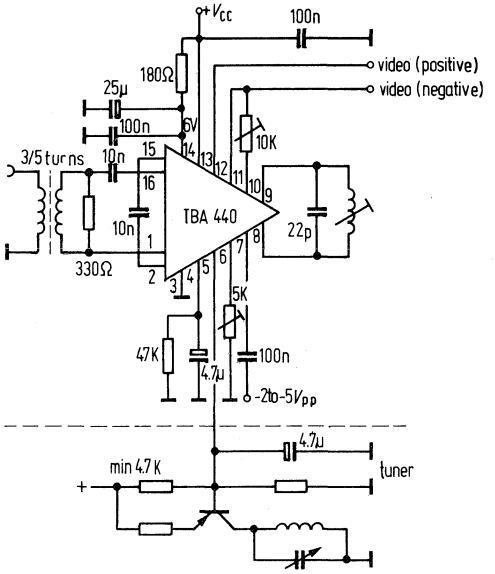
Block-diagramm



V1. V2 IF regulating stages
V3 IF amplifier stage
M Mixer
IW Impedance buffer
Ph-U. Phase inverter
B Limiter-amplifier
RV Regulating voltage amplifier
SWV Threshold-amplifier
TK Temperature compensation
TV Clock amplifier

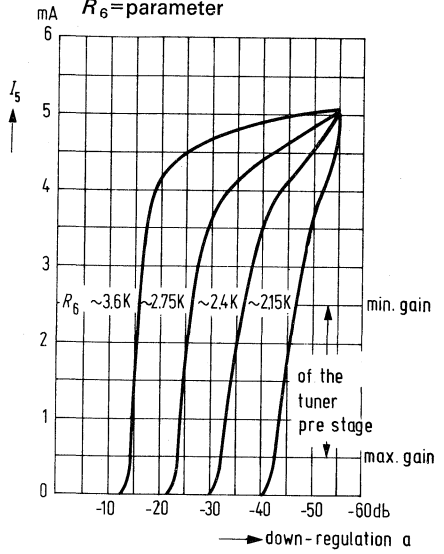
TBA 440
TBA 440 Q

Test circuit

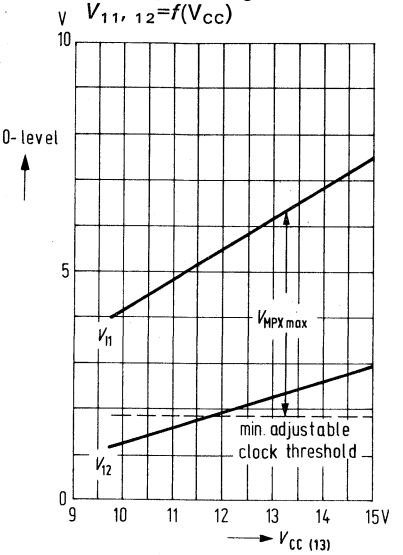


1, 16	IF-input
2, 15	DC-feedback
3	Ground
4	Regulating voltage filter
5	Delayed tuner regulating voltage
6	Start of the delayed tuner regulation control
7	Line return pulse(–2 to–5 V_{pp} negative)
8, 9	Parallel circuit 38.9 MHz
10	Start of regulation control
11, 12	Video output negative / positive
13	V_{CC} (10 to 15 V)
14	I_{14} (30 to 50 mA, internally stabilized to 6 V)

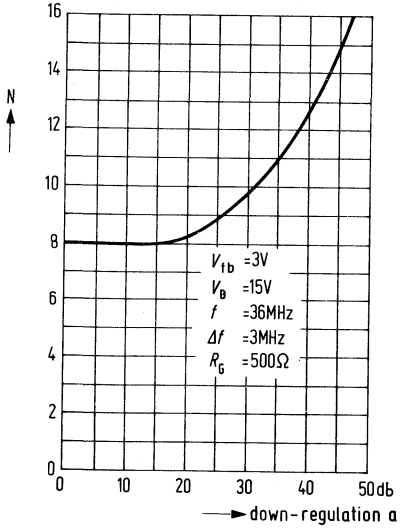
Tuner regulating current $I_5=f(a)$
R_6=parameter



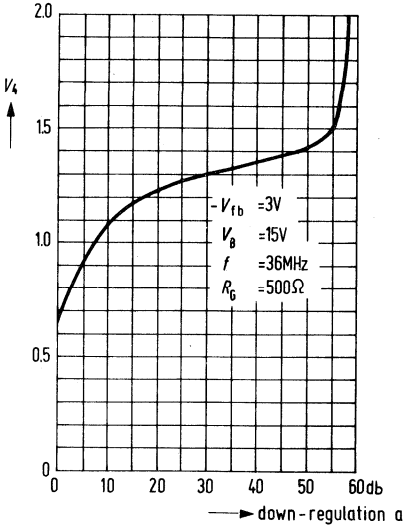
DC output voltage without carrier
$V_{11,\ 12}=f(V_{CC})$



Noise behaviour N=f(a)
(video freq. measured)–V_{fb}=3 V,
V_{CC}=15 V, f=36 MHz, Δf=3 MHz, R_G=500Ω



Regulating voltage curve $V_4=f(a)$
–V_{fb}=3 V, V_B=15 V, f=36 MHz,
R_G=500 Ω



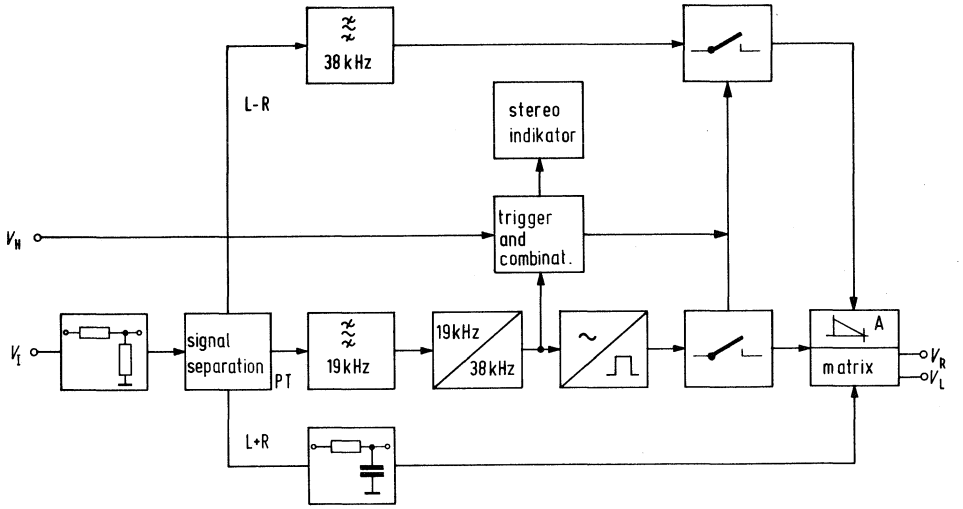
TBA 450

Ordering code
TBA 450: Q62702-A283

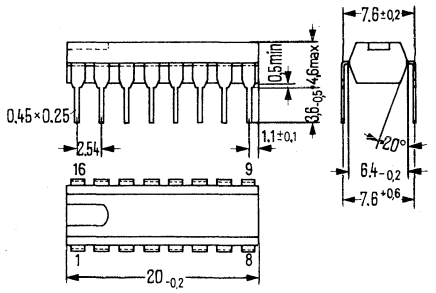
Stereo decoder

Integrated matrix stereo decoder. Automatic mono-stereo switching and a manual stereo-mono switching (enforced mono). Indicator lamp driver up to 100 mA.

Block diagram



Package outlines

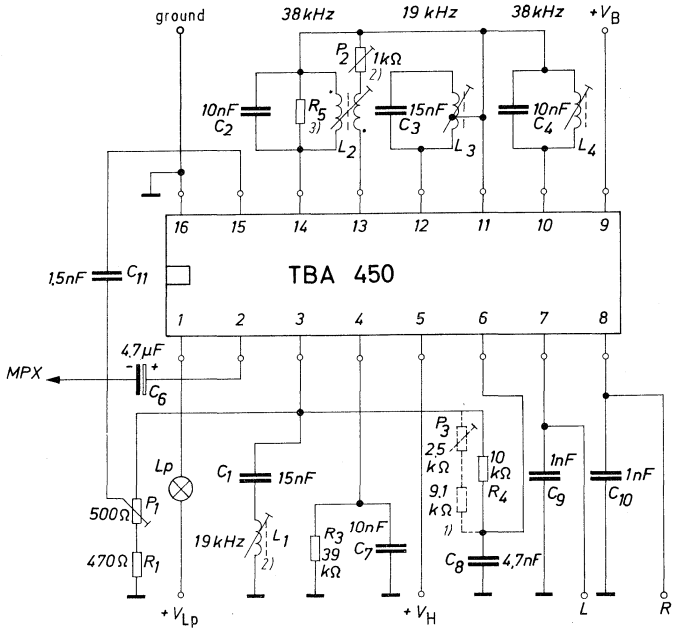


Weight approx. 1.2 g
Dimensions in mm

Plastic plug-in package 20 A 16 DIN 41 866 (16 pins)

Maximum ratings		TBA 450	
Supply voltage	V_{CC}	18	V
Auxiliary voltage	V_H	3	V
Lamp voltage	V_{Lp}	18	V
Current for stereo indicator	I_1	100	mA
Total power dissipation	P_{tot}	650	mW
Storage temperature	T_S	–40 to 125	°C
Ambient operating temperature	T_{amb}	0 to 70	°C
Range of operation	V_{CC}	4.5 to 18	V
Operating characteristics (T_{amb}=25°C, V_{CC}=15 V)			
Total current requirement (I_1=100 mA)	I_{CC}	20	mA
Input resistance	R_I	>25	kΩ
Output resistance each channel	R_Q	1.7 or 4.5	kΩ
MPX-input voltage	V_{Ipp}	<2	V
Output voltage each channel	V_{Qpp}	2[1])	V
Saturation voltage of the lamp driver (I_1=100 mA)	$V_{C\,Esat}$	<1.5	V
Distortion factor (f_{AF}=1 kHz; V_{Qpp}=350 mV)	k	<0.5	%
Auxiliary voltages for the switching of mono to stereo	V_H	>0.71	V
stereo to mono	V_H	<0.47	V
Attenuation at 19 kHz	a_{pT}	>40	db
Attenuation at 38 kHz	a_{pT}	>40	db
Attenuation at 67 kHz (SCA signal) without additional circuit	a_{SCA}	>35	db
Cross-talk attenuation			
f_{AF}≤6.3 kHz	a_{ct}	>36	db
f_{AF}≤10 kHz	a_{ct}	>30	db
Balance	a_{bal}	<0.2	db

[1]) at R_Q=4.5 kΩ



1) For an easier total-tuning with improved cross-talk attenuation (regarding the entire frequency range) it is recommended to use a combination of 9.1 kΩ resistor and 2,5 kΩ potentiometer (P 3) in series in place of the fixed resistor R_4.

2) In case of reduced requirements the 19 kHz trap consisting of L_1 and C_1 may be omitted and potentiometer P_2 be replaced by a fixed resistor of 220 Ω.

3) The value of damping resistor R_5 depends on the dc-resistance of coil L_2. For an overall Q=30 of the tank circuit, R_5 will be approximately 3 kΩ.

Ordering codes

TBA 460: Q67000-A284
TBA 460 Q: Q67000-A579

TBA 460
TBA 460 Q

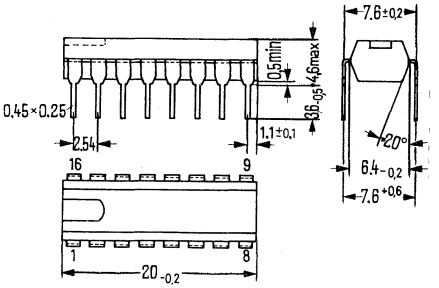
AM/FM-IF-and AF-amplifier

Combined AM/FM-IF amplifier with AF pre-amplifier. A high level of integration and excellent performance characteristics of both amplifiers permit a universal application in battery- and ac-operated receivers.

RF-portion: good control characteristics
for AM-operation,
good limiting characteristics
for FM-operation.

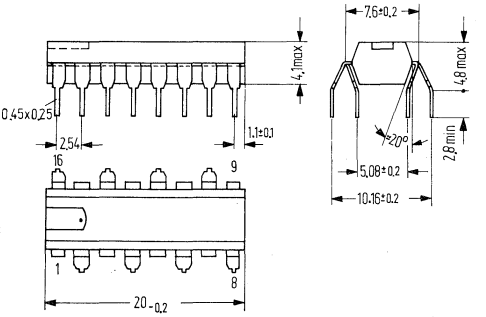
AF-portion: good frequency characteristics 30 Hz–70 kHz,
high driver-current 130 mA,
P_Q (with AD 161; AD 162)=10 W
low distortion, up to 8 W k<1%

Package outlines



Plastic plug-in package, 16 pins
20 A 16 DIN 41866
(DIL=dual-in-line)

Weight approx. 1.2 g
Dimensions in mm



Plastic plug-in package (16 pins)
20 A 16 DIN 41866 (similar)
(Q_{IL}=quad-in-line)

Maximum ratings

	TBA 460 TBA 460 Q	
Supply voltage IF-portion	V_{CCIF} 12	V
Supply voltage AF-portion	V_{CCAF} 18	V
Ambient operating temperature	T_{amb} 0 to 70	°C
Storage temperature	T_S –40 to 125	°C
Range of operation, IF-portion	V_{CCIF} 5 to 12	V
Range of operation, AF-portion	V_{CCAF} 5 to 18	V

TBA 460
TBA 460 Q

Operating characteristics (V_{CC}=9 V, T_{amb}=25 °C)

		min	typ	max	
Total current (no signal)	I_{sat}		29		mA
Partial current (no signal)	I_{11}	8	11	14	mA
IF-portion, AM-operation: (f_{IF}=460 kHz, f_{AF}=1 kHz, m=50%)					
Stabilized voltage	V_{16}	2.8		2.95	V
Voltage gain	G_v		90		db
Range of regulation ($\Delta V_{AF} \leq 10$ db)	$\triangle G_v$		60		db
Start of regulation[1])	V_I		15		μV
Feedback voltage (V_I=15 μV)	$-V_{fb}$		200		mV
AF-output voltage (V_I=15 μV)	V_{AF}		120		mV
Input voltage starting overdrive (k=10%)	V_{OD}		25		mV
Input voltage starting pre-stage regulation	V_I		0.9		mV
Pre-stage regulation voltage ($V_I \leq 200$ μV)	V_{15}	2.8			V
Pre-stage regulation voltage ($V_I \geq 3$ mV)	V_{15}			0.5	V
IF-portion, FM-operation (f_{IF}=10.7 MHz, f_{AF}=1 kHz, $\Delta f = \pm 75$ kHz)					
Voltage gain	G_v		86		db
Input voltage for start of limiting[2])	V_I		500		μV
AF output voltage at limiting condition	V_{AF}		350		mV
AM suppression factor (FM: $\Delta f = \pm 75$ kHz; AM: m=50%) at limiting condition	V_{FM}/V_{AM}		50		db

Start of regulation is defined as that input voltage for which $\frac{\Delta V_I}{\Delta V_{AF}} = \frac{10}{3}$ db

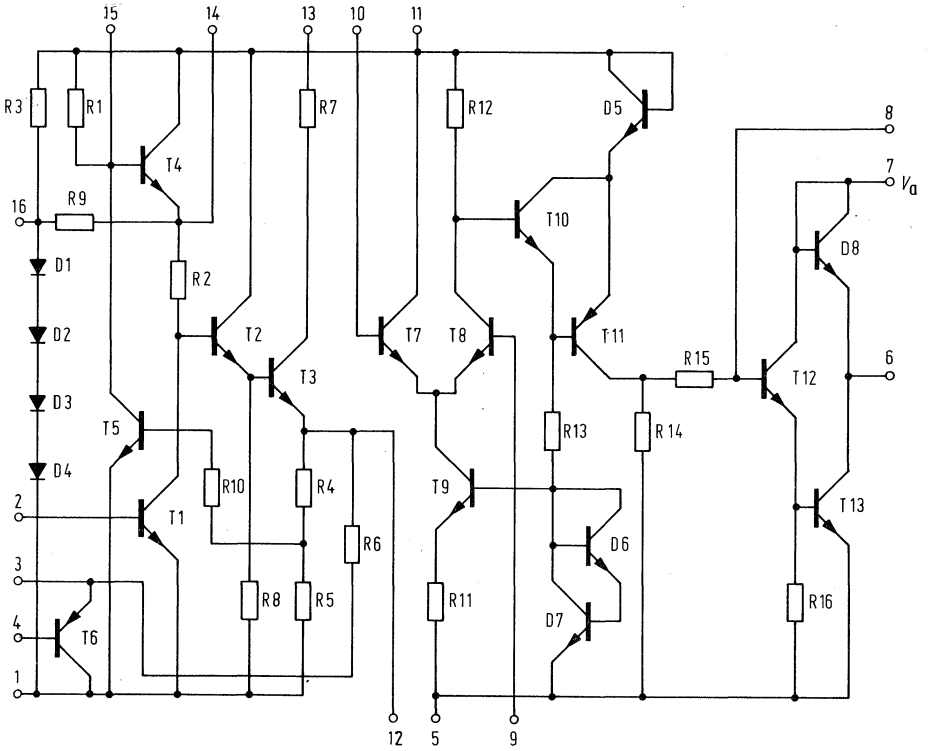
Start of limiting is defined as that input voltage for which the AF output voltage is down 3 db. Reference potential is V_I=100 mV.

TBA 460
TBA 460 Q

AF-portion

		min	typ	max	
Current requirement	$I_{7/6}$		22.5		mA
Diode voltage	$V_{7/6}$		0.7		V
Quiescent voltage gain	G_{vo}		72		db
Output voltage (G_v=45 db; k=10%)	V_{Qrms}		3.2		V
Distortion factor (V_{Qrms}=2 V, G_v=45 db, R_G=1 kΩ)	k		0.3		%
Separation of foreign voltage (V_Q=1 V)	S_{FV}	60			db
Voltage/frequency characteristic (±3 db)	$\frac{V_Q}{V_{Q1ooo}}$		30 Hz to 70 kHz		
Maximum permissible collector current T 13	I_{max}		130		mA
Noise voltage (referred to the input, R_g=1 kΩ)			2.5		μV

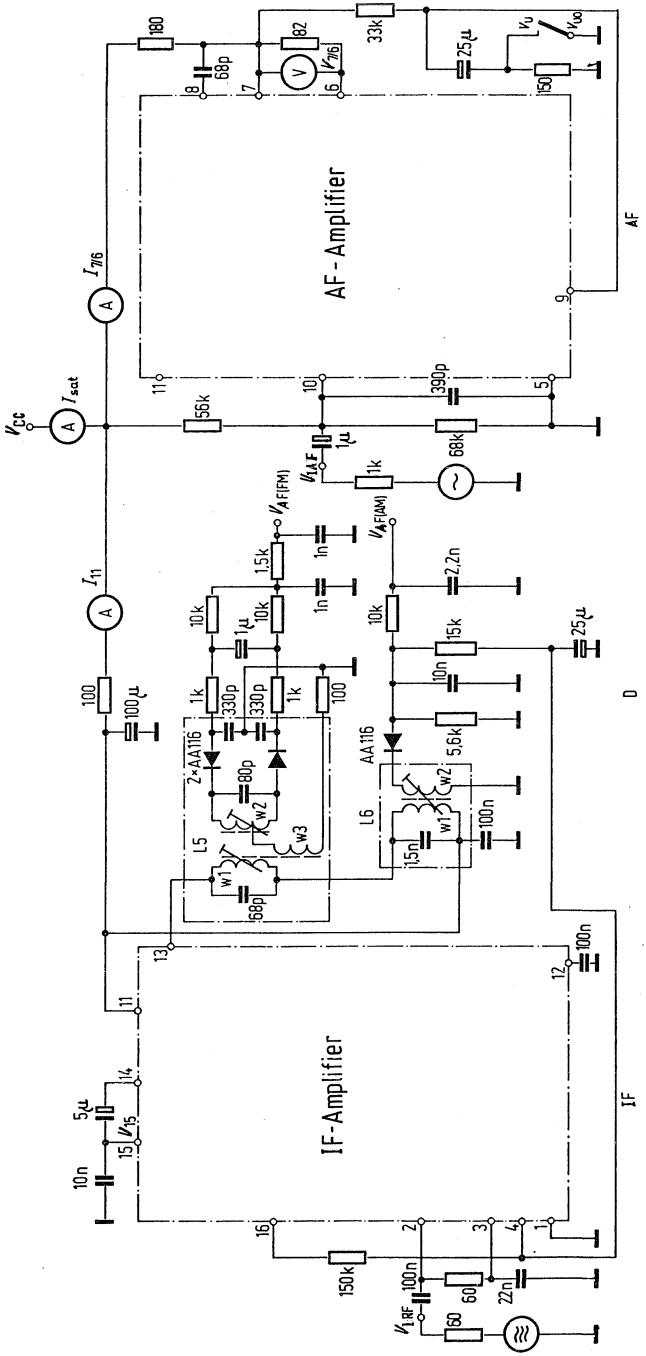
Circuit diagram



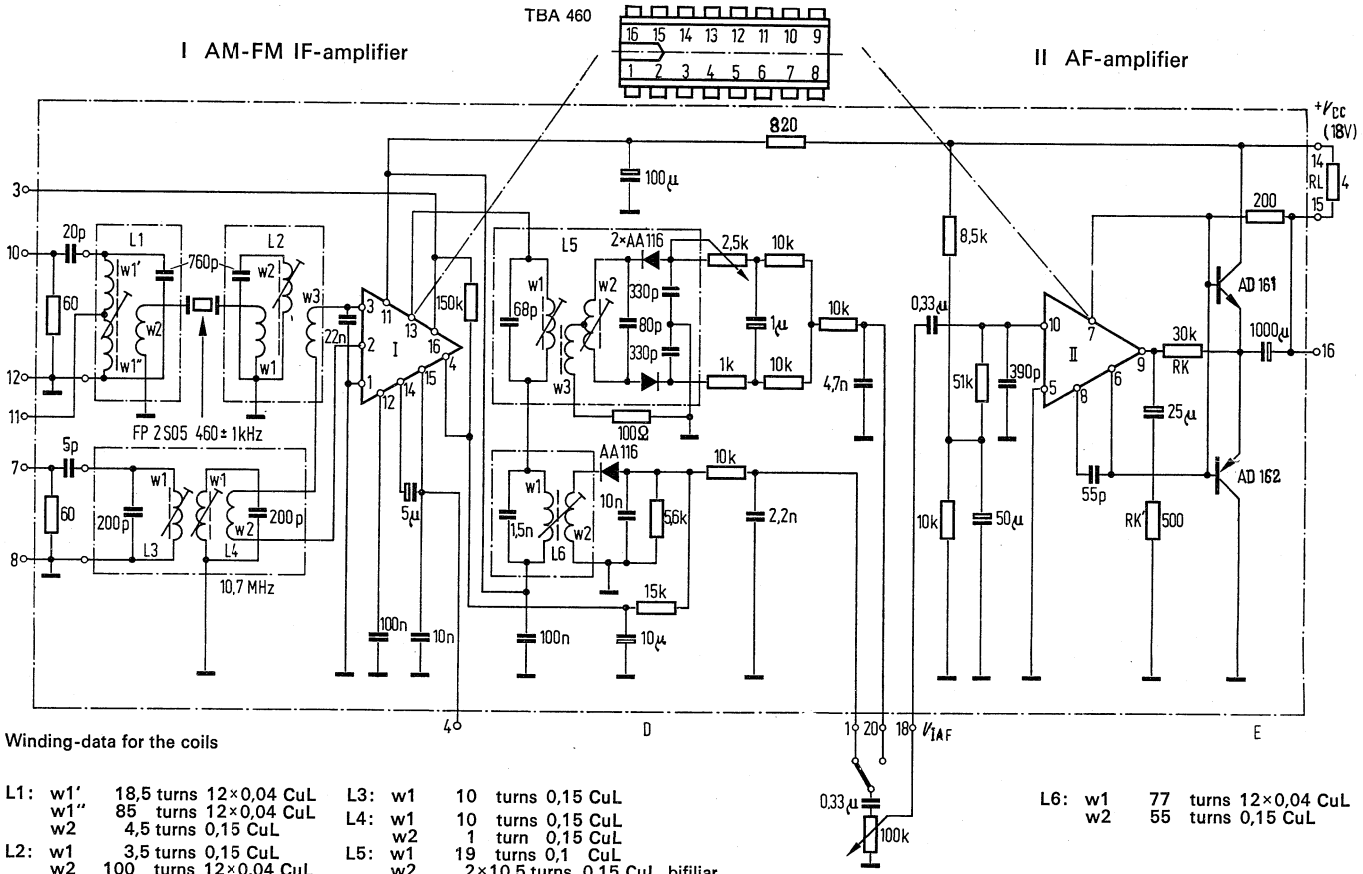
If the AF-portion is used separately, pin 5 should be connected to pin 1.

TBA 460
TBA 460 Q

Test circuit



Application-example, 10 Watt output power



Winding-data for the coils

L1:	w1'	18,5 turns	12×0,04 CuL	L3:	w1	10 turns	0,15 CuL	
	w1"	85 turns	12×0,04 CuL	L4:	w1	10 turns	0,15 CuL	
	w2	4,5 turns	0,15 CuL		w2	1 turn	0,15 CuL	
L2:	w1	3,5 turns	0,15 CuL	L5:	w1	19 turns	0,1 CuL	
	w2	100 turns	12×0,04 CuL		w2	2×10,5 turns,	0,15 CuL, bifiliar	
	w3	7 turns	0,15 CuL		w3	3 turns	0,15 CuL	

L6:	w1	77	turns 12×0,04 CuL
	w2	55	turns 0,15 CuL

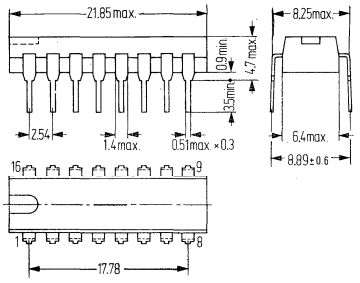
TBA 920

Ordering code
TBA 920 = Q67000–A566

Horizontal combination

for black-and-white and colour-TV sets with any kind of H-deflection.
The monolithic horizontal-combination circuit TBA 920 comprises the following units:
Pulse separation stage;
Noise strobing input for the suppression of noise signals having the same polarity as the information signal;
Line oscillator based on the threshold-switch principle; Phase comparison I between synch.-pulse and oscillator;
Time-constant and gain switching (also for the connection of a video-recorder);
Phase comparison II between line-return and horizontal strobe and output stage for the control of a thyratron or a transistor drives stage.

Package outlines



Dimensions in mm
Weight approx. 1.2 g

Plastic plug-in package (16 pins) similar to 20 A 16 DIN 41866

Maximum ratings:

Supply voltage	V_{CC}	13.2	V
Total power dissipation	P_{tot}	600[1])	mW
Currents	I_2	20	mA
	I_{2M}	200[2])	mA
	$I_{5M}, I_7, I_{8M}, I_{9M}$	10 each	mA

[1])[2]) Footnotes see page 460

Voltages	V_3	0 to 13.2	V
(measured with respect to ground potential 16)	V_8	−12	V
	V_{10}	−0.5 to 12	V
Ambient operating temperature	T_{amb}	−20 to +60	°C
Storage temperature	T_S	−25 to +125	°C

Operating characteristics (V_{CC}=12 V, T_{amb}=25 °C) voltages referred to ground 16

Inputs

Pulse separation stage

Input current	$I_{8M\,min}$	10	μA
Input voltage (BAS)	$V_{8MM\,min}$	0.5	V
Input leakage current	$I_{8\,max}$	1	μA

Noise strobing input

Input current	$I_{9M\,min}$	30	μA
Input voltage	V_9	0.7	V
Input resistance	$R_{9\text{-}16}$	0.2	kΩ

Return pulse

Input current	$I_{5M\,min}$	50	μA
Input voltage	V_{5M}	±700	mV
Input resistance	R_6	400	Ω

Outputs

Synch.-pulse (pos.)

Output voltage	V_{7MM}	10	V
Output resistance			
Rise-edge	$R_{7/16}$	≈50	Ω
Fall-edge	$R_{7/16}$	2.2	kΩ

Control pulse

Output voltage	V_{2MM}	10	V
output resistance	R_{i2}	2.5; 15[3]) low res.	Ω
Control pulse width	T_2	0.2 to 0.5[4])	period

Oscillator

Threshold	V_{14}	5 to 8	V
Charging/discharging current	I_{14}	$\pm I_{15}$	
Current source voltage	V_{15}	3.1	V
Current source current	I_{15}	0.94	mA
($R_{15\text{-}16}$=3.3 kΩ)			
(for fine-tuning of the oscillator I_{15} is varied)			

Pulse former

Input voltage	V_3	6 to 8	V
(for max. variation of control pulse duration)			
Input current	I_3	2	μA

Phase comparison I (synch.-pulse oscillator)

Range of regulating voltage	V_{12}	0.8 to 5.5	V
Regulating currents (V_{10}>4.5V) with V_6>1.5 V	I_{12M}	±2	mA
Regulating currents (V_{10}<2 V) with V_6>1.5 V	I_{12M}	± 6	mA
Output resistance			
(V_{12}=0.8–5.5 V)	R_{i12}	high res. (currentsource circuit)	
(V_{12}=<0.8 V; >5.5 V)	R_{i12}	low res. (about 2 kΩ) for limiting of the regulation-range	

Phase comparison I-switching

Output voltage	V_{11}	3.1	V
Internal resistance			
(V_{10}<2 V)	R_{i11}	2	kΩ
(V_{10}>4.5 V)for I_{11}<±1 mA	R_{i11}	150	Ω

[3]), [4]) footnotes see page 460

The switching of R_{i11} and I_{12} is performed automatically through an internal coincidence circuit (coincidence of V_{7M} and V_{5M} and an external RC-circuit connected to pin 10) or through a direct control at pin 10.

Switching voltages			
for R_{i11}=2 kΩ	V_{10}	<2	V
R_{i11}=150 Ω	V_{10}	>4.5	V
Switching currents			
for R_{i1}=2 kΩ (V_{10}=2 V)	I_{10}	120	μA
R_{i1}=150 Ω (V_{10}=4.5 V)	I_{10}	80	μA
with synch. pulses at pins 7 and 8, pin 10 not connected to ext. components			
Phase comparison II (line return-pulse oscillator)			
Range of regulating voltage	V_4	2 to 9	V
Regulating current	I_{4M}	±0.7	mA
output resistance	R_{i4}	high res. (currentsource circuit)	
Operating characteristics, circuit shown on page 461 (CCIR-standard) (V_{CC}=12 V; Tamb=25°C)			
Total current requirement (I_2=0)	I_1	36	mA
Inputs			
Video signal (BAS)			
Input signal (pos. synch.-pulse)	V_{8MM}	1 to 7 (typ. 3 V)	V
Input clock signal	$_{R8M}$	0.2	mA
Noise pulse provisions			
Input noise signal voltage	V_{9M}	>0.7	V
Input noise signal current	I_{9M}	0.03 to 10	mA
Input impendance	$R_{9\text{-}16}$	200	Ω

Return pulse

Input voltage	V_{5M}	±1	V
Input current	I_{5M}	1	mA
Input impedance	$R_{6\text{-}16}$	400	Ω

Outputs

synch.-pulses (pos.)

Output voltage	V_{7M}	10	V
output resistance			
rise edge	R_{i7}	≈50	Ω
fall edge	R_7	2.2	kΩ
additional output load	R_{7add}	>2	kΩ

Control pulse

Output voltage	V_{2MM}	10	V
Mean output current	I_{2max}	20	mA
Peak output current	$I_{2M\,max}$	200[2])	mA
Internal output resistance	R_{i2}	2.5; 15[3])	Ω
Control pulse width (synchr. condition) (switching delays of the H-output stage are automatically compensated through phase-comparsion)	f_2	12 to 32[4])	µs
Permissible delay between the rise-edge of the control pulse and the rise-edge of the return-pulse	t_{Dtot}	0 to 15	µs

Oscillator

Oscillator frequency unsynchronized ($R_{15\text{-}16}$=3.3 kΩ)	f_o	15.625[5])	kHz
Tolerance of osc.-frequency	$\Delta f/f_o$	<±10[6])	%
Change of frequency with decrease of the supply voltage to V_1 ≥4 V	$\Delta f/f_{12v}$	<±10	%
Frequency adjustment gain	$\Delta f/\Delta I_{15}$	16.5	Hz/µA
Adjustment range of the network shown in the circuit on page 454	$\Delta f/f_o$	±15	%

[2]), [6]) footnotes see page 460

Phase comparison I (between synch. pulse and oscillator)

Range of regulating voltage	V_{12}	0.8 to 5.5	V
Regulation sensitivity			
a) coincidence of synch.-pulse and line return pulse or $V_{10}>4.5$ V	$\Delta f/\Delta t$	1	kHz/μs
b) no coincidence or $V_{10}<2$ V	$\Delta f/\Delta t$	3	kHz/μs
Catch or retain range	Δf	± 1	kHz
Catching time for $\Delta f/f_0=\pm$ 3% (Δf=0.47 kHz)	t	≈ 20	μs
Time duration for switching from a higher sensitivity of regulation to a low sensitivity, after catching	t	20	μs

Phase comparison II (between line return pulse and osc.)

Permissible delay between the rise-edge of the control pulse and the rise-edge of the return pulse	t_{Dtot}	0 to 15	μs
Static regulation-error	$\Delta t/\Delta t_D$	<0.5[7])	%
output current during return-pulse	I_4	± 0.7	mA

Overall phase condition

Phase distance from rise-edge of synch.-pulse to center of return pulse	t	4.9[8])	μs
Tolerance of phase-condition	Δt	<1	μs
Voltages for T_2=12 to 32μs	V_3	6 to 8	V
Adjustment-gain	$\Delta T_2/\Delta V_3$	10	μs/V
Input current	I_3	<2	μA

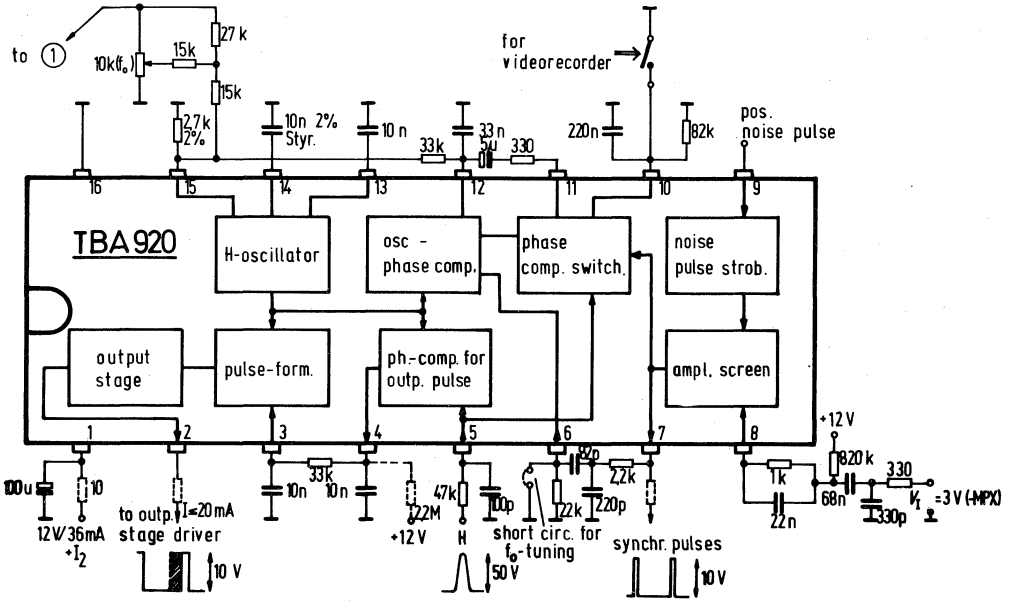
The adjustment of the overall phase condition, and consequently of the rise-edge of the control pulse, is performed automatically through phase comparison II or through a dc-voltage put on pin 3.

[7]), [8]) footnotes see page 460

Footnotes

1. At turn-on 800 mW.
2. The maximum value of mean output current must not be exceeded.
3. R_{i2} depends on the switching-state and the direction of the output current; R_{i2}=2.5 Ω is valid only for $V_{2\text{-}16}$=+10.5 V and a current load (i. e. through a resistor) to pin 16.
4. Adjustment of the control pulse width is done by shifting the rise-edge (adjustable through $V_{3\text{-}16}$=6 to 8 V).
5. For other line-standards the frequency is adjusted through an appropriate choice of $C_{14\text{-}16}$.
6. Variations in external component values not included.
7. Regulation error is the remaining deviation from the intended position (rise-edge synch. pulse and center of return pulse) resulting from variations in the switching times of the output stage.
8. This nominal phase position is based on a delay line of Δt=500 ns in colour TV-sets between the input signal of the pulse-separation stage and the control voltage of the colour picture tube. If the pulse separation stage is connected behind the delay line or if this is not present, as in the case of black-and-white TV sets, the nominal phase position can be achieved using $C_{5\text{-}16}$= 560 pf.

Principle circuit arrangement of the horizontal-combination TBA 920



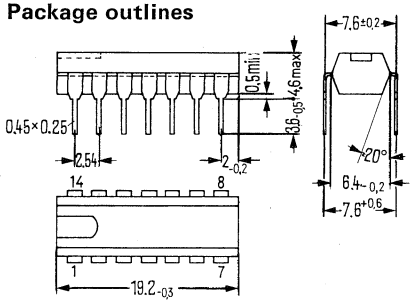
S 041 P
similar to TBA 120

Ordering code
S 041 P: Q67000-A529

FM-IF-amplifier with demodulator

The S 041 P is a symmetrical six-stage amplifier with symmetrical coincidence-demodulator for the amplification, limiting and demodulation of frequency-modulated signals. It is particularly well suited for sets where a low current consumption is of importance, or where major supply voltage fluctuations occur.
Pin connections correspond to the well known TBA 120. However, pin 5 is not connected to external components. The S 041 P is especially suited for applications in narrow-band FM-systems (455 kHz) and in VHF-IF (10.7 MHz).

Package outlines



Dimensions in mm
Weight approx. 1.1 g

Plastic plug-in package 20 A 14 DIN 41866 (14 pins)

Maximum ratings

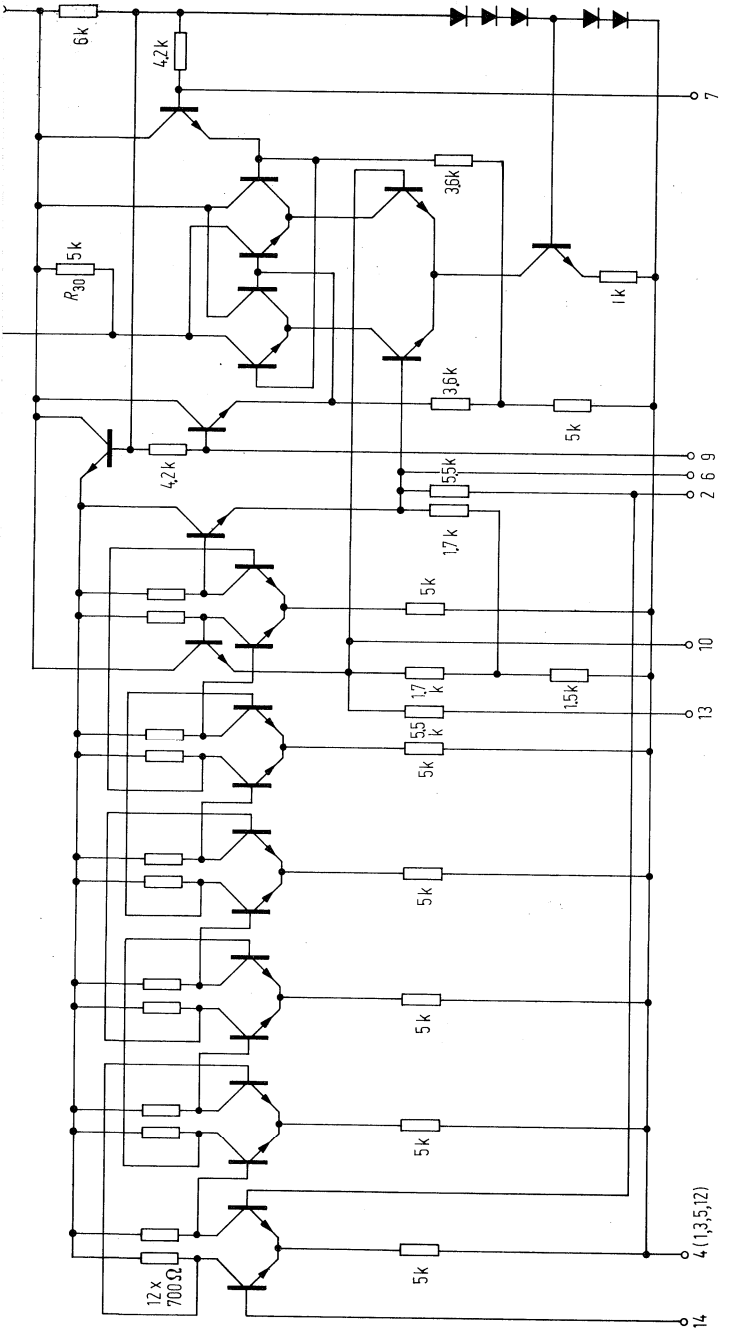
Supply voltage	V_{CC}	14	V
Range of operation	V_{CC}	4 to 14	V
Frequency range	f	0 to 35	MHz
Ambient operating temperature	T_{amb}	–25 to +85	°C
Storage temperature	T_S	–40 to +125	°C

Operating characteristics (V_{CC}=8 V, T_{amb}=25 °C)

Current requirement	I_{CC}	5	mA
AF output voltage (k=1%, f=10.7 MHz, Δf=±75 kHz or 455 kHz±5 kHz)	V_{AFrms}	200	mV
Input voltage starting limiting (pin 14) at 10.7 MHz	V_I	40	μV
at 455 kHz	V_I	15	μV
AM suppression (f=10.7 MHz, V_I=10 mV, Δf=±75 kHz, m=30%, f_{mod}=1 kHz)	a	60	db
IF-Voltage gain at 10.7 MHz	G_V	63	db .

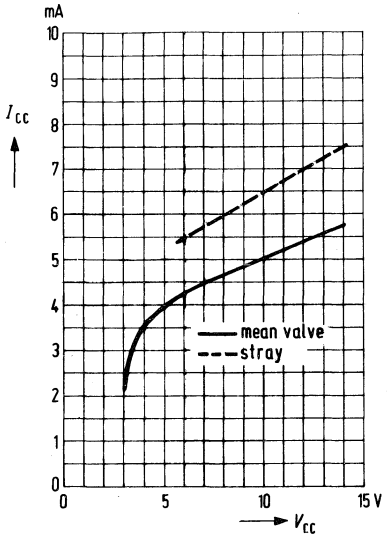
S 041 P

Circuit diagram
S 041 P

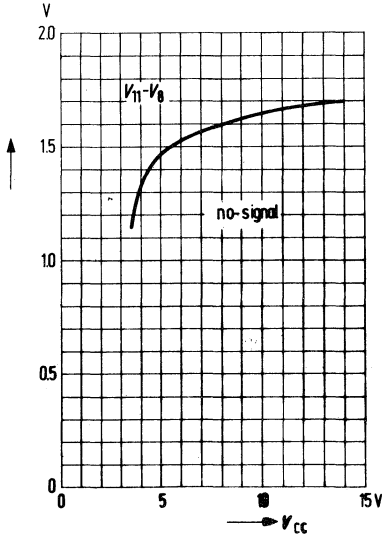


S 041 P

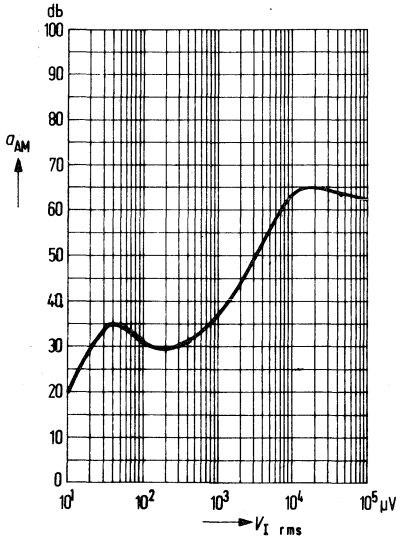
Current requirement $I_{CC}=f(V_{CC})$



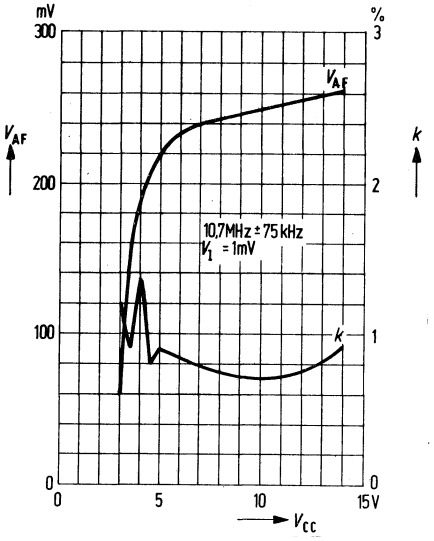
Voltage drop at AF load resistance
$V_{11/8}=f(V_{CC})$



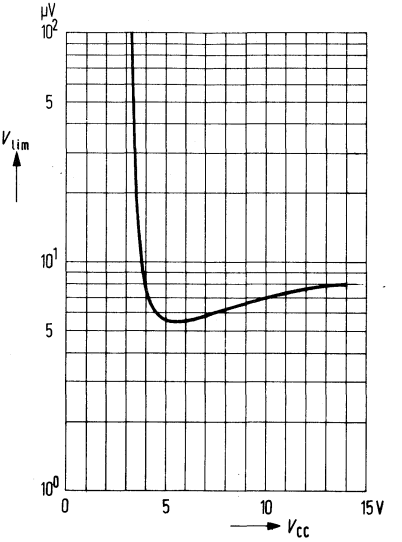
AM-Suppression $a_{AM}=f(V_{I\,rms})$



AF-output voltage $V_{AF}=f(V_{CC})$
Distortion factor $k=f(V_{CC})$

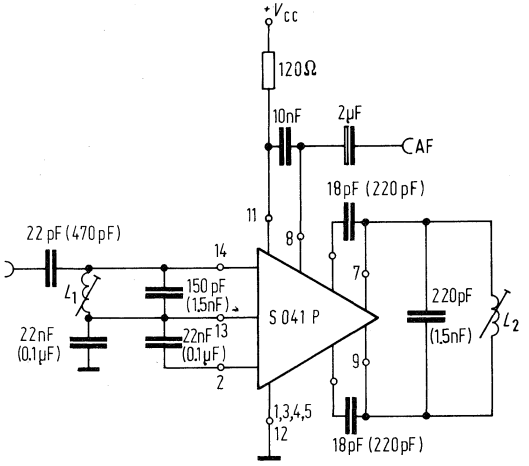


Start of limiting $V_{lim}=f(V_{CC})$
f=10.7 MHz, $\Delta f=\pm 75$ kHz, f_{mod}=1 kHz



S 041 P

Application circuit for 10,7 MHz (UHF-FM-ZF)
and 455 kHz (narrow-band FM)



Values in brackets for 455 kHz (narrow-band FM)

Coils	10.7 MHz	455 kHz
L_1	15 Wdg/0.15 CulS	71.5 Wdg/12×0.04 CulS
L_2	12 Wdg/0.25 CulS	71.5 Wdg/12×0.04 CulS
Kit	D 41-2165	D 41-2393 (Vogt Co.)

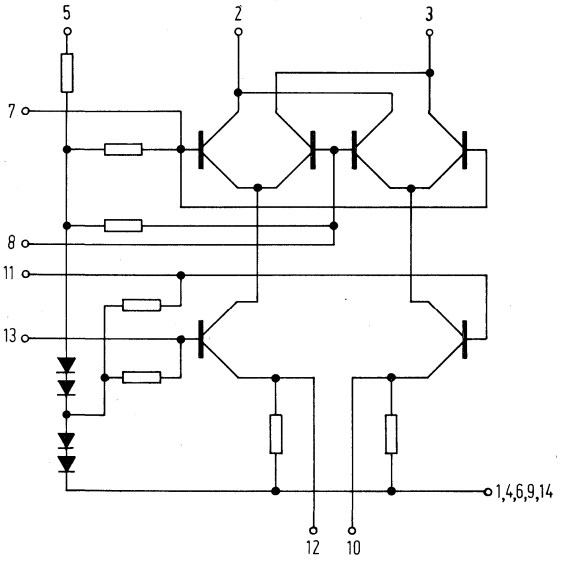
Ordering code
S 042 P: Q67000-A335

S 042 P

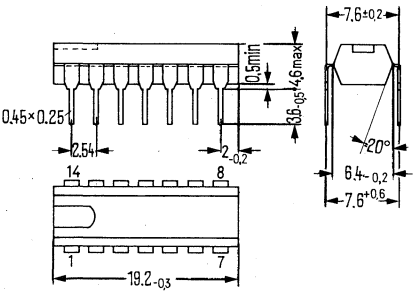
Mixer

The S 042 P is a universally applicable symmetrical mixer for frequencies up to 200 MHz. It can be driven from an external source or from the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer-applications in receivers, converters and demodulators for AM and FM, the S 042 P can be used as an electronic polarity-switch, multiplier etc.

Circuit diagramm



Package outlines



Plastic plug-in package, 14 pins
20 A 14 DIN 41866
Weight approx. 1.1 g, dimensions in mm

S 042 P

Maximum ratings

Supply voltage	V_{CC}	14	V
Ambient operating temperature	T_{amb}	–15 to +70	°C
Storage temperature	T_S	–40 to +125	°C
Range of operating supply voltage (pins 2; 3; 5)	V_{CC}	4 to 14	V

Operating characteristics (V_{CC}=10 V, T_{amb}=25 °C)

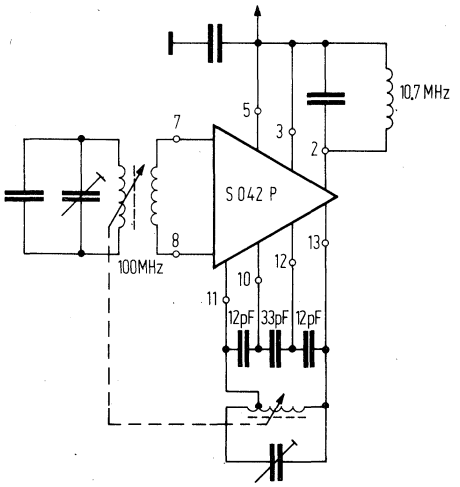
Current requirement	$I_{sat}=I_2+I_3+I_5$	1.9	mA
Output current	I_2	500	μA
	I_3	500	μA
Supply current	I_5	900	μA
Breakthrough voltage	V_2 (I_{11}=10 μA)	> 25	V
	V_5 (I_{12}=10 μA)	> 25	V
Output capacity	$C_{2\text{-}M}$; $C_{3\text{-}M}$	6	pf
Mixing-gain	$S=I_2/V_{7\text{-}8}=I_3/V_{7\text{-}8}$	5	mS
Noise figure (f=100 MHz; R_g=240 Ω)	N	7	db

A galvanic connection between pins 7 und 8 and pins 11 and 13 through coupling-windings is recommended.

Between pins 10 and 14 (ground) and between 12 and 14 a resistance of at least 200 Ω may be connected to increase the currents and therefore the gain. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this connection to pin 14 must be at least 100 Ω. Depending on the construction of the circuit a capacitor (10 to 50 pf) may be required between pins 7 and 8 to prevent oscillations in the VHF range.

Application-example for S 042 P

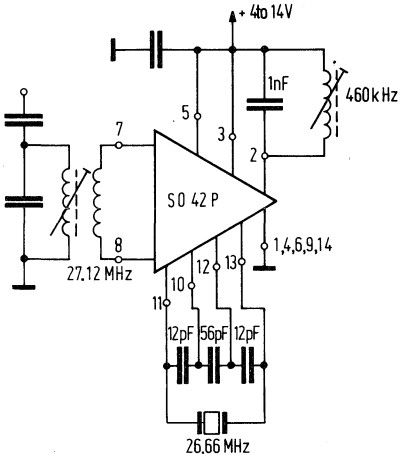
VHF-mixer with inductive tuning



S 042 P

Application-example for S 042 P

Mixer for remote-control receivers, self-oscillating



When using a harmonic-frequency quartz crystal, an appropriate inductance should be connected between pins 10 and 12 to prevent oscillation at the basic frequency.

Ordering code

SAS 560=Q67000–S11
SAS 570=Q67000–S13

SAS 560
SAS 570

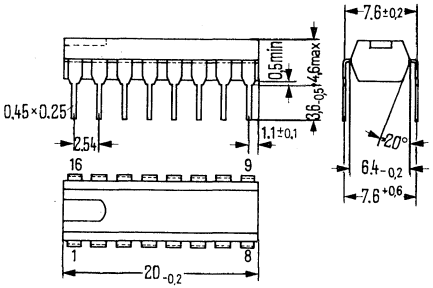
Sensitive switching-amplifier for touch-keys

Preliminary data

The integrated circuit SAS 560 and SAS 570 are especially well suited for an application in radio- and TV-sets, as well as in elevators, to perform touch-controlled switching functions.
When an amplifier is switched on, the voltage at pin 7 (i.e. 30 V, highly stabilized) is put on the corresponding output (pins 3, 4, 5 or 6). Simultaneously voltage V_{CC2} is switched to pins 15, 13 11 or 9, activating an indicator and a range switch, if desired.

- High input sensitivity
- Low saturation voltage of the switching transistors
- Low temperature-drift of the output transistor for the tuning voltage

Package outlines



Plastic plug-in package (16 pins) 20 A 16 DIN 41866
Weight approx. 1.2 g, dimensions in mm

Maximum ratings

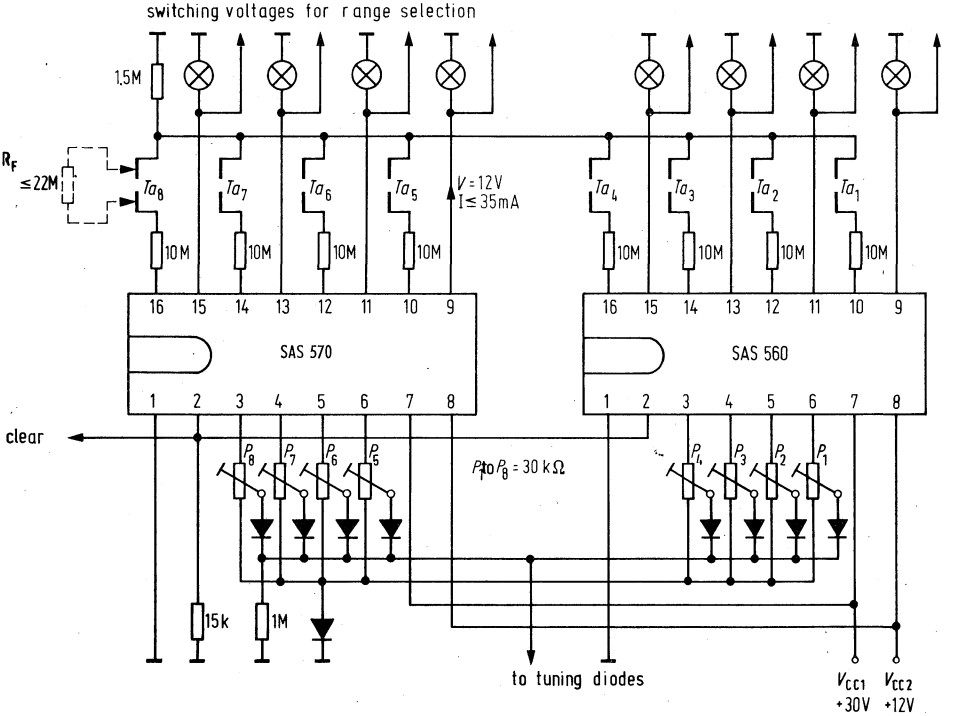
		SAS 560, SAS 570	
Supply voltage 1	V_{CC1}	36	V
Supply voltage 2	V_{CC2}	26.5	V
Driver current	$I_9, I_{11}, I_{13}, I_{15}$	35	mA
Max. driver current ($t_{max} \leqq 2$ s.)	$I_{9M}, I_{11M}, I_{13M}, I_{15M}$	70	mA
Tuning current	I_3, I_4, I_5, I_6	1	mA
Storage temperature	T_S	–40 to +125	°C
Ambient operating temperature	T_{amb}	0 to +70	°C
Range of operation	V_{CC1}	15 to 33	V
	V_{CC2}	6 to 24	V
	$V_{CC1-CC2}$	2 to 24	V

Operating characteristics (V_{CC1}=30 V, V_{CC2}=12 V)

Switching voltage while using keys $T_1 \ldots T_4$	$V_{2/1}$	4.5	V
Holding voltage after using keys $T_1 \ldots T_4$	$V_{2/1}$	3	V
Saturation voltage of range-switch after use of the corresponding key	$V_{15/8}$, $V_{13/8}$, $V_{11/8}$, $V_{9/8}$	<1.0	V
Saturation voltage of tuning switch after use of the corresponding key	$V_{3/7}$, $V_{4/7}$, $V_{5/7}$, $V_{6/7}$	<0.5	V
Temperature drift of the tuning switch T_{amb}=25 ° to 55 °C	$V_{3/7}$ to $V_{6/7}$	<1	mV/°C

After a simultaneous activation of several keys only one channel remains conducting.

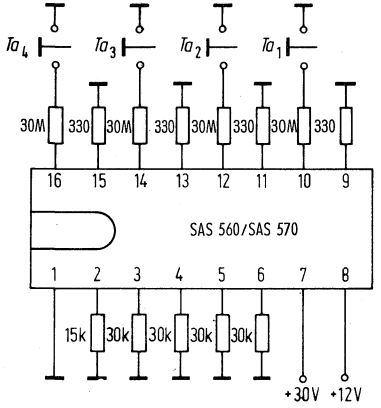
Application circuit



all diodes BA 127

SAS 560
SAS 570

Test circuit



B. Analog integrated circuits for industrial applications

Summary of types

Preface on operational amplifiers

Integrated operational amplifiers are dc-amplifiers with a very broad range of applications in automatic control systems, industrial electronics and the audio frequency area.

1. Symbols and terms used

The logic symbol "operational amplifier" shows only signal inputs and outputs. Figure 1 shows the symbol used, with an inverting input 1, a non-inverting input 2 and output 3. A positive signal at "1" results in a negative signal at output 3. Definitions of the most important terms generally used to characterize an operational amplifier are listed below. All definitions refer to symmetrical supply voltages.

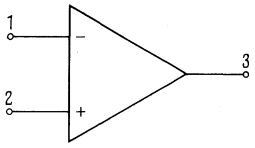


fig. 1

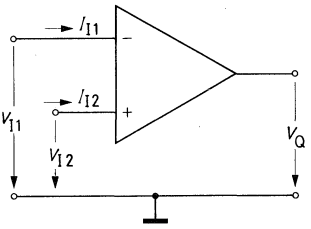


fig. 2

a) Input offset voltage V_{Io} is the dc voltage which must be applied between the input terminals to force the quiescent dc output voltage to OV (fig. 2).
$V_{Io}=V_{I1}-V_{I2}$ at $V_Q=O$ and generator resistance $R_G=O$.

b) Input current I_I is the current required for the opreration of the OP (fig. 2).

$$I_I=\frac{I_{I1}+I_{I2}}{2}$$

c) Input offset current I_{Io} is the difference between the currents into the two input terminals with the output at zero volts. At high values of generator resistance I_{Io} can cause difficulties (fig. 2)
$I_{Io}=I_{I1}-I_{I2}$ at $V_Q=O$.

d) Open-loop voltage gain G_v is the voltage gain without negative feedback from the output to the input (fig. 3).

$$G_v=\frac{V_Q}{V_I} \text{ at } Rf=\infty$$ (Rf=feedback resistance between output and input).

e) Common-mode voltage gain G_{VCM} is the voltage gain resulting when a signal is applied to both inputs at equal phase (fig. 4).

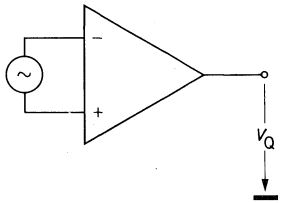


fig. 3

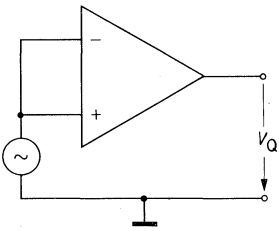


fig. 4

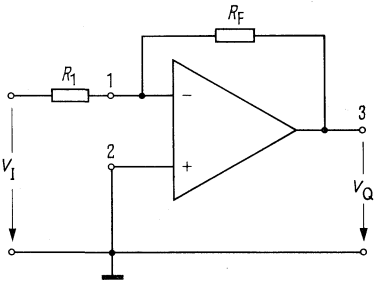
f) Common mode rejection ratio CMRR is the ratio of differential voltage gain (G_{VDF}) to common mode voltage gain (G_{VCM}).
$CMRR = 20\log|G_{VDF}| - 20\log|G_{VCM}|$.

g) Temperature coefficients of the input offset voltage and input offset current specify average values as a function of temperature. For a given range of temperature these coefficients may be regarded as approximately linear.

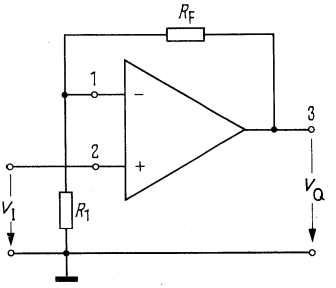
h) Input resistance R_I is the resistance measured between the inverting and the non-inverting input.

2. Basic circuits

Inverting amplifier: $V_Q = -\frac{R_F}{R_1} \cdot V_I$

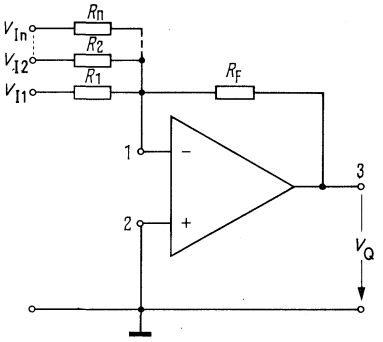


Non-inverting amplifier: $V_Q = \frac{R_1+R_F}{R_1} \cdot V_I$



Summing-amplifier

$$V_Q = -R_F\left(\frac{V_{I1}}{R_1} + \frac{V_{I2}}{R_2} + \ldots + \frac{V_{In}}{R_n}\right)$$

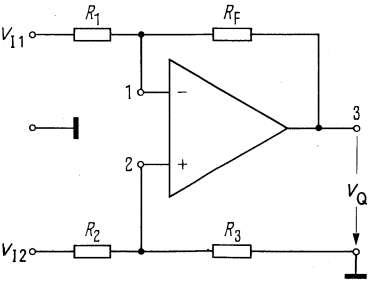


Difference-amplifier

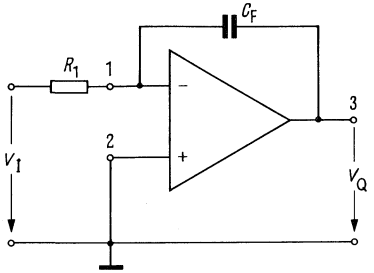
$$V_Q = \frac{R_3}{R_1}\left(\frac{R_1+R_F}{R_2+R_3}\right) \cdot V_{I2} - \frac{R_F}{R_1} \cdot V_{I1};$$

for $R_2 = R_1$ and $R_3 = R_F$,

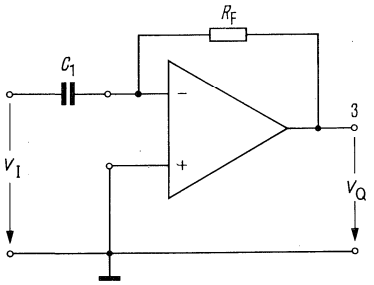
$$V_Q = \frac{R_F}{R_1}(V_{I2} - V_{I1})$$



Integrating amplifier $V_Q = -\frac{1}{R_1 C_F} \int V_I dt$



Differentiating amplifier: $V_Q = -R_F C_1 \cdot \frac{dV_I}{dt}$



Ordering codes

TAA 521: Q67000-A3
TAA 521 A: Q67000-A164
TAA 522: Q67000-A84

TAA 521
TAA 521 A
TAA 522

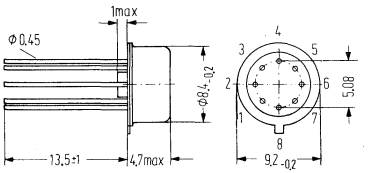
Operational amplifiers

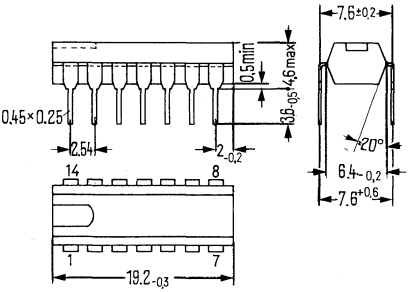
The integrated circuits TAA 521, TAA 521 A and TAA 522 are integrated operational amplifiers for demanding applications. These amplifiers are exceptionally well suited for industrial applications such as servo-systems, analog computers, measuring equipment etc. The frequency response can be adjusted by external circuits.

- High-resistance symmetrical input
- Low-resistance single-ended output
- Excellent temperature stability
- High common mode rejection

Package outlines

TBA 221, TBA 222





Package similar to 5 G 8 DIN 14873
(similar TO-99)
weight approx. 1.1g

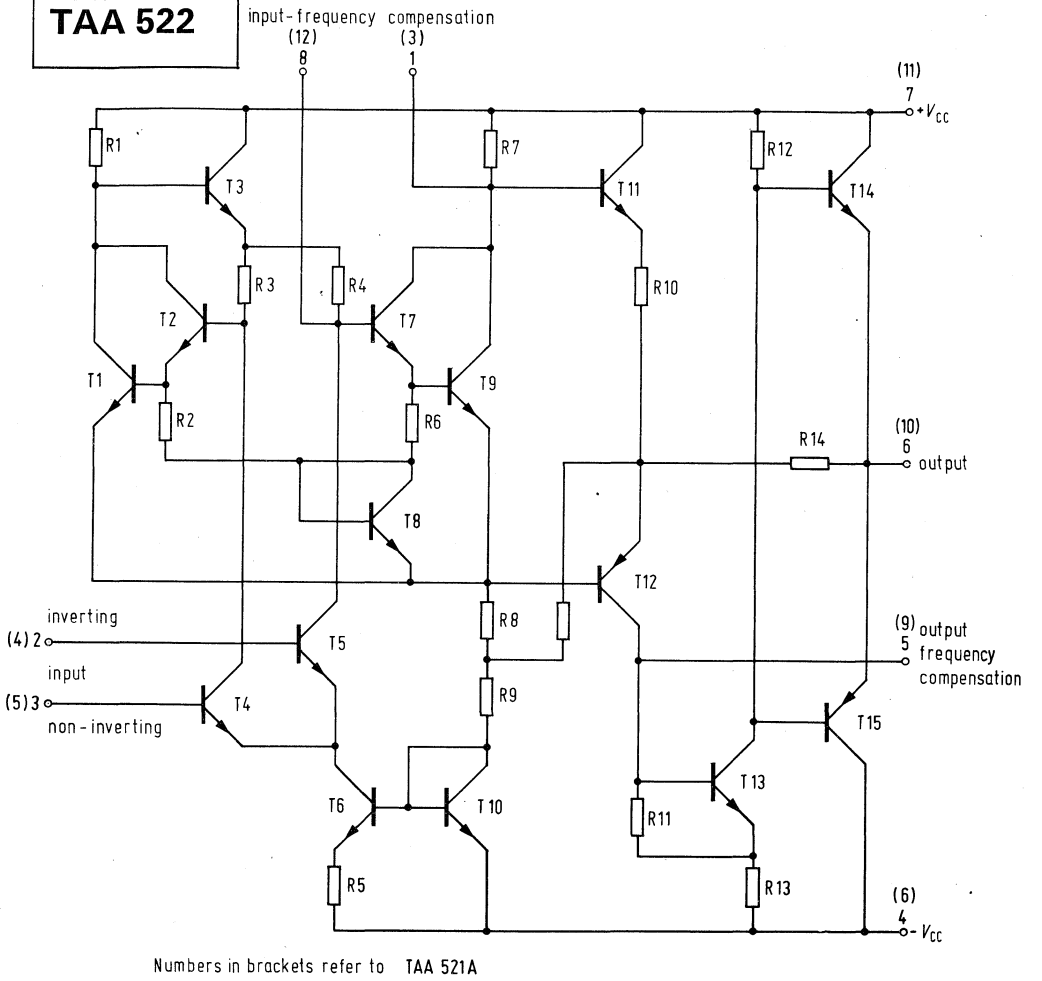
Plastic plug-in package (14 pins)
20 A 14 DIN 41866 (TO-116)
weight approx. 1.1g

Maximum ratings

		TAA 521 TAA 521 A	TAA 522	
Supply voltages	V_{CC}	±18	±18	V
Differential input voltage	V_{ID}	± 5	± 5	V
Maximum input voltage	V_I	±10	±10	V
Total power dissipation (T_{Case}=70°C)	P_{tot}	250	–	mW
(T_{Case}=95°C)	P_{tot}	–	300	mW
Output short circuit duration		5	5	s
Ambient operating temperature	T_{amb}	0 to 70	–55 to 125	°C
Storage temperature	T_S	–65 to 150	–65 to 150	°C

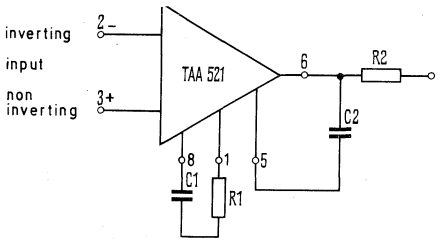
TAA 521
TAA 521 A
TAA 522

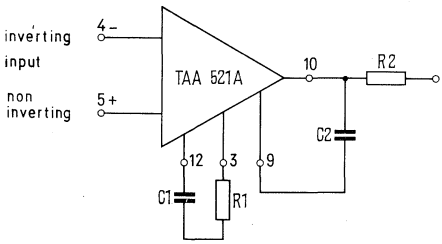
Circuit



Numbers in brackets refer to TAA 521A

Frequency compensating circuit: $R2=50\ \Omega$ for capacitive loads

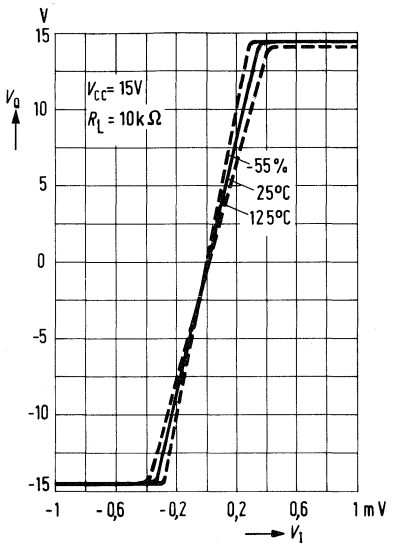




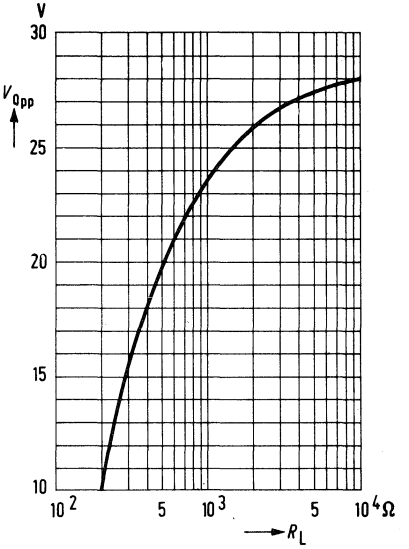
Operating characteristics (V_{CC}=±15 V, T_{amb}=25 °C, unless stated otherwise)		TAA 521, TAA 521A			TAA 522			
		min	typ	max	min	typ	max	
Total power dissipation (no load, no signal)	P_{tot}		80	200		80	165	.mW
Input offset voltage (R_G<10 kΩ)	V_{IO}		2	7.5		1	5	mV
Input offset voltage (R_G<10 kΩ, T_{amb}=0 to 70 °C)	V_{IO}			10			6	mV
Input offset current	I_{IO}		100	500		50	200	nA
Input offset current (T_{amb}=0 to 70°C)	I_{IO}			750				nA
Input offset current (T_{amb}=–55 to +125 °C)	I_{IO}					20	200	nA
Input current	I_I		0.3	1.5		0.21	0.5	μA
Input current (T_{amb}=0 to 70 °C)	I_I			2.0				μA
Input current (T_{amb}=–55 to +125 °C)	I_I					500	1500	nA
Input impedance	Z_I	50	250		150	400		kΩ
Input impedance (T_{amb}=–55 to +125 °C)	Z_I				40	100		kΩ
Maximum output voltage (R_L>10 kΩ)	V_{Opp}	±12	±14					V
Maximum output voltage (R_L≥10 kΩ, T_{amb}=–55 to +125 °C)	V_{Opp}				±12	±14		V
Maximum output voltage (R_L=2 kΩ)	V_{Opp}	±10	±13					V
Maximum output voltage (R_L≥2 kΩ, T_{amb}=–55 to +125 °C)	V_{Opp}				±10	±13		V
Output impedance	Z_O		150			150		Ω
Voltage gain (V_{Opp}=±10 V, R_L=2 kΩ)	G_v	83.6	93					db
Voltage gain (V_{Opp}=±10 V, R_L>2 kΩ, T_{amb}=0 to 70 °C)	G_v	81.5						db
Voltage gain (V_{Opp}=±10 V, R_L>2 kΩ, T_{amb}=–55 to +125 °C)	G_v				88	93		db
Common mode rejection ratio (R_G<10 kΩ)	$CMRR$	65	90		70	90		db
Average temperature coefficient of input offset voltage (R_G<10 kΩ, T_{amb}=0 to 70 °C)	α_{VIO}		10					μV/°C
Average temperature coefficient of input offset voltage (R_G=50 Ω, T_{amb}=–55 to +125 °C)	α_{VIO}						3	μV/° C
Average temperature coefficient of input offset voltage (R_G≤10 kΩ, T_{amb}=–55 to +125 °C)	α_{VIO}						6	μV/°C

TAA 521
TAA 521 A
TAA 522

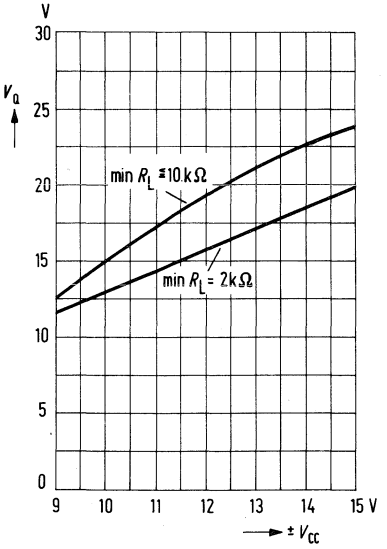
Transfer characteristic $V_Q = f(V_I)$



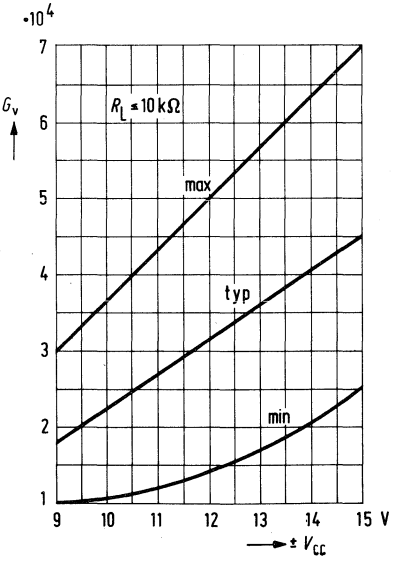
Output voltage $V_{Qpp} = f(R_L)$



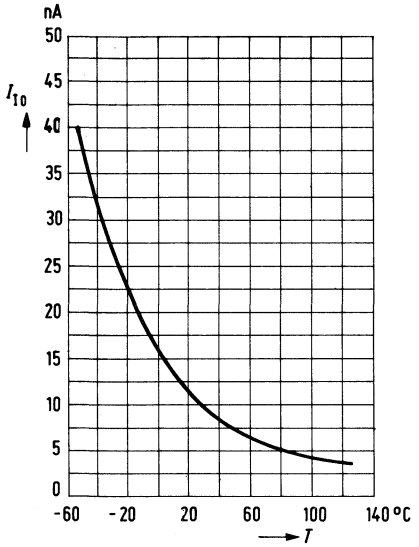
PP-output voltage $V_Q = f(V_{CC})$



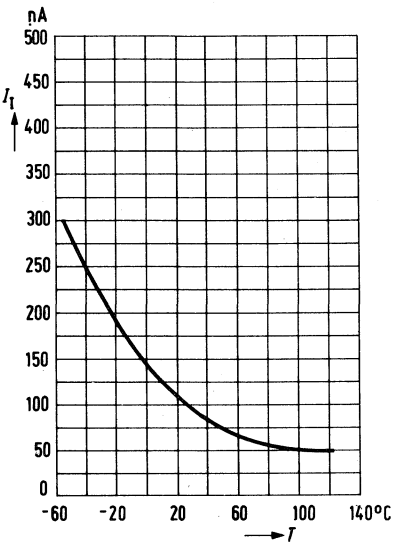
Open loop voltage gain $G_V = f(V_{CC})$



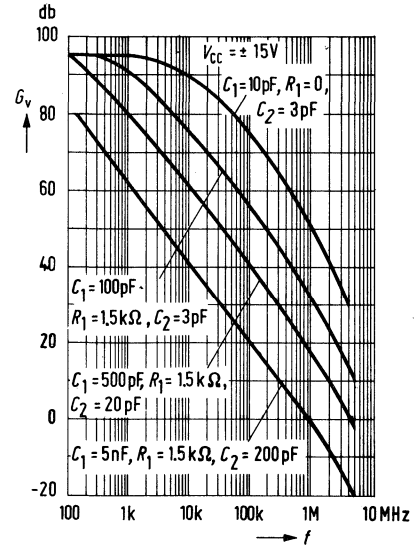
Input offset current $I_{IO}=f(T)$



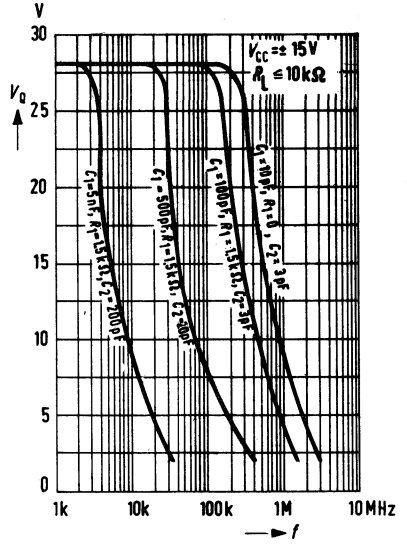
Input current $I_I=f(T)$



Open loop gain for various degrees of compensation $G_V=f(f)$



PP-output voltage $V_Q=f(f)$



TAA 721
TAA 722

Ordering codes

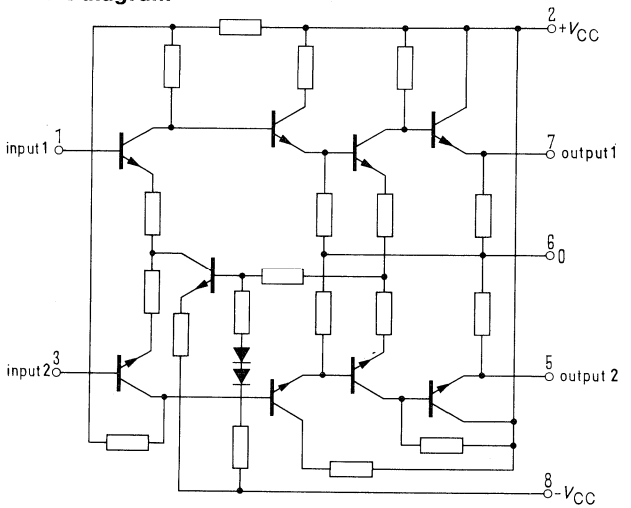
TAA 721: Q67000-A82
TAA 722: Q67000-A83

Broadband amplifier

The integrated circuits TAA 721 and TAA 722 are differential amplifiers with great bandwidth.

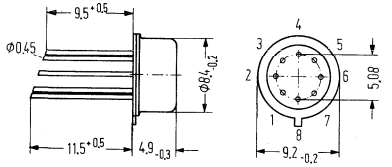
Differential inputs and outputs
Great bandwidth of 0 to 40 MHz
High common-mode rejection of 85 db
Excellent stability
Insensitive to asymmetrical supply voltages

Circuit diagram



(pin 4 connected to case)

Case outlines



Case 5 G 8 DIN 41873
(similar TO-78)
weight approx. 1.1 g

Maximum ratings

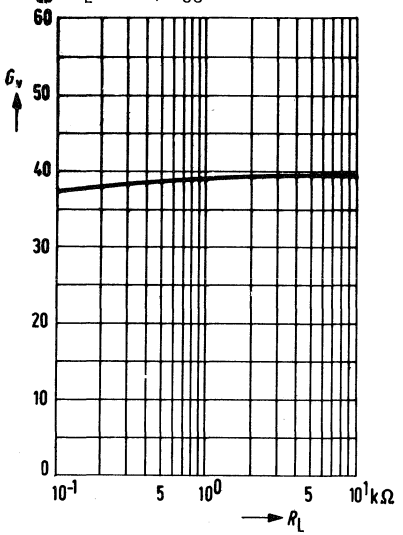
		TAA 721	TAA 722	
Supply voltage	V_{CC}	±8	±8	V
Differential input voltage	V_{ID}	5	5	V
Ambient operating temperature	T_{amb}	0 to 70	–55 to 125	°C
Storage temperature	T_S	–65 to 150	–65 to 150	°C

Operating characteristics
(V_{CC}=±6 V, T_{amb}=25 °C)

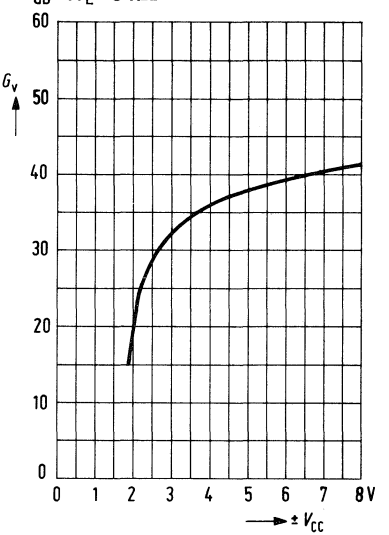
		TAA 721			TAA 722			
		min	typ	max	min	typ	max	
Current requirement	$\pm I_{CC}$	11.5	18.0	24.5	13.5	18.0	22.5	mA
Power dissipation (no load, no signal)	P_{tot}		165	220		165	220	mW
Input current	I_I		50	100		40	80	μA
Input offset current	I_{IO}		5	30		3	20	μA
Input impedance (f=100 kHz)	Z_I		6			6		kΩ
Maximum output voltage (R_L=5 kΩ, f=100 kHz)	V_{Qpp}		3.7			3.7		V
Output offset voltage[1])	V_{Qo}		0.5	2.0		0.5	1.2	V
Output impedance (f=100 kHz)	Z_Q		35			35		Ω
Voltage gain[2]) (V_I=1 mV, R_C=5 kΩ, f=100 kHz)	G_v	35.5	39.6	41.6	37.5	39.6	40.8	db
Common mode rejection ratio (f=100 kHz, R_L=5 kΩ)	$CMRR$		85			85		db
Common mode voltage gain (V_{ICM}=0.3 V, R_L=5 kΩ, f=100 kHz)	G_{VCM}		–45	–30		–45	–30	db
Bandwidth (–3 db)	B		40			40		MHz
Distortion factor (V_I=1 V, R_L=5 kΩ, f=10 kHz)	k		2.0			1.5		%
Rise time ⎫ of the	t_r		10	15		9	12	ns
Fall time ⎭ output pulse (V_I=5 mV)	t_f		10	15		9	12	ns

[1]) measured between both outputs
[2]) output voltage to ground. Between both outputs, the gain measured is twice as high, the outputs being of opposite phase.

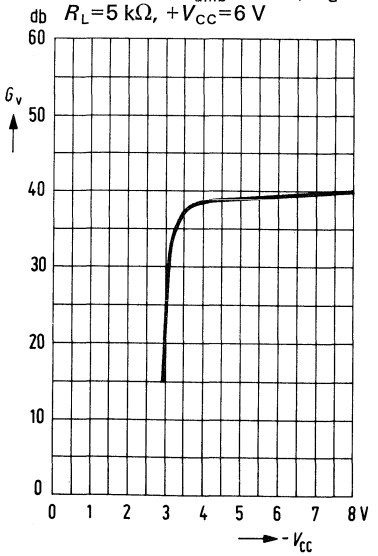
Voltage gain $G_V = f(R_L)$
f=100 kHz, T_{amb}=25 °C, R_G=50 Ω
R_L=5 kΩ, V_{CC}=±6 V



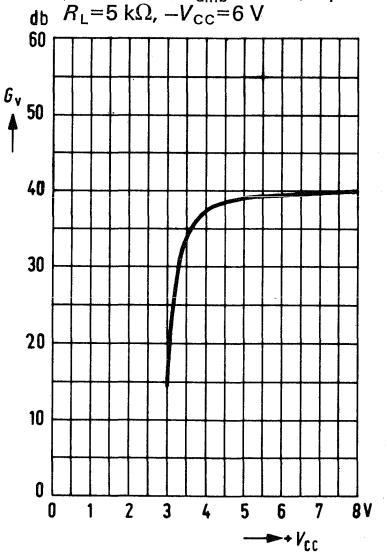
Voltage gain $G_V = f(\pm V_{CC})$
f=100 kHz T_{amb}=25 °C, R_G=50 Ω
R_L=5 kΩ



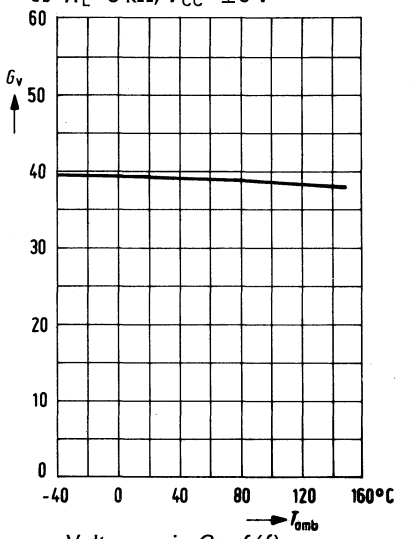
Voltage gain $G_V = f(-V_{CC})$
f=100 kHz, T_{amb}=25 °C, R_G=50 Ω
R_L=5 kΩ, $+V_{CC}$=6 V



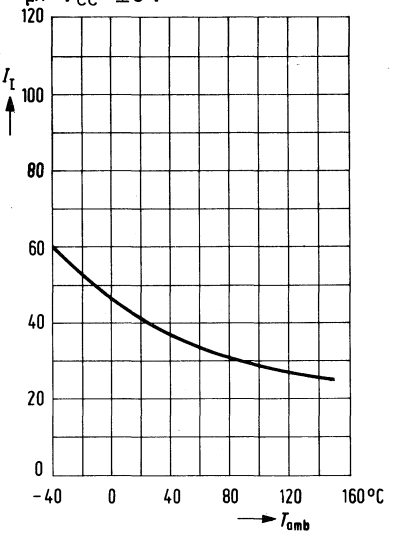
Voltage gain $G_V = f(+V_{CC})$
f=100 kHz, T_{amb}=25 °C, R_I=50 Ω
R_L=5 kΩ, $-V_{CC}$=6 V



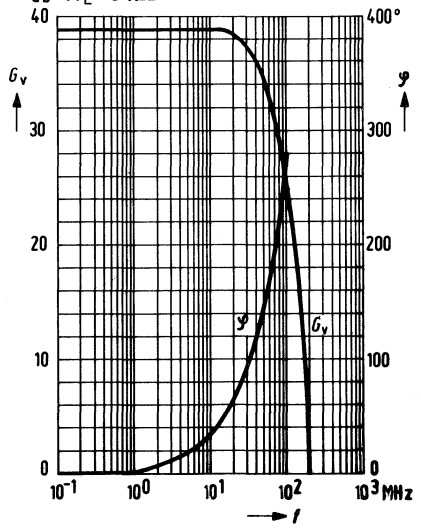
Voltage gain $G_V=f(T_{amb})$
f=100 kHz, T_{amb}=25 °C, R_G=50 Ω,
R_L=5 kΩ, V_{CC}=±6 V



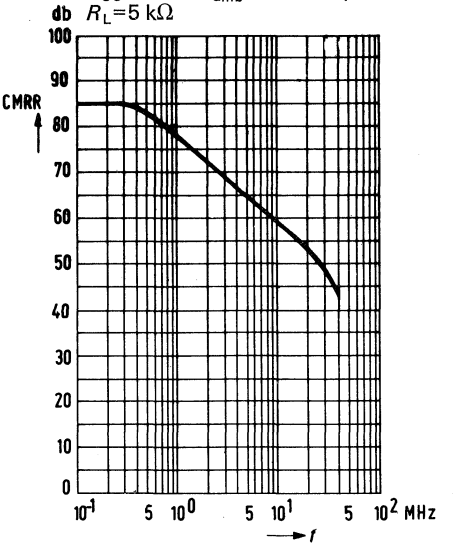
Input current $I_I=f(T_{amb})$
V_{CC}=±6 V



Voltage gain $G_V=f(f)$
Phase deviation $\varphi=f(f)$
V_{CC}=±6 V T_{amb}=25 °C, R_I=50 Ω,
R_L=5 kΩ



Common mode rejection $CMRR=f(f)$
V_{CC}=±6 V, T_{amb}=25 °C, R_I=50 Ω,
R_L=5 kΩ



TAA 761
TAA 761 A
TAA 761 W
TAA 765
TAA 765 A
TAA 765 W

Ordering codes

TAA 761:	Q67000-A224
TAA 761 A:	Q67000-A522
TAA 761 W:	Q67000-A598
TAA 765:	Q67000-A229
TAA 765 A:	Q67000-A524
TAA 765 W:	Q67000-A599

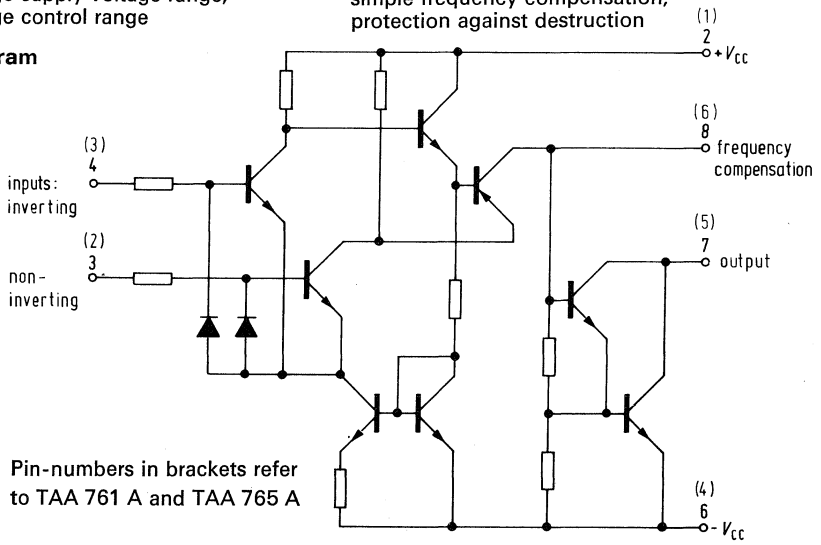
Operational amplifier

A particularly economical and universal operational amplifier which by its excellent performance qualities is well suited for a wide range of applications, such as automatic controls, automobile electronics, AF-circuits, analog computers etc.
In addition to a high gain, high input resistance, low offset voltage, low temperature- and supply voltage-dependence, the amplifier features

wide common-mode range,
large supply voltage range,
large control range

high output current,
simple frequency compensation,
protection against destruction

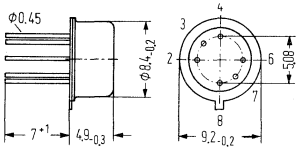
Circuit diagram



Pin-numbers in brackets refer to TAA 761 A and TAA 765 A

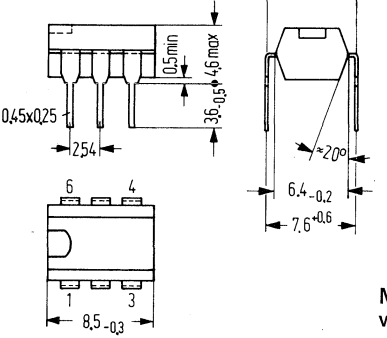
Package outlines:

TAA 761, TAA 765



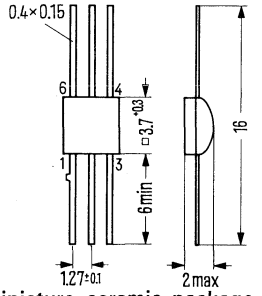
Case 5 H 6
DIN 41873
(similar TO 78)
Weight approx. 1 g

TAA 761 A, TAA 765 A



Plastic plug-in package
6 pins
20 A 6 DIN 41866
Weight approx. 0.7 g

TAA 761 W, TAA 765 W



Miniature ceramic-package
weight approx. 0.07 g

TAA 761
TAA 761 A
TAA 761 W
TAA 765
TAA 765 A
TAA 765 W

Maximum ratings

Supply voltage	V_{CC}	±18	V
Max. output current	I_Q	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	V
Range of operation	V_{CC}	±2 to ±18	V
Ambient operating temperature (TAA 761, 761 A)	T_{amb}	0 to +70	°C
Ambient operating temperature (TAA 765, 765 A)	T_{amb}	–25 to +80	°C
Junction temperature	T_j	150	°C
Storage temperature	T_s	–40 to +125	°C
Thermal resistances:			
System-case (TAA 761, TAA 765)	$R_{thSease}$	80	°C/W
System-ambient air	R_{thSamb}	300	°C/W
System-package (TAA 761 A, TAA 765 A)	$R_{thSease}$	160	°C/W
System-package (TAA 761 W, TAA 765 W)	$R_{thSease}$	140	°C/W

Operating characteristics
(V_{CC}=±15 V, T_{amb}=25 °C)

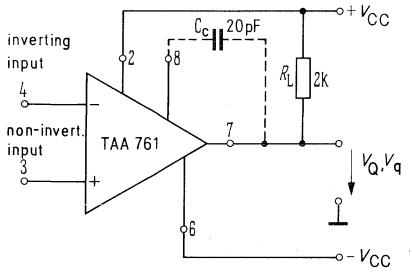
		min	typ	max	
Power dissipation (R_L=2 kΩ, V_Q~0 V)	P_{tot}		150		mW
Current requirement (no signal, no load, I through conn. 2)	I_{CC2}		1.8	2.5	mA
Input offset voltage (R_G=60 Ω)	V_{IO}			7.5	mV
Input offset current	I_{IO}		50	300	nA
Input current	I_I		0.3	1.0	μA
Maximum output voltage (R_L=2 kΩ)	V_{Qpp}	±14			V
Maximum output voltage (R_L=620 Ω)	V_{Qpp}	±12			V
Maximum output voltage (R_L=2 kΩ, f=100 kHz)	V_{Qpp}		±10		V
Input impedance (f=1 kHz)	Z_I		200		kΩ
Open-loop voltage gain (R_L=2 kΩ, f=1 kHz)	G_V	81.5	85		db
Open-loop voltage gain (R_L=10 kΩ, f=1 kHz)	G_V		90		db
Open-loop voltage gain (R_L=2 kΩ, f=1 MHz)	G_V		43		db
Output leakage current	I_{Qlk}		7		μA

Operating characteristics (continued)
(V_{CC}=±15 V, T_{amb}=25 °C)

		min	typ	max	
Input common-mode range (R_L=2 kΩ)	V_{ICM}	±12.0	±13.5		V
Common mode rejection ratio (R_L=2 kΩ)	$CMRR$		86		db
Supply voltage effect suppression (C_C=1 pf, G_V=100)	$\frac{\Delta V_{IO}}{\Delta V_{CC}}$		25	200	μV/V
Temp.-coeff. of V_{IO} (R_G=60 Ω)	α_{VIO}		6		μV/°C
Temp.-coeff. of I_{IO} (R_G=60 Ω)	α_{IIO}		0.3		nA/°C
Rise time of V_Q for non-inverting operation (test circuit 1)	$\frac{dV_Q}{dt_r}$		9		V/μs
Rise time of V_Q for inverting operation (test circuit 2)	$\frac{dV_Q}{dt_r}$		18		V/μs

Connection diagram

C_C=Output frequency compensation, R_L=Load resistor



Ordering code
TAA 762: Q67000-A523

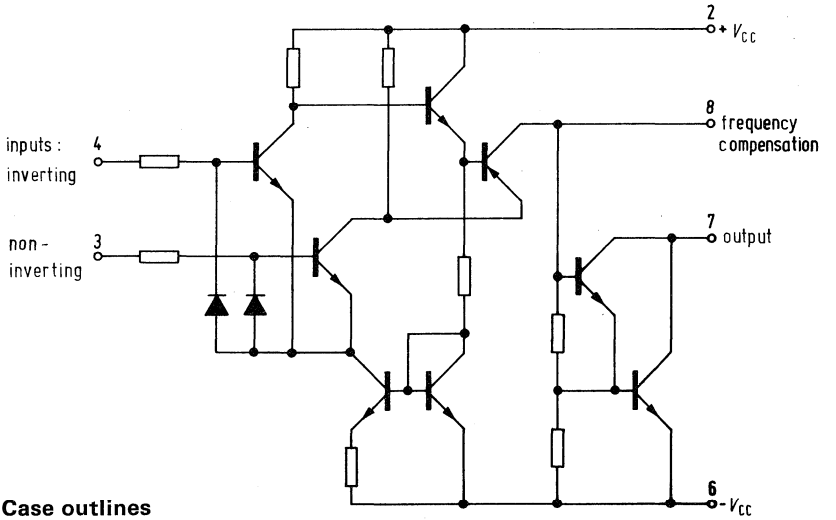
TAA 762

Operational amplifier

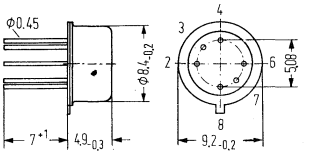
A particularly economical and universal operational amplifier which by its excellent performance qualities is well suited for a wide range of applications, such as automatic controls, automobile electronics, AF-circuits, analog computers etc.
In addition to a high gain, high input resistance, low offset-voltage, low temperature- and supply voltage-dependence, the amplifier features

wide common-mode range,
large supply-voltage range,
large control range,
high output current,
simple frequency compensation
protection against destruction
wide temperature range

Circuit diagram



Case outlines



Case 5 H 6
DIN 41873
(similar TO-78)
Weight approx. 1 g

TAA 762

Operational amplifier

Maximum ratings

Supply voltage	V_{CC}	±18	V
Max. output current	I_Q	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	
Range of operation	V_{CC}	±2 to ±18	V
Ambient operating temperature	T_{amb}	–55 to +125	°C
Junction temperature	T_j	150	°C
Storage temperature	T_S	–55 to +125	°C

Thermal resistance:			
System-case	$R_{thScase}$	80	°C/W
System-ambient air	R_{thSamb}	300	°C/W

Operating characteristics
(V_{CC}=±15 V, T_{amb}=–55 to + 125°C)

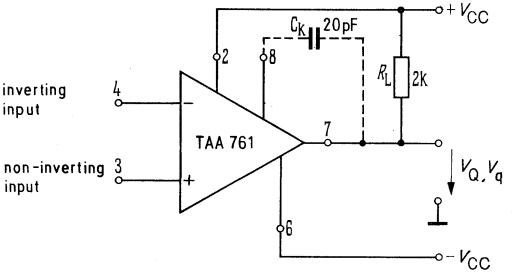
		min	typ at 25° C	max	
Power dissipation (R_L=2 kΩ, V_Q≈0)	P_{tot}		150		mW
Current repuirement (no signal, no load, I through conn. 2)	I_{CC2}		1.8	2.5	mA
Input offset voltage (R_G=60 Ω)	V_{1o}			7.5	mV
Input offset current	I_{Io}		50	300	nA
Input Current	I_I		0.3	1.5	μA
Maximum output voltage (R_L=2 kΩ)	V_{Qpp}	± 14			V
Maximum output voltage (R_L=620 Ω)	V_{Qpp}	± 12			V
Maximum output voltage (R_L=2 kΩ, f=100 kHz)	V_{Qpp}		± 10		V
Input impedance (f=1 kHz)	Z_I		200		kΩ
Open-loop voltage gain (R_L=2 kΩ, f=1 kHz)	G_V	81.5	85		db
Open-loop voltage gain (R_L=10 kΩ, f=1 kHz)	G_v		90		db
Open-loop voltage gain (R_L=2 kΩ, f=1 MHz)	G_v		43		db
Output leakage current	I_{Qlk}		7		μA

Operating characteristics (continued)
(V_{CC}=±15 V, T_{amb}=–55 to 125 °C)

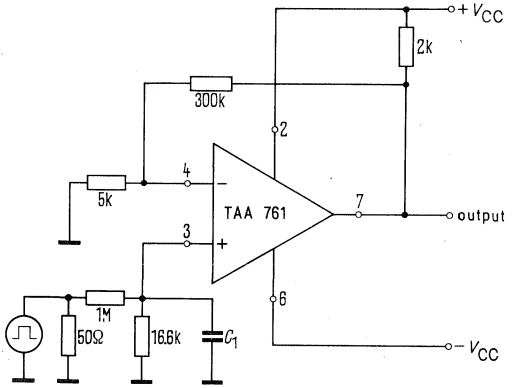
		min	typ at 25° C	max	
Input common mode range (R_L=2 kΩ)	V_{ICM}		± 13.5		V
Common mode rejection ratio (R_L=2 kΩ)	$CMRR$		86		db
Supply voltage effect suppression (C_C=1 pf, G_v=100)	$\frac{\Delta V_{IO}}{\Delta V_{CC}}$		25	200	μV/V
Temp.-coeff of V_{IO} (R_G=60 Ω)	α_{VIO}		6		μV/°C
Temp.-coeff of I_{IO} (R_G=60 Ω)	α_{IIO}		0.3		nA/°C
Rise time of V_Q for non-inverting operation (test circuit 1)	$\frac{dV_Q}{dt_r}$		9		V/μsec
Rise time of V_Q for inverting operation (test circuit 2)	$\frac{dV_Q}{dt_r}$		18		V/μsec

Connection diagram

C_C=Output frequency compensation, R_L=Load resistor

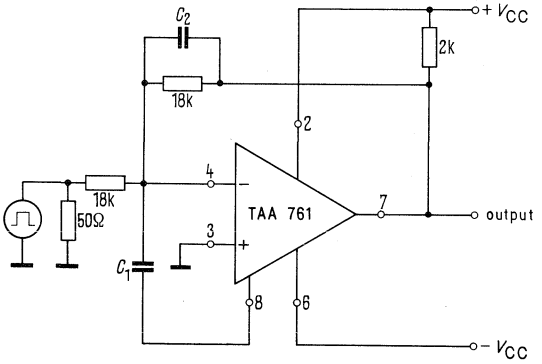


Test circuit 1 (non-inverting operation)



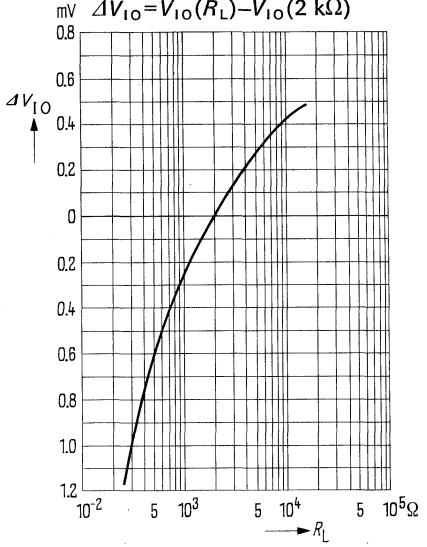
C_1 for min. overshoot (approx. 22 pf)

Test circuit 2 (inverting operation)

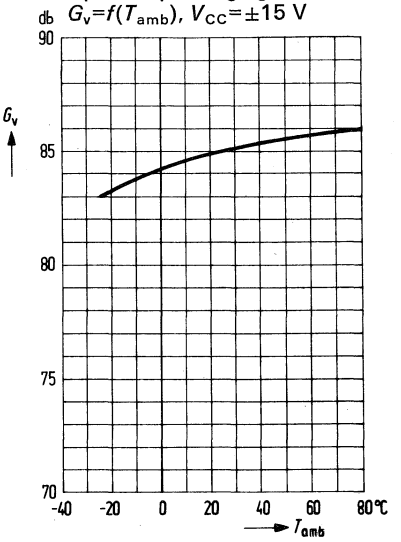


C_2 has the effect of a frequency-dependent compensation for the reduction of the rise-times (approx. 390 pf), C_1 for min. overshoot (approx. 3.9 pf)

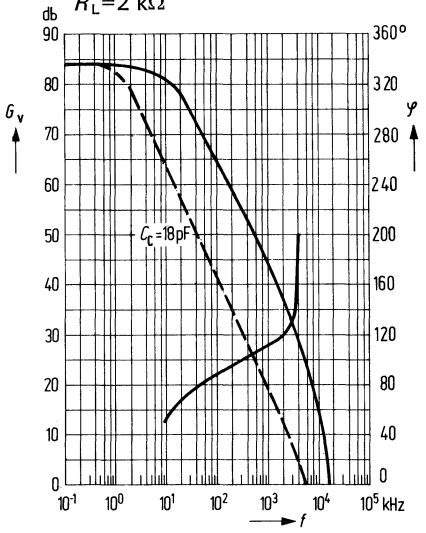
Offset voltage change $\Delta V_{IO}=f(R_L)$
$V_{CC}=\pm 15$ V
$\Delta V_{IO}=V_{IO}(R_L)-V_{IO}(2\ k\Omega)$



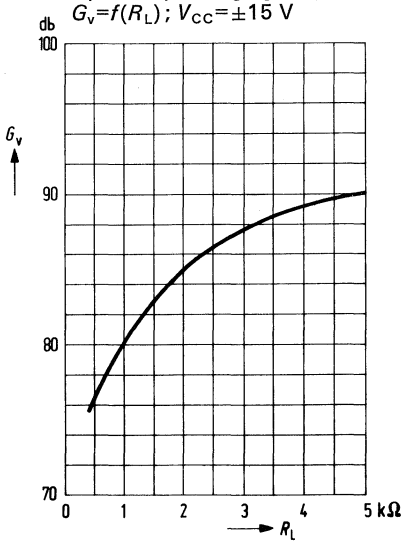
Open-loop voltage gain
$G_v=f(T_{amb})$, $V_{CC}=\pm 15$ V



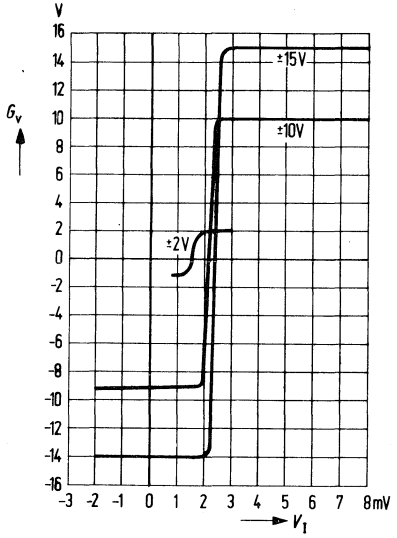
Open-loop gain and phase
$G_v=f(f)$; $\varphi=f(f)$; $V_{CC}=\pm 15$ V
$R_L=2\ k\Omega$



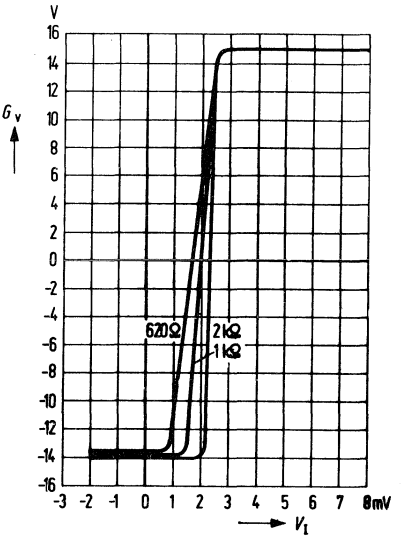
Open-loop voltage gain
$G_v=f(R_L)$; $V_{CC}=\pm 15$ V



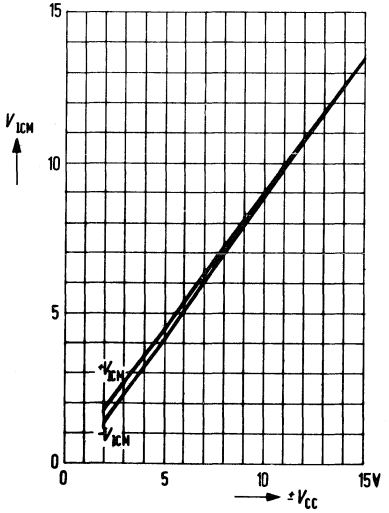
Transfer characteristic $G_v=f(V_I)$
V_{CC}=parameter, R_L=2 kΩ



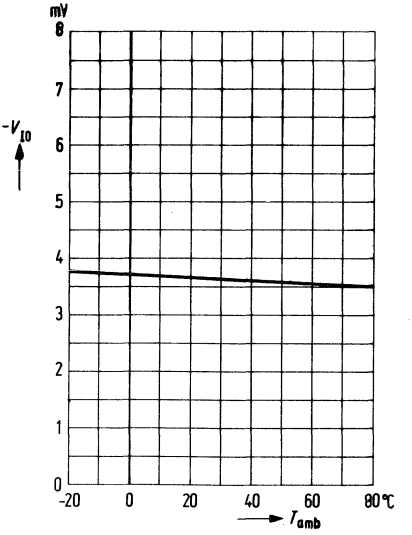
Transfer characteristic $G_v=f(V_I)$
V_{CC}=±15 V, R_L=parameter



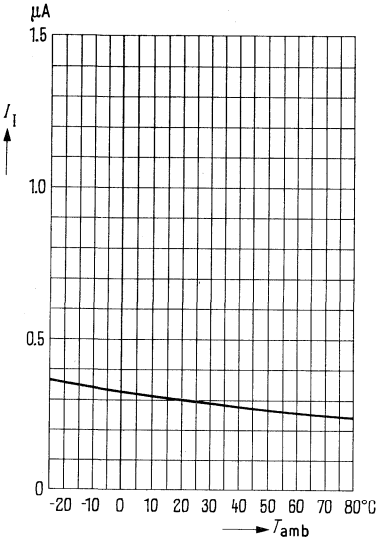
Common mode range
$V_{ICM}=f(V_{CC})$



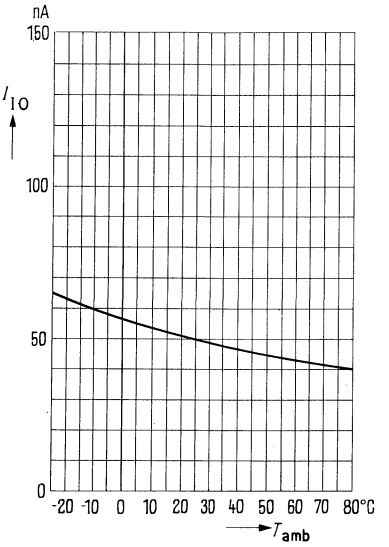
Input offset voltage $V_{IO}=f(T_{amb})$
V_{CC}=±15 V; R_L=2 kΩ



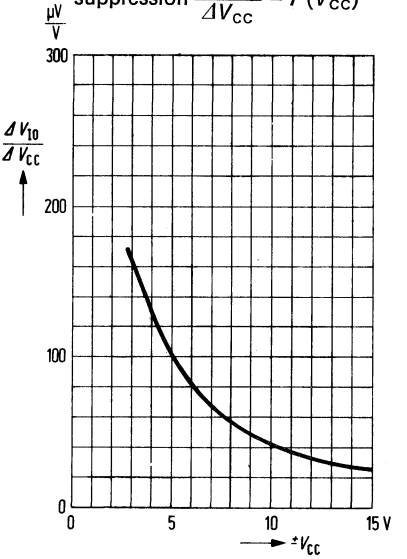
Input current $I_I = f(T_{amb})$
$V_{CC} = \pm 15$ V; $R_L = 2$ kΩ



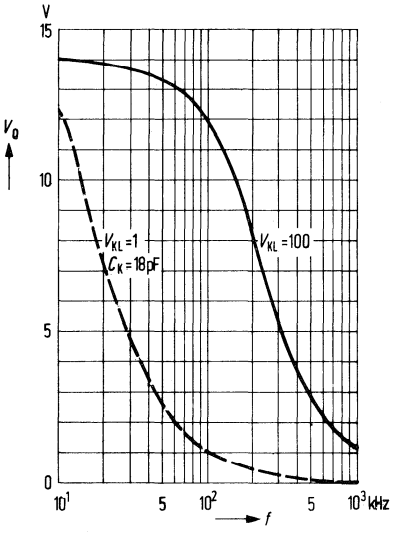
Input current $I_{IO} = f(T_{amb})$
$V_{CC} = \pm 15$ V; $R_L = 2$ kΩ



Supply voltage effect
suppression $\frac{\Delta V_{IO}}{\Delta V_{CC}} = f(V_{CC})$



Frequency dependence of the large signal control range $V_Q = f(f)$



Ordering codes

TAA 861: Q67000-A89
TAA 861 A: Q67000-A278
TAA 861 W: Q67000-A89-S3
TAA 865: Q67000-A109
TAA 865 A: Q67000-A279
TAA 865 W: Q67000-A109-S1

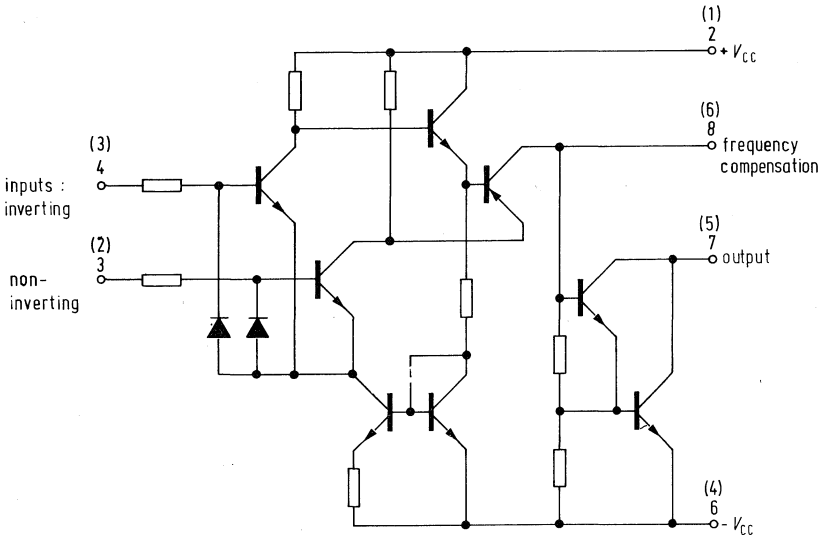
TAA 861
TAA 861 A
TAA 861 W
TAA 865
TAA 865 A
TAA 865 W

Operational amplifiers

Especially economical and universal operational amplifiers which by their excellent performance qualities are well suited for a wide range of applications, such as automatic controls, automobile electronics, AF-circuits, analog computers etc.
In addition to a high gain, high input resistance, low offset voltage, low temperature- and supply voltage-dependence, the amplifiers feature

wide common-mode range,
large supply voltage range,
large control range,
high output current,
simple frequency compensation
protection against destruction

Circuit diagrams
for TAA 861, TAA 865
and TAA 861 A, TAA 865 A



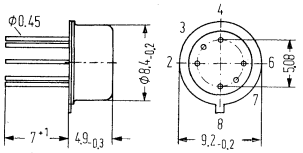
Connection numbers in brackets refer to TAA 861 A and TAA 865 A

TAA 861
TAA 861 A
TAA 861 W
TAA 865
TAA 865 A
TAA 865 W

Operational amplifiers:

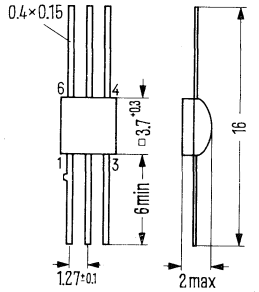
Package outlines

TAA 861, TAA 865



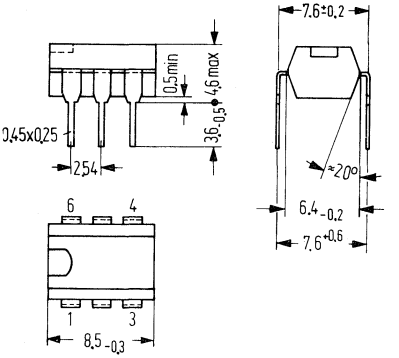
Package 5 H 6 DIN 41873
(similar TO-78)
weight approx. 1 g

TAA 861 W, TAA 865 W



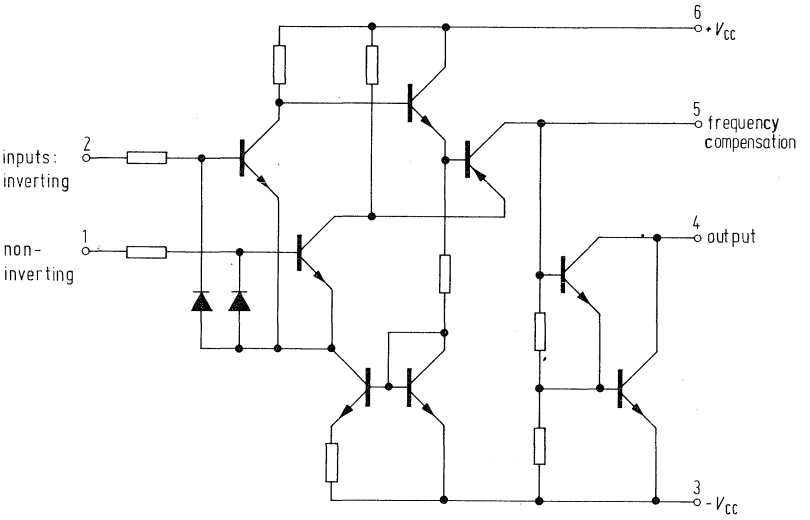
Miniature
ceramic-package
weight approx. 0.07 g

TAA 861 A, TAA 865 A



Plastic plug-in package, 6 pins
20 A 6 DIN 41866
weight approx. 0.7 g

Circuit for TAA 861 W and TAA 865 W



TAA 861
TAA 861 A
TAA 861 W
TAA 865
TAA 865 A
TAA 865 W

Operational amplifiers

Maximum ratings		TAA 861 TAA 861 A TAA 861 W	TAA 865 TAA 865 A TAA 865 W	
Supply voltage	V_{CC}	±10	±10	V
Max. output current	I_O	70	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	$\pm V_{CC}$	V
Range of operation	V_{CC}	±2 to ±10	±2 to ±10	V
Ambient operating temperature	T_{amb}	0 to +70	–25 to +80	°C
Junction temperature	T_j	150	150	°C
Storage temperature	T_s	–40 to +125		°C
Thermal resistances				
System-case (TAA 861, TAA 865)	$R_{thScase}$	80		°C/W
System-ambient air (TAA 861, TAA 865)	R_{thSamb}	200		°C/W
System-package (TAA 861 A, TAA 865 A)	$R_{thScase}$	160		°C/W
System-package (TAA 861 W, TAA 865 W)	$R_{thScase}$	140		°C/W

TAA 861
TAA 861 A
TAA 861 W
TAA 865
TAA 865 A
TAA 865 W

Operating characteristics
(V_{CC}=±10 V, T_{amb}=25 °C)

		min	typ	max	
Power dissipation (R_L=2 kΩ, V_Q~0)	P_{tot}		70		mW
Current requirement (no signal, no load, I through conn. 2)	I_{CC2}		1.0	2.5	mA
Input offset voltage (R_G=60 Ω)	V_{IO}		4.0	10	mV
Input offset current	I_{IO}		70	300	nA
Input current	I_I		0.3	1.0	μA
Maximum output voltage (R_L=2 kΩ)	V_{Qpp}	±9			V
Maximum output voltage (R_L=250 Ω)	V_{Qpp}	±8			V
Input impedance (f=1 kHz)	Z_I		200		kΩ
Open-loop gain (R_L=2 kΩ, f=1 kHz)	G_V	75	84		db
Open-loop gain (R_L=10 kΩ, f=1 kHz)	G_V		90		db
Open-loop gain (R_L=2 kΩ, f=1 MHz)	G_V		43		db
Input common-mode range (R_L=2 kΩ)	V_{ICM}		±9		V
Common mode rejection ratio (R_L=2 kΩ)	$CMRR$		86		db
Noise voltage (according to DIN 45405; radio-application; referring to input; R_S=2.5 kΩ)	V_N	3.1	3.1		μV
Temperature-coefficient of V_{IO} (R_G=60 Ω, T_{amb}=0 to 70 °C)	α_{VIO}		6		μV/°C
Temperature-coefficient of I_{IO} (R_G=60 Ω, T_{amb}=0 to 70 °C)	α_{IIO}		0.3		nA/°C
Rise time of V_Q for non-inverting operation (test circuit 1, TAA 861)	$\frac{dV_Q}{d_{tr}}$		3		V/μsec
Rise time of V_Q for inverting operation (test circuit 2, TAA 861)	$\frac{dV_Q}{d_{tr}}$		12		V/μsec

Ordering codes

TAA 862: Q67000-A236
TAA 862 F: Q67000-A280

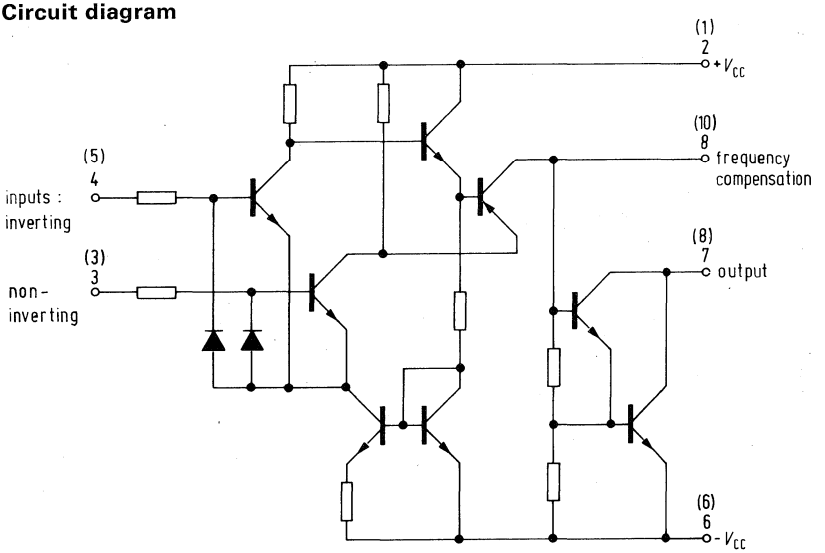
TAA 862
TAA 862 F

Operational amplifiers

Especially economical and universal operational amplifiers which by their excellent performance qualities are well suited for a wide range of applications.
In addition to a high gain, high input resistance, low offset voltage, low temperature- and supply voltage-dependence, the amplifiers feature

wide common-mode range,
large supply-voltage range,
wide range of operating temperature,
large control range
high output current,
simple frequency compensation
protection against destruction

Circuit diagram

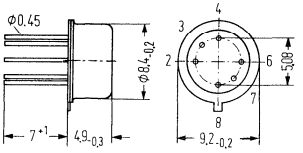


Connection numbers in brackets refer to TAA 862 F

TAA 862
TAA 862 F

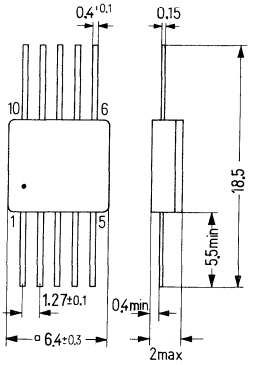
Package outlines

TAA 862



Metal-case 5 H 6 DIN 41873
(similar TO-78)
weight approx. 1 g

TAA 862 F



Metal-ceramic package
21 B 10 DIN 41865
(similar TO-91)
weight approx. 1.1 g

Maximum ratings

	TAA 862, TAA 862 F	
Supply voltage	V_{CC}	±10	V
Max. output current	I_O	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	V
Range of operation	V_{CC}	±2 to ±10	V
Ambient operating temperature	T_{amb}	–55 to +125	°C
Junction temperature	T_j	150	°C
Storage temperature	T_s	–55 to +125	°C
Thermal resistances			
System-case (TAA 862)	$R_{thScase}$	80	°C/W
System-ambient air (TAA 862)	R_{thSamb}	200	°C/W

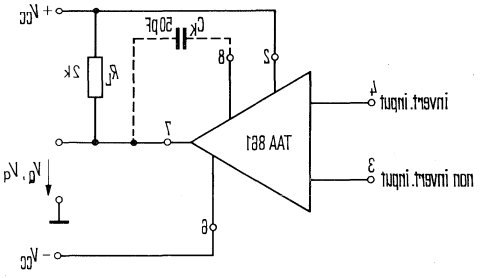
Operating characteristics
(V_{CC}=±10 V, T_{amb}=–55 to +125 °C)

		min	typ at 25 °C	max	
Power dissipation (R_L=2 kΩ, V_Q~0)	P_D		70		mW
Current requirement (no signal, no load, I through conn. 2)	I_{CC2}		1.0	2.5	mA
Input offset voltage (R_G=60 Ω)	V_{IO}		2	10	mV
Input offset current	I_{IO}		60	300	nA
Input current	I_I		0.3	1.0	μA
Maximum output voltage (R_L=2 kΩ)	V_{Opp}	±9			V
Maximum output voltage (R_L=400 Ω)	V_{Opp}	±8			V
Input impedance (f=1 kHz)	Z_I		200		kΩ
Open loop gain (R_L=2 kΩ, f=1 kHz)	G_V	75	85		db
Open loop gain (R_L=10 kΩ, f=1 kHz)	G_V		90		db
Open loop gain (R_L=2 kΩ, f=1 MHz)	G_V		43		db
Input common mode range (R_L=2 kΩ)	V_{ICM}		±9		V
Common mode rejection ratio (R_L=2 kΩ)	$CMRR$	80	86		db
Noise voltage (according to DIN 45405; radio application; referring to input; R_S=2.5 kΩ)	V_N		3.1		μV
Temperature coefficient of V_{IO} (R_G=60 Ω)	α_{VIO}		6		μV/°C
Temperature coefficient of I_{IO} (R_G=60 Ω)	α_{IIO}		0.3		nA/°C
Rise time of V_Q for non-inverting operation (test circuit 1, TAA 861)	$\frac{dV_Q}{d_{tr}}$		3		V/μsec
Rise time of V_Q for inverting operation (test circuit 2, TAA 861)	$\frac{dV_Q}{d_{tr}}$		12		V/μsec

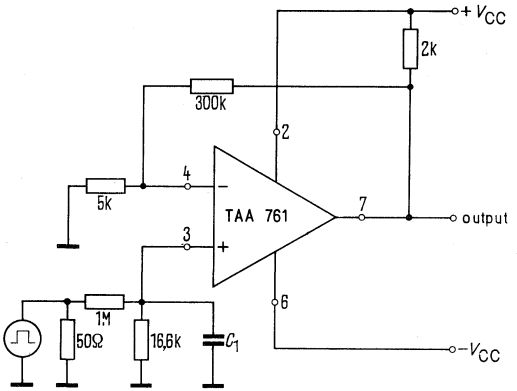
TAA 861
TAA 862
TAA 865

Connection diagram:

C_C=Output frequency compensation; R_L=load resistor

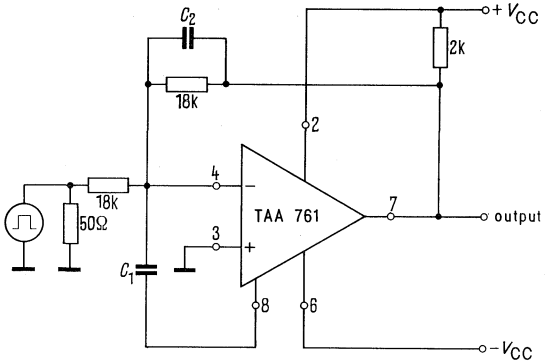


Test circuit 1 (non-inverting operation)



C_1 for min. overshoot (about 22 pf)

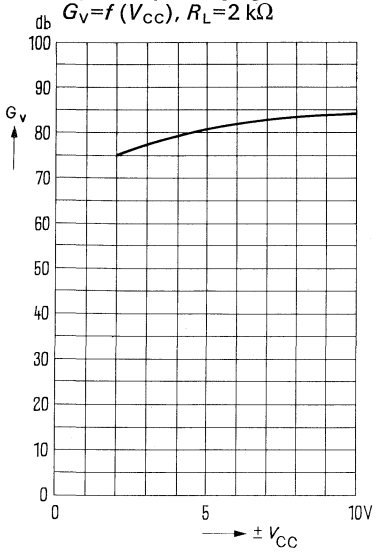
Test circuit 2 (inverting operation)



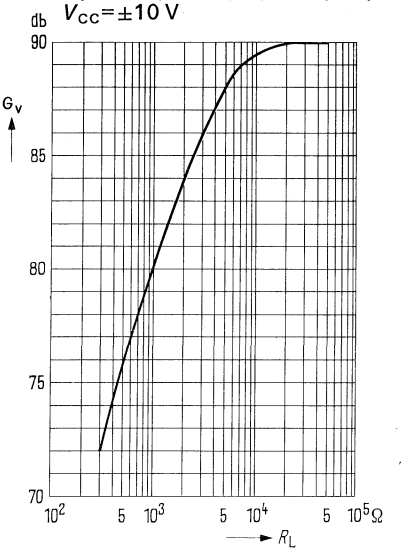
C_1 has the effect of a frequency-dependent compensation for the reduction of the rise-times (approx. 390 pf)
C_2 for min. overshoot (approx. 3.9 pf)

TAA 861
TAA 862
TAA 865

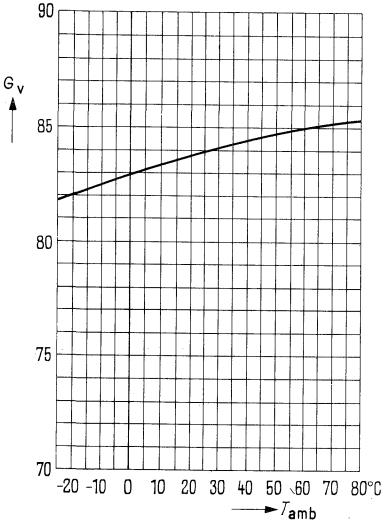
Open loop voltage gain
$G_V = f(V_{CC})$, $R_L = 2\,k\Omega$



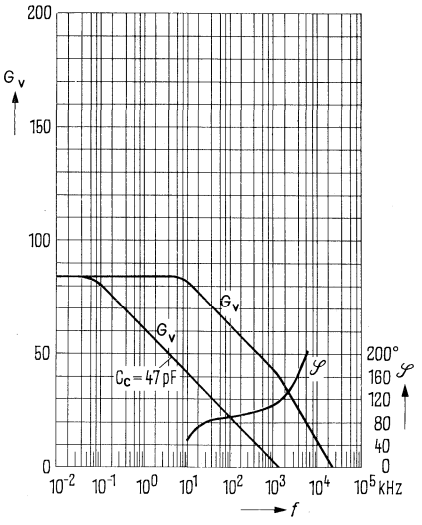
Open-loop voltage gain $G_V = f(R_L)$;
$V_{CC} = \pm 10$ V



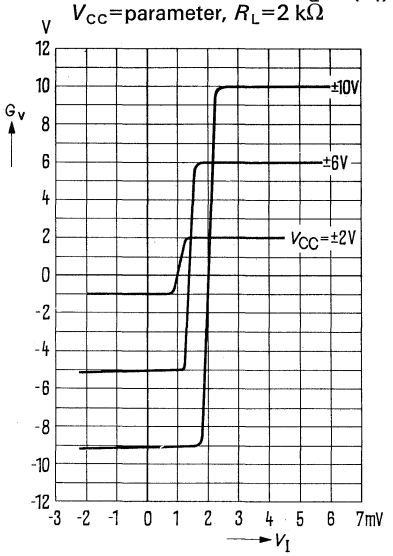
Open-loop voltage gain $G_V = f(T_{amb})$,
$V_{CC} = \pm 10$ V



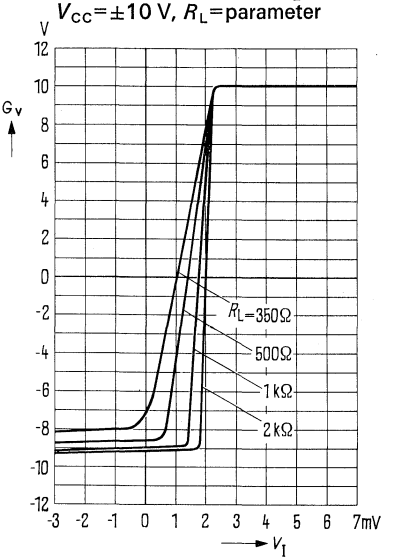
Open-loop gain and phase
$G_V = f(f)$; $\varphi = f(f)$; $V_{CC} = \pm 10$ V
$R_L = 2\,k\Omega$



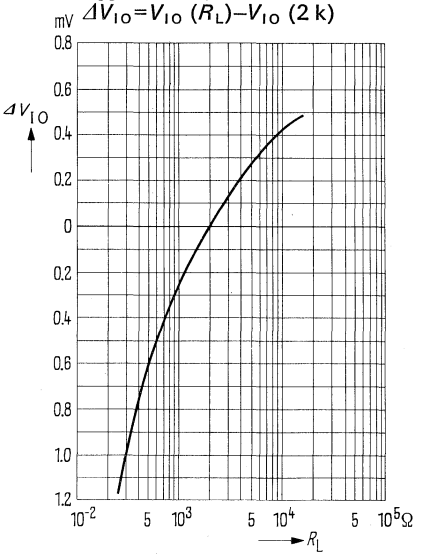
Transfer characteristic $V_Q = f(V_I)$
V_{CC}=parameter, R_L=2 kΩ



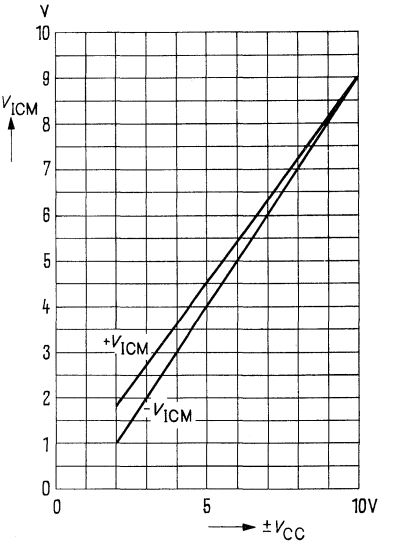
Transfer characteristic $V_Q = f(V_I)$
V_{CC}=±10 V, R_L=parameter



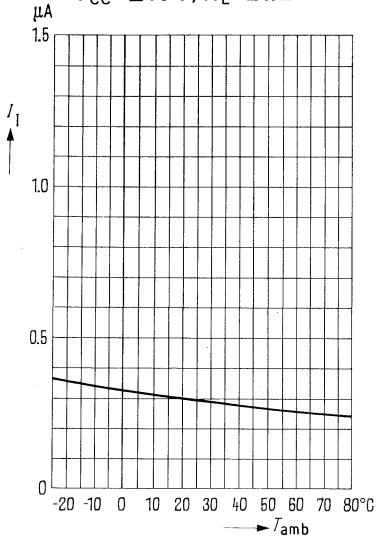
Offset voltage change $\Delta V_{IO} = f(R_L)$
V_{CC}=±10 V
$\Delta V_{IO} = V_{IO}(R_L) - V_{IO}$ (2 k)



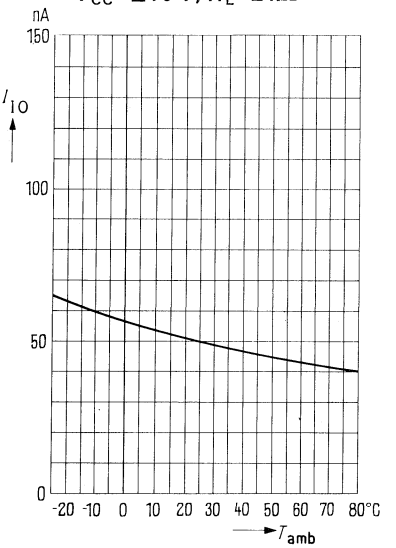
Common mode range
$V_{ICM} = f(V_{CC})$



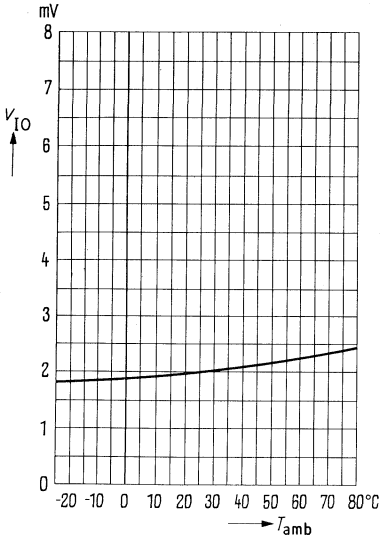
Input current $I_I = f(T_{amb})$
$V_{CC} = \pm 10$ V; $R_L = 2$ kΩ



Input current $I_{IO} = f(T_{amb})$
$V_{CC} = \pm 10$ V; $R_L = 2$ kΩ



Input offset voltage $V_{IO} = f(T_{amb})$
$V_{CC} = \pm 10$ V; $R_L = 2$ kΩ



Ordering codes

TBA 221: Q67000-A134
TBA 221 A: Q67000-A225
TBA 221 B: Q67000-A281
TBA 222: Q67000-A97

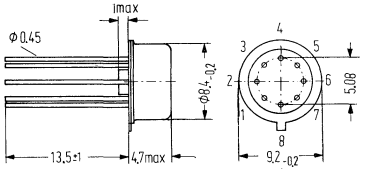
TBA 221
TBA 221 A
TBA 221 B
TBA 222

Operational amplifiers

TBA 221 and TBA 222 are monolithic integrated operational amplifiers in packages similar to 5 G 8 DIN 41873 (TO-99). They are outstanding by their large common-mode voltage range and permanently short-circuit proof. In addition, they feature an adjustable input offset-voltage. The pin-connections correspond to TAA 521, but no external components for frequency compensation are required. An internal gain reduction of 6 db/octave yields maximum stability in feedback circuit applications. TBA 221 A (14 pins), TBA 221 B (8 pins) in plastic plug-in package.

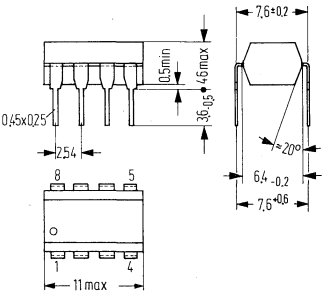
Package outlines

TBA 221, TBA 222



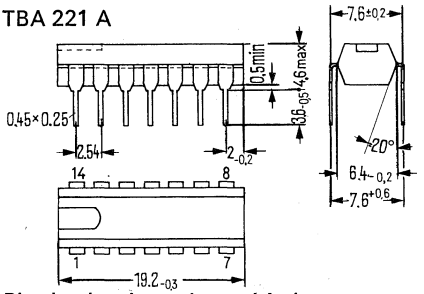
Case similar 5 G 8 DIN 41873 (TO-99)
Weight approx. 1.2 g, dimensions in mm.

TBA 221 B



Plastic plug-in package, 8 pins;
20 A 8 DIN 41866, weight approx. 0.7 g

TBA 221 A



Plastic plug-in package, 14 pins;
20 A 14 DIN 41866 (TO-116), weight approx. 1.1 g

Maximum ratings

		TBA 221 TBA 221 A TBA 221 B	TBA 222	
Supply voltage	V_{CC}	±18	±22	V
Input voltage[1])	V_I	±15	±15	V
Differential input voltage	V_{ID}	±30	±30	V
Storage temperature	T_S	–65 to +150	–65 to +150	°C
Ambient operating temperature	T_{amb}	0 to 70	–55 to +125	°C
Total power dissipation	P_{tot}	500	500	mW
Short circuit duration[2])	t_{SC}	∞	∞	

Notes

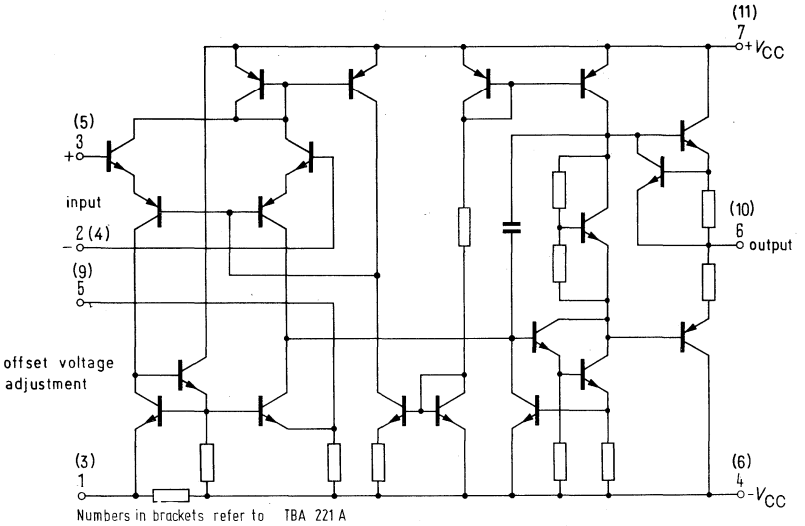
[1]) For supply voltages <±15 V the maximum input voltage is equal to the supply voltage.
[2]) Short circuit may be to ground or to V_{CC}.

TBA 221
TBA 221 A
TBA 221 B
TBA 222

Operating characteristics (V_{CC}=±15 V, T_{amb}=25 °C, unless stated otherwise)

		TBA 221			TBA 222			
		min	typ	max	min	typ	max	
Input offset voltage	V_{IO}			6			5	mV
(R_G≥10 kΩ, T_{amb}=0 to 70 °C)	V_{IO}			7.5				mV
(R_G≥10 kΩ, T_{amb}=–55 to 125 °C)	V_{IO}						6	mV
Input offset current	I_{IO}		30	200		30	200	nA
(T_{amb}=0 to 70 °C)	I_{IO}			300				nA
(T_{amb}=–55 to 125 °C)	I_{IO}						500	nA
Input current	I_I		200	500		200	500	nA
(T_{amb}=0 to 70 °C)	I_I			800				nA
(T_{amb}=–55 to 125 °C)	I_I						1.5	μA
Input resistance	R_I	300	1000		300	1000		kΩ
Output voltage								
(R_L≥10 kΩ)	V_{Qpp}	±12	±14		±12	±14		V
(R_L≥2 kΩ)	V_{Qpp}	±10	±13		±10	±13		V
Input voltage range	V_I	±12	±13		±12	±13		V
Voltage gain (V_{Qpp}=±10 V, R_L≥2 kΩ)	G_V	86	100		94	106		db
Voltage gain (V_{Qpp}=±10 V, R_L≥2 kΩ) T_{amb}=0 to 70 °C)	G_V	83.5						db
Voltage gain V_{Qpp}=±10 V, R_L≥2 kΩ, T_{amb}=–55 to 125 °C)	G_V				88			db
Common mode rejection ratio (R_G≥10 kΩ)	$CMRR$	90	90		70	90		db
Total power dissipation (no load, no signal)	P_{tot}		50	85		50	85	mW
Transient behaviour of the output voltage at G_V=1:								
Rise time (V_I=20 mV, R_L=2 kΩ, C_L<100 pf, V_L=20 mV, R_L=2 kΩ, C_L<100 pf)	t_r		0.3			0.3		μs
Rising edge (R_L≥2 kΩ)	$\frac{dV_{Qpp}}{dt}$		0.5			0.5		V/μs
Temp.-coeff.	of V_{IO}					3		μV/°C
Temp.-coeff.	of I_{IO}					0.4		nA/°C

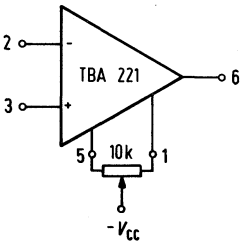
Circuit diagram: TBA 221, TBA 221 A, TBA 221 B, TBA 222



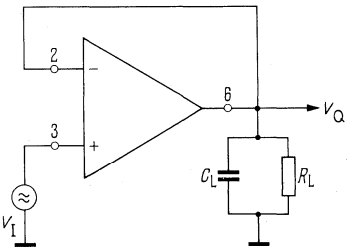
With types TBA 221, TBA 221 A and TBA 222 (plastic plug-in package, 14 pins) pins No. (1), (2), (7), (8), (12), (13) and (14) are not used.

With type TBA 221 B (plastic plug-in package, 8 pins) pin No. 8 is not used.

Offset voltage adjustment circuit



Test circuit for the transient behaviour of V_{QPP}



TBA 830 G
TBA 830 R

Ordeing codes

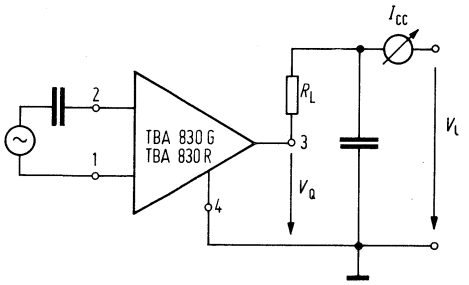
TBA 830 G: Q67000-A546
TBA 830 R: Q67000-A547

Microphone amplifiers

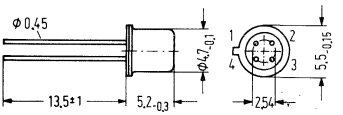
Two-stage microphone amplifiers; the ac output voltage is superimposed on the supply voltage. These amplifiers are especially well suited for piezoelectric microphones in telephone sets.

- gain 40 db
- small change in gain with supply current variations
- good frequency characteristic
- no destruction by reversal of polarity

Test circuit

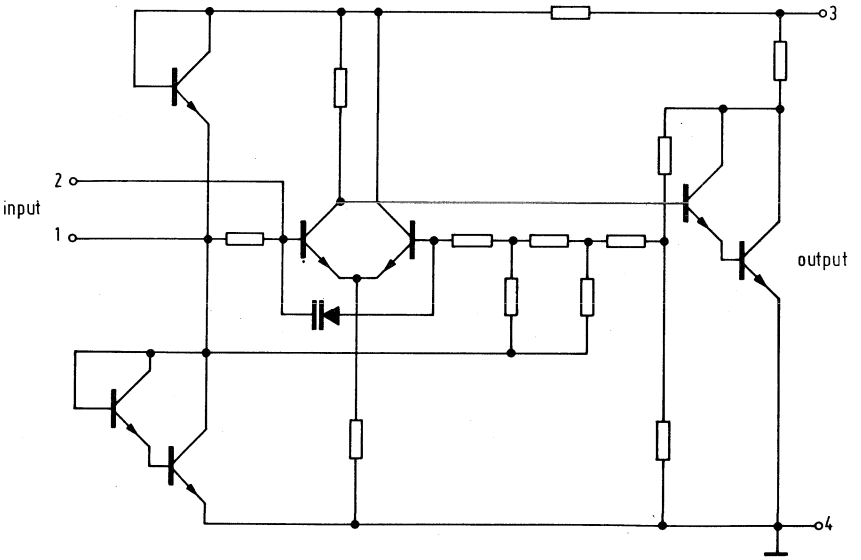


Case outlines:



Case 18 A 4 DIN 41876 (similar TO-72), weight approx. 0.4 g. dimensions in mm.

Circuit diagram



Maximum ratings

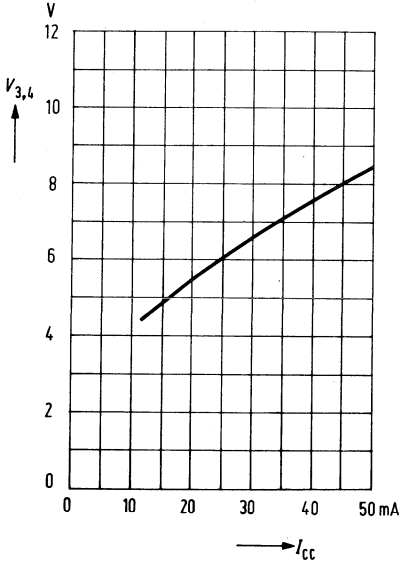
		TBA 830 G TBA 830 R	
Supply voltage	$V_{3,1}$	12	V
Frequency range	f	0 to 20	kHz
Ambient temperature	T_{amb}	–20 to 55	°C
Storage temperature	Ts	–55 to 125	°C
Junction temperature	Tj	150	°C
Power dissipation	P_{tot}	400	mW
Thermal resistance:			
System-case	$R_{thScase}$	150	°C/W
System-ambient air[1])	R_{thSamb}	450	°C/W
Operating range	I_{CC}	12.5 to 50	mA

Operating characteristics (f=1 kHz, R_L=400 Ω, I_{CC}=18 mA, V_{Qrms}=400 mV, T_{amb}=25 °C)

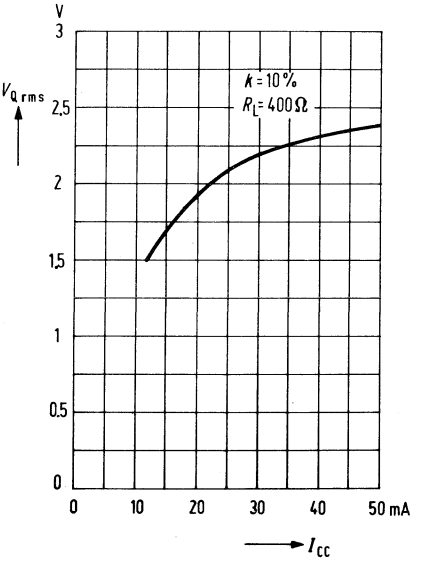
		Test conditions	min	typ	max	
Voltage gain	G_V	for TBA 830 R	38.5	40	42.5	db
	G_V	for TBA 830 G	36	37.5	40	db
Change of gain	ΔG_V	18/12.5 mA			±1	db
	ΔG_V	18/37,5 mA			±1	db
Distortion factor	k			0.5	4	%
Output dc resistance	R_Q			320	400	Ω
Output ac resistance	r_Q		125	170	300	Ω
Input ac resistance	r_I		13	23		kΩ
Max. output ac voltage k=10 %	V_{Qrms}			1.8		V

[1]) when cooled with cooling-clip, R_{thSamb}=320 °C/W

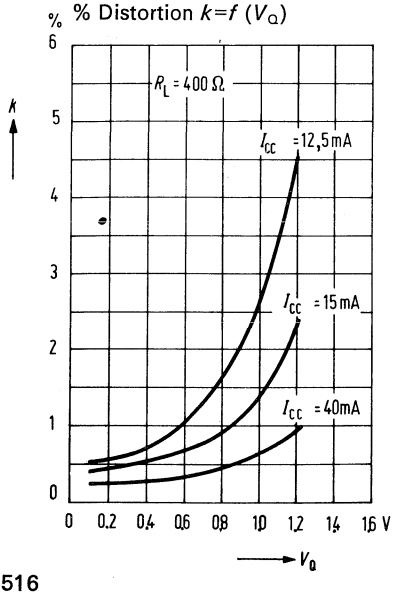
Supply voltage $V_{3,4}=f(I_{CC})$



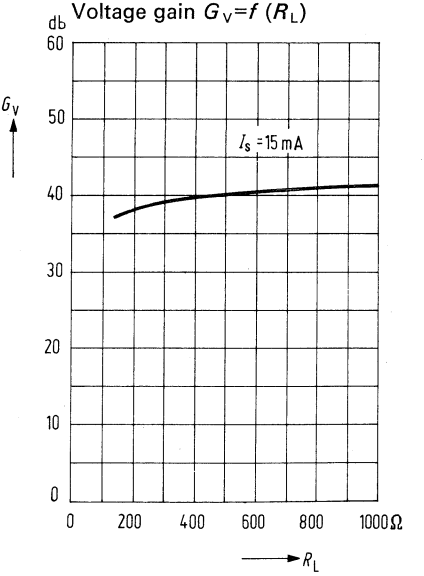
Max. output ac voltage $V_{Q\,rms}=f(I_{CC})$



% Distortion $k=f(V_Q)$



Voltage gain $G_V=f(R_L)$



Ordering codes

TCA 105: Q67000-A527
TCA 105 B: Q67000-A587
TCA 105 BW: Q67000-A601
TCA 105 W: Q67000-A600

TCA 105
TCA 105 B
TCA 105 BW
TCA 105 W

Threshold switches

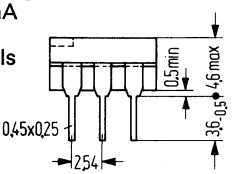
Preliminary data

TCA 105, TCA 105 B, TCA 105 BW and TCA 105 W comprise an oscillator stage, a threshold switch and two anti-valent output stages. In addition, these circuits contain a voltage stabilization and are especially well suited for an application in proximity switches, light beam- and other contactless switching applications.

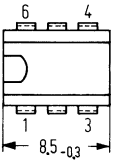
Wide range of battery voltage 4.5 to 30 V
high output current 50 mA
TTL-compatible
triggerable with dc-signals

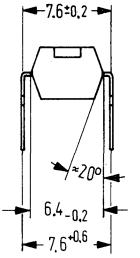
Package outlines

TCA 105, TCA 105 B

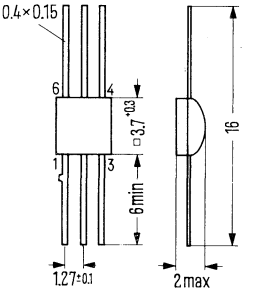


Plastic plug-in package
(6 pins)
20 AG DIN 41866
Weight approx. 0.7 g





TCA 105 W, TCA 105 BW



Miniature-ceramic-case
Weight approx. 0.07 g

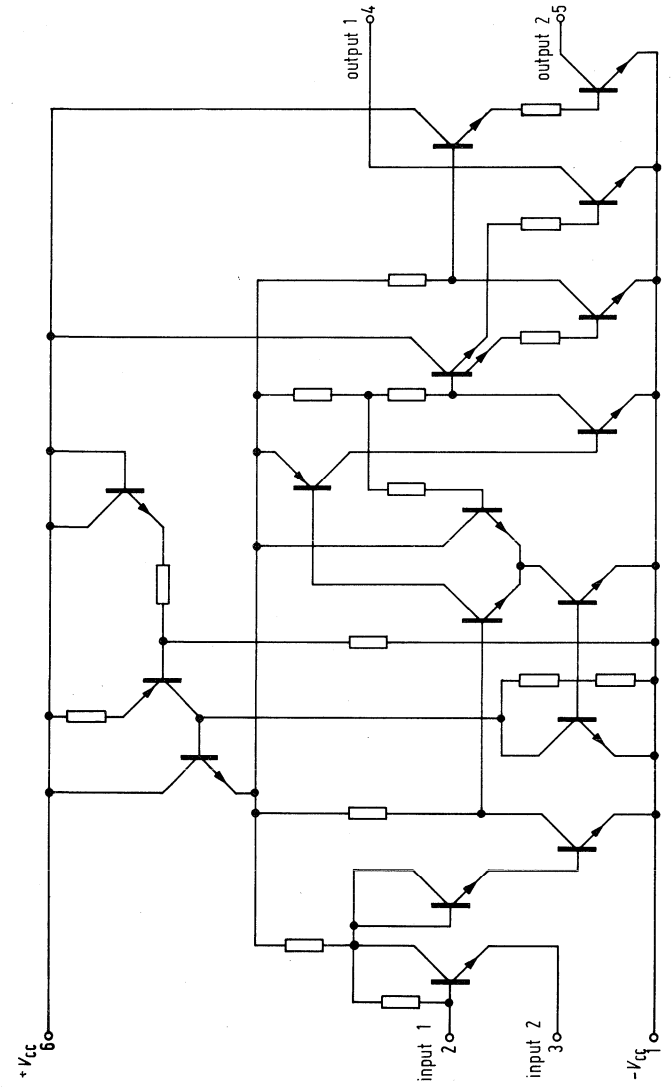
Maximum ratings

		TCA 105 TCA 105 W	TCA 105 B TCA 105 BW	
Supply voltage	V_{CC}	30	20	V
Range of operation	V_{CC}	4.5 to 27	4.5 to 18	V
	f	0 to 15	0 to 15	kHz
Output voltage	V_Q	30	20	V
Output current	I_Q	50	50	mA
Ambient operating temperature	T_{amb}	–25 to 50	–25 to 70	°C
Storage temperature	T_S	–40 to 125	–40 to 125	°C
Termal resistance: System-case	$R_{thS case}$	160	140	°C/W

Operating characteristics

Static measurement, pins 3 and 1 connected (T_{amb}=16 °C, V_{CC}=12 V)

		min	typ	max	
Current requirement	I_{CC}			9.5	mA
Input threshold voltage	V_{th}		750		mV
Input threshold current	I_{th}	30	45	60	µA
Output voltage log. 0					
I_Q=16 mA (TTL fan out=10)	V_{Q0}		0.25	0.35	V
I_Q=50 mA	V_{Q0}		0.70	1.15	V
Output voltage log. 1					
I_Q=16 mA	V_{Q1}	V_{CC}–0.05			V
Rise time (10% to 90%)	t_r		0.5		µs
I_Q=16 mA					
Switching time	t_S		3		µs
(I_Q=16 mA)					


output 1
4
output 2
5
+Vcc
6
input 1
2
input 2
3
-Vcc
1

Ordering code
TCA 315 A: Q67000-A561

TCA 315 A

Operational amplifier

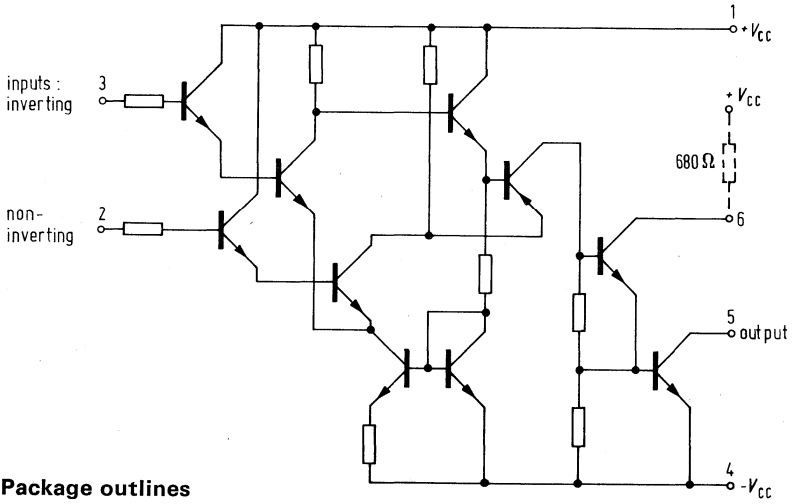
Preliminary data

An economical operational amplifier which is well suited to be used as a Schmitt-trigger or comparator for control applications and automobile electronics. The output has been designed to control TTL-circuits directly. In addition to a high gain, low offset-voltage, small temperature- and supply voltage dependence, the amplifier features

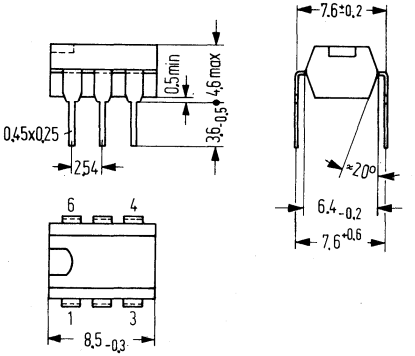
very high input resistance
wide common-mode range
large supply voltage range
large control range

high output current
low output saturation voltage
TTL-compatibility

Circuit diagram



Package outlines



Plastic plug-in package (6 pins)
20 A 6 DIN 41866
weight approx. 0.7 g

TCA 315 A

Maximum ratings

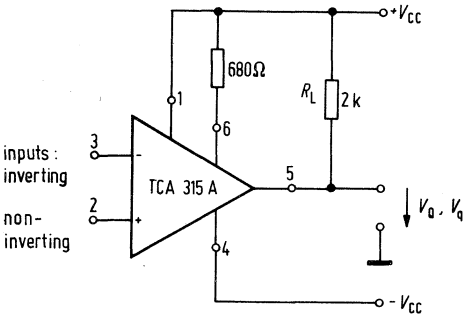
		TCA 315 A	
Supply voltage	V_{CC}	±15	V
Max. output current	I_Q	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	
Range of operation	V_{CC}	±2 to ±15	V
Ambient operating temperature	T_{amb}	0 to +70	°C
Junction temperature	T_j	150	°C
Storage temperature	T_s	−40 to +125	°C
Thermal resistance: System-ambient air	R_{thSamb}	160	°C/W

Operating characteristics
(V_{CC}=±15 V, T_{amb}=25 °C)

		min	typ	max	
Power dissipation (R_L=2 kΩ, V_Q~0)	P_D		150		mW
Current requirement (no load, no signal, I through conn. 2)	I_{CC2}		1.8		mA
Input offset voltage (R_Q=60 Ω)	V_{IO}		10	20	mV
Input offset current	I_{IO}		10	25	nA
Input current	I_I		20	50	nA
Max. output voltage (R_L=2 kΩ)	V_{Qpp}	±14			V
Max. output voltage (R_L=620 Ω)	V_{Qpp}	±12			V
Max. output voltage (R_L=2 kΩ, f=100 kHz)	V_{Qpp}		±10		V
Input impedance (f=1 kHz)	Z_I		3		MΩ
Open-loop voltage gain (R_L=2 kΩ, f=1 kHz)	G_v		84		db
Open-loop voltage gain (R_L=10 kΩ, f=1 kHz)	G_v		90		db
Open-loop voltage gain (R_L=2 kΩ, f=1 MHz)	G_v		35		db
Input common-mode range (R_L=2 kΩ)	V_{ICM}		±13.5		V
Common-mode rejection ratio (R_L=2 kΩ)	$CMRR$		85		db
Supply voltage effect suppression (C_C=1 pf, G_v=100)	$\frac{\Delta V_I}{\Delta V_{CC}}$		35		μV/V
Temp.-coefficient of V_{IO} (R_G=60 Ω)	α_{VIO}		6		μV/°C
Temp.-coefficient of I_{IO} (R_G=60 Ω)	α_{IIO}		0.3		nA/°C
Output saturation voltage (I_Q=10 mA)	V_{QSAT}			350	mV

Connection diagram

R_L=load resistance



TCA 325 A

Ordering code
TCA 325 A: Q67000-A562

Operational amplifier

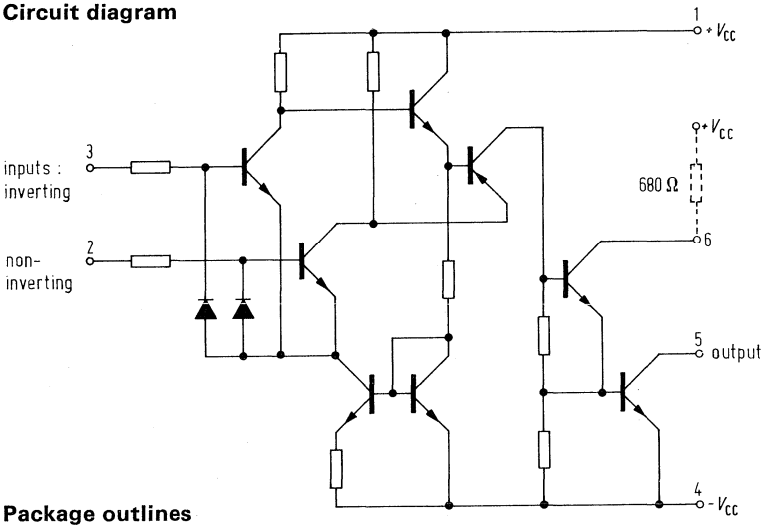
Preliminary data

An economical operational amplifier which is well suited to be used as a Schmitt-trigger or comparator for control applications and automobile electronics. The output has been designed to control TTL-circuits directly. In addition to a high gain, low offset voltage, small temperature- and supply voltage dependence, the amplifier features:

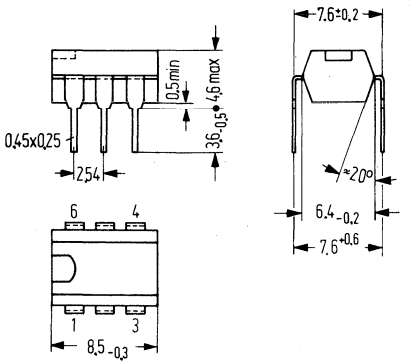
- Wide common-mode range
- wide control range
- high output current
- TTL-compatibility

- large supply voltage range
- protection against destruction
- low output saturation voltage

Circuit diagram



Package outlines



Plastic plug-in package
20 A 6 DIN 41866
(6 pins)
weight approx. 0.7 g

Maximum ratings

		TCA 325 A	
Supply voltage	V_{CC}	±15	V
Max. output current	I_Q	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	
Range of operation	V_{CC}	±2 to ±15	V
Ambient operating temperature	T_{amb}	0 to +70	°C
Junction temperature	T_j	150	°C
Storage temperature	T_s	−40 to +125	°C
Thermal resistance System-ambient air	R_{thSamb}	160	°C/W

Operating characteristics

(V_{CC}=±15 V, T_{amb}=25 °C)

		min	typ	max	
Power dissipation (R_L=2 kΩ, V_Q~0)	P_D		150		mW
Current requirement (no signal, no load, I through conn. 2)	I_{CC2}		1.8		mA
Input offset voltage (R_G=60 Ω)	V_{IO}			7.5	mV
Input offset current	I_{IO}		50		nA
Input current	I_I		0.3	1.0	μA
Max. output voltage (R_L=2 kΩ)	V_{Qpp}	±14			V
Max. output voltage (R_L=620 Ω)	V_{Qpp}	±12			V
Max. output voltage (R_L=2 kΩ, f=100 kHz)	V_{Qpp}		±10		V
Input impedance (f=1 kHz)	Z_I		200		kΩ
Open-loop gain (R_L=2 kΩ, f=1 kHz)	G_v		84		db
Open-loop gain (R_L=10 kΩ, f=1 kHz)	G_v		90		db
Open-loop gain (R_L=2 kΩ, f=1 MHz)	G_v		43		db

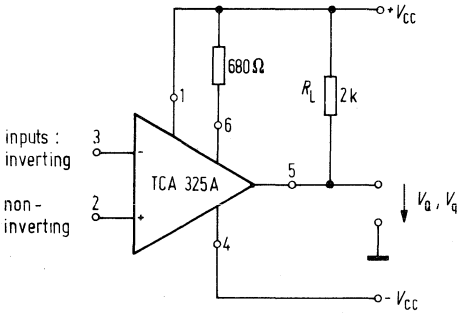
TCA 325 A

Operating characteristics
(V_{CC}=±15 V; T_{amb}=25° C)

		min	typ	max	
Input common-mode range (R_L=2 kΩ)	V_{ICM}		±13.5		V
Common-mode rejection ratio (R_L=2 kΩ)	$CMRR$	80	86		db
Supply voltage effect suppression (C_C=1 pf, G_v=100)	$\frac{\Delta V_I}{\Delta V_{CC}}$		25	200	μV/V
Temp.-coefficient of V_{IO} (R_G=60 Ω)	α_{VIO}		6		μV/°C
Temp.-coefficient of I_{IO} (R_G=60 Ω)	α_{IIO}		0.3		nA/°C
Rise time of V_a for non-inverting operation (TAA 761 test circuit 1)	$\frac{dV_Q}{dt_r}$		9		V/μsec
Rise time of V_a for inverting operation (TAA 761 test circuit 2)	$\frac{dV_Q}{dt_r}$		18		V/μsec
Output saturation voltage (I_Q=10 mA)	V_{QSAT}			350	mV

Connection diagram

R_L=load resistor



Ordering code

TCA 335 A: Q67000-A563

TCA 335 A

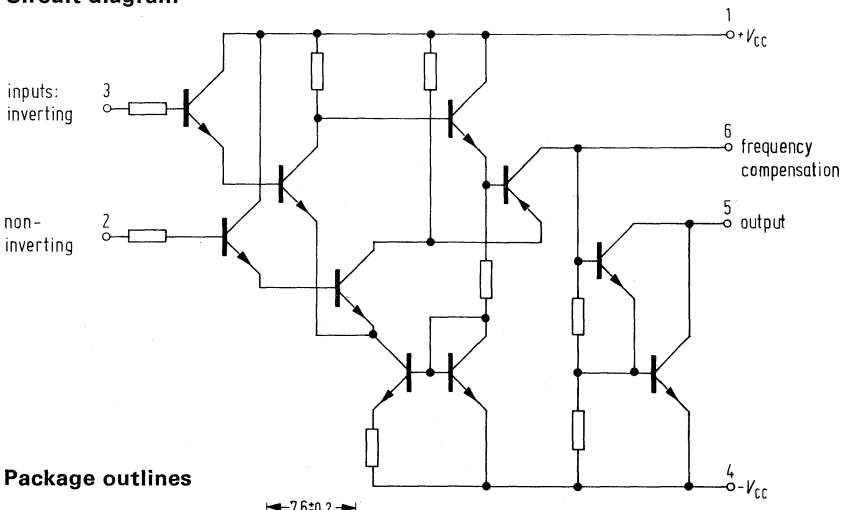
Operational amplifier with Darlington input

Preliminary data

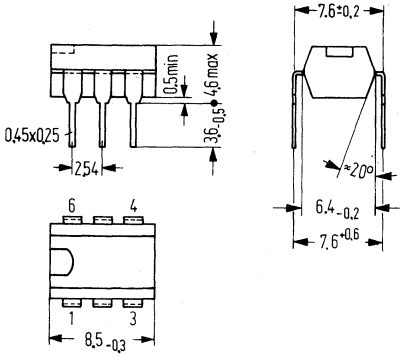
An economical and universal operational amplifier which by its excellent performance qualities is well suited for a wide range of applications such as measurement- and servo-systems, automobile electronics, AF-circuits, analog computers etc. The low input current of this amplifier is particularly advantageous in measurement- and servo-system applications.
In addition to a high gain, low offset voltage, small temperature- and supply voltage-dependence, the amplifier features

- high input resistance
- wide common-mode range
- large supply voltage range
- large control range
- high output current
- simple frequency compensation

Circuit diagram



Package outlines



Plastic plug-in package
(6 pins)
20 A 6 DIN 41866
weight approx. 0.7 g

TCA 335 A

Ordering code
TCA 335 A: Q67000-A563

Maximum ratings

		TCA 335 A	
Supply voltage	V_{CC}	±15	V
Max. output current	I_Q	70	mA
Max. input voltage	V_I	$\pm V_{CC}$	
Range of operation	V_{CC}	±2 to ±15	V
Ambient operating temperature	T_{amb}	0 to +70	°C
Junction temperature	T_j	150	°C
Storage temperature	T_S	−40 to +125	°C
Thermal resistance: System-ambiant air	R_{thSamb}	160	°C/W

Operating characteristics
(V_{CC}=±15 V, T_{amb}=25 °C)

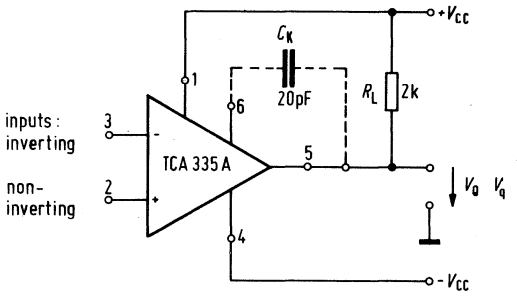
		min	typ	max	
Power dissipation (R_L=2 kΩ, V_Q~0)	P_D		150		mW
Current requirement (no signal, no load, I through conn. 2)	I_{CC2}		1.8		mA
Input offset voltage (R_G=60 Ω)	V_{IO}		10	20	mV
Input offset current	I_{IO}		10	25	nA
Input current	I_I		20	50	nA
Max. output voltage (R_L=2 kΩ)	V_{Qpp}	±14			V
Max. output voltage (R_L=620 Ω)	V_{Qpp}	±12			V
Max. output voltage (R_L=2 kΩ, f=100 kHz)	V_{Qpp}		±10		V
Input impedance (f=1 kHz)	Z_I		3		MΩ
Open-loop voltage gain (R_L=2 kΩ, f=1 kHz)	G_v		84		db
Open-loop voltage gain (R_L=10 kΩ, f=1 kHz)	G_v		90		db
Open-loop voltage gain (R_L=2 kΩ, f=1 MHz)	G_v		35		db

Operating characteristics (continued)
(V_{CC}=±15 V, T_{amb}=25 °C)

		typ	max	
Input common-mode range (R_L=2 kΩ)	V_{ICH}	±13.5		V
Common-mode rejection ratio (R_L=2 kΩ)	$CMRR$	85		db
Supply voltage effect suppression (C_C=1 pf, G_v=100)	$\frac{\Delta V_I}{\Delta V_{CC}}$	35	200	μV/V
Temp. coefficient of V_{IO} (R_G=60 Ω)	α_{VIO}	6		μV/°C
Temp. coefficient of I_{IO} (R_G=60 Ω)	α_{IIO}	0.3		nA/°C

Connection diagram

C_C=Output frequency compensation, R_L=load resistance



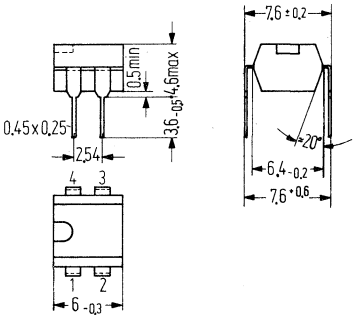
TCA 345 A

Ordering code
TCA 345 A: Q67000-A564

Threshold switch

A threshold switch for battery operation with very low current requirement and low input currents. The threshold is fixed, with a voltage value proportional to the supply voltage.

Package outlines

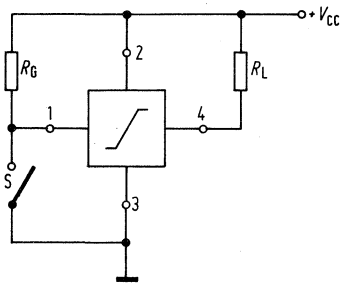


Plastic plug-in package
20 A 4 DIN 41866
(4 pins)
weight approx. 0.5 g

Maximum ratings		**TCA 335 A**	
Output current	I_Q	70	mA
Output voltage	V_{Qpp}	25	V
Supply voltage	V_{CC}	2 and 3	V
Ambient operating temperature	T_{amb}	–25 to 70	°C
Storage temperature	T_S	–35 to 125	°C

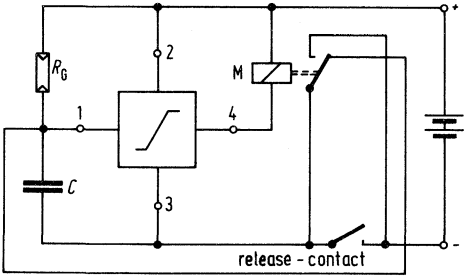
Operating characteristics (V_{CC}=2 V, 3 V, T_{amb}=25 °C)		min	typ	max	
Supply current, for output current I_Q=40 mA					
and V_{CC}=2 V	I_{CC2}		1.8	3.0	mA
V_{CC}=3 V	I_{CC2}		3.0	4.5	mA
Supply current, for output current I_Q=0 and V_{CC}=2 V to 3 V	I_{CC2}			0.8	mA
Rest-voltage for I_Q=40 mA, V_{CC}=2 V	V_{QO}			300	mV
Switching threshold for V_{CC}=2 V	V_I	1.20	1.30	1.45	V
V_{CC}=3 V	V_I	1.80	1.9	2.2	V
(linearly dependent on V_{CC})					
Output leakage current for short-circuited input and V_{CC}=3 V	I_{QG}			10	μA
Switching at:	R_G			20	MΩ

Test circuit



Application example:

Shutter-timing control



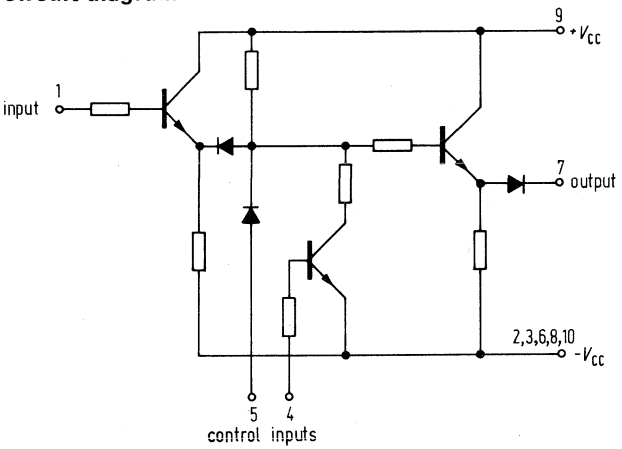
P 1

Ordering code
P 1: Q67000-A528

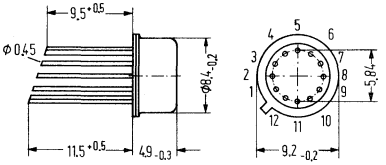
Active matrix-point

The active matrix-point P 1 is used for the switching of signals with a large bandwidth. It may be used, for example, in video distribution networks.

Circuit diagram



Package outlines



Package 5 J 10
DIN 41873
(similar TO-100)
weight approx. 1.1 g

Maximum ratings (T_{amb}=25 °C)		**P 1**	
Supply voltages	V_{CC+}	10	V
	V_{CC-}	10	V
Total power dissipation (T_{case}=45 °C)	P_{tot}	350	mW
Ambient temperature	T_{amb}	–25 to 85	°C
Storage temperature	T_S	–40 to 125	°C

P 1

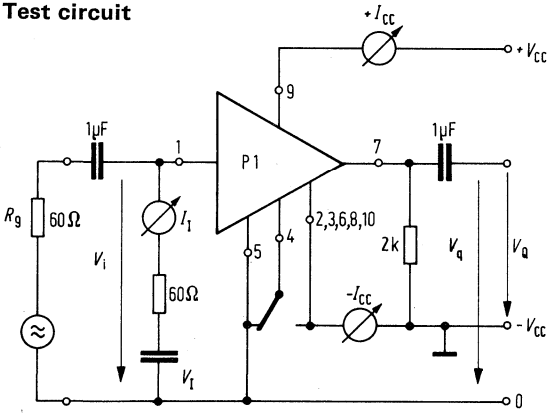
Operating characteristics at V_{CC}=±9 V, V_I=3 V and R_L=2 kΩ (T_{amb}=25 °C), for the test circuit shown below

If desired, the circuits can be supplied in selected groups of dc-shift ($V_{1,7}$)

		Test conditions	min	typ	max	
Output dc-voltage	V_Q		1.20	1.40	1.60	V
DC-shift[1][2]	$V_{1,7}$		1.40	1.60	1.80	V
Max. output voltage	V_{Qrms}	f=1 MHz	1.6	2.0		V
Differential amplitude	V_a/V_i	f=5 MHz		0.3	0.7	%
Differential phase	b/V_i	V_i=0 to 1 V_{pp}		0.07	0.2	°el.
Input current	I_I			25	80	μA
Control current	I_4			50		μA
Signal attenuation	A	f=1 MHz		0.40	0.60	db
Cross-talk suppression[3]	A_{CT}	f=1 MHz	82	87		db
Cross-talk suppression[3]	A_{CT}	f=5 MHz		74		db
Input resistance	R_I			100		kΩ
Output resistance	R_Q	f=1 to 5 MHz		23		Ω
Input capacitance	C_I			3.4		pF
Output inductance	L_Q			600		nH
Cutoff frequency (–3 db)	f_U		20	30		MHz
Current requirement	I_{CC+}	circuit		11	15	mA
	I_{CC-}	conducting		11	15	mA
	I_{CC+}	circuit		12	16	mA
	I_{CC-}	non-conducting		16	21	mA

[1]) Can be selected in groups of $\Delta V_{1,7}$ in 50 mV intervals.
[2]) $V_{1,7}=V_I-V_Q$.
[3]) Connection in a matrix yields a cross-talk suppression which is typically higher by 8 db.

Test circuit



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